MP4008

High-Brightness, High-Current Accuracy WLED Controller

The Future of Analog IC Technology

DESCRIPTION

The MP4008 is a current-mode controller designed for driving high brightness light emitting diodes (LEDs) with a wide input voltage from 9V to 28V. It can be used in boost and SEPIC topologies.

The MP4008 drives an external MOSFET with a fixed frequency architecture to regulate the LED current, which is measured through an external current-sense resistor. The LED current feedback voltage is 280mV. The switching frequency is fixed to 180kHz. The cycle-by-cycle current limit can be programmed by the sense resistor on CS.

The MP4008 employs fast PWM dimming to the LED current with a high dimming ratio.

Integrated protection features include under-voltage lockout, over-voltage protection, over-current protection, short LED protection, short output protection, short inductor/diode protection, and OTP.

The MP4008 is available in a SOIC-8 package.

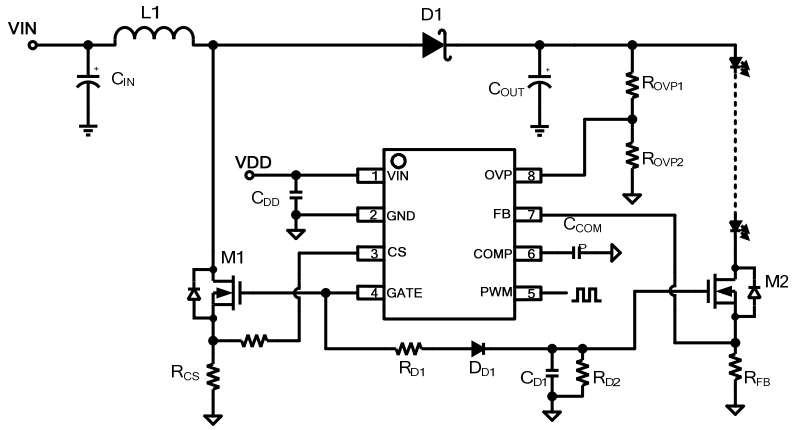
FEATURES

- Constant Current WLED Driver
- 280mV Feedback Voltage with ±1.8% Accuracy
- 9V to 28V Input Voltage
- Leading Edge Blanking for Current Sense
- Frequency Fixed to 180kHz
- Fast PWM Dimming
- Soft Start
- Over-Voltage Protection
- Short LED Protection
- Short Output Protection
- Over-Current Protection
- Short Inductor/Diode Protection
- VIN UVLO
- Thermal Shutdown
- Available in a SOIC-8 Package

APPLICATIONS

- LCD Backlighting
- DC/DC LED Driver
- General Illumination
- Industrial Lighting
- Automotive/ Decorative LED Lighting

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4008GS	SOIC-8	*See Below*

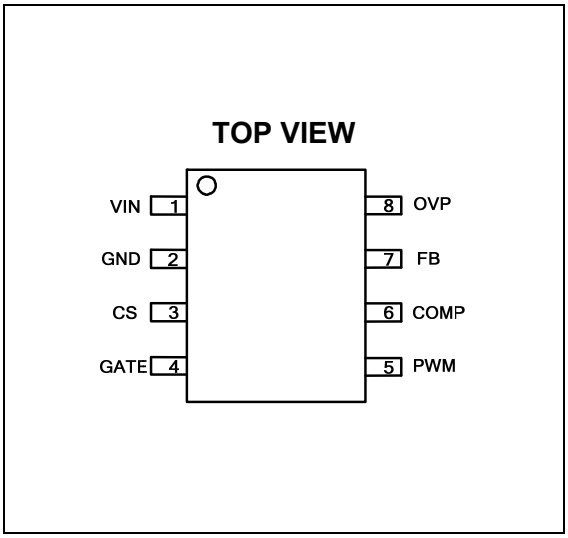
* For Tape & Reel, add suffix –Z (e.g. MP4008GS–Z)

TOP MARKING

MP4008
LLLLLLLL
MPSYWW

MP4008: Part number
LLLLLLLL: Lot number
MPS: MPS Prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}..... -0.3V to 30V
V_{GATE}.....-0.3V to 19V
All other pins.....-0.3V to 6.5V
Junction temperature.....150°C
Lead temperature.....260°C
Continuous power dissipation (T_A = +25°C) **(2)**
SOIC-8.....1.3W

Recommended Operating Conditions (3)

IN supply voltage (V_{IN}) .....9V to 28V
Operating junction temp. T_J.....-40°C to +125°C

Thermal Resistance (4)	***θ_{JA}***	***θ_{JC}***
SOIC-8	96	45

°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		9		28	V
Supply current (quiescent)	I_Q	V_{FB} = 500mV	0.9	1.1	1.3	mA
VIN under-voltage lockout	V_{IN_UVLO}	V_{IN} rising		8.6	9	V
VIN under-voltage lockout hysteresis	$V_{IN\_UVLO\_HYS}$			600		mV
Feedback						
FB feedback voltage	V_{FB}		275	280	285	mV
FB input current	I_{FB}	V_{FB} = 280mV	-0.1		0.1	µA
Oscillator						
Oscillator frequency	f_{OSC}			180		kHz
Maximum duty cycle	D_{MAX}		90	96		%
PWM Dimming						
PWM low threshold	$V_{PWMI-LO}$	V_{PMWI} falling			0.8	V
PWM high threshold	$V_{PWMI-HI}$	V_{PMWI} rising	1.5			V
PWM pull-down resistance	R_{PWM}			1		MΩ
GATE						
GATE high threshold	V_{GATE}		12	13	13.8	V
GATE output rise time	T_{RISE}	C_{GATE} = 1nF, V_{IN} = 12V		40		ns
GATE output fall time	T_{FALL}	C_{GATE} = 1nF, V_{IN} = 12V		40		ns
Current Sense						
Current limit value	V_{CL}	Duty = 0	435	485	535	mV
OCP detect voltage	V_{OCP}	Over-current protection		485		mV
Leading edge blanking time	T_{BLANK}		100	200	300	ns
Compensation						
Transconductance of error amplifier	G_{EA}		380	440	500	µA/V
Maximum sourcing/sinking current	I_{EA}			80		µA
Soft-start current	I_{SS}	V_{FB} < 0.8*REF	15	21	27	µA
Time for COMP saturated protection detection	T_{COMP}			2048		cycle

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Protection						
OVP threshold	V_{OVP-TH}		2.6	2.75	2.9	V
OVP threshold hysteresis	$V_{OVP-HYS}$			410		mV
SCP protection threshold	V_{OVP_SCP}		210	280	350	mV
FB short protection threshold			0.54	0.58	0.62	V
Propagation time for short-circuit detection	T_{OFF}	FB = 620mV		1		µs
Thermal shutdown (5)				150		°C

NOTE:

5) Guaranteed by design.

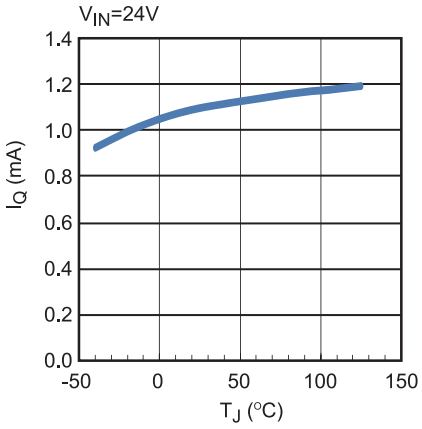
PIN FUNCTIONS

Pin Number	Name	Pin Function
1	VIN	**Input supply, 9V-28V.** VIN is the input of the internal linear regulator. VIN must be bypassed locally.
2	GND	**Ground.**
3	CS	**Switch current sense input.** CS is used to sense the current of the external power FET. It integrates a built-in blanking time to avoid switching noise interruption.
4	GATE	**External MOSFET gate driver.**
5	PWM	**PWM dimming input.** Apply a PWM signal on PWM for brightness control. GATE is disabled when the PWM signal is low. GATE is enabled when the PWM signal is high.
6	COMP	**Compensation.** COMP is used to compensate the regulation control loop. Connect a capacitor or a series RC network from COMP to GND. Also, COMP is used for soft start. When the IC starts up, the current of the internal error amplifier is limited until the output current reaches 80% of the setting current.
7	FB	**Feedback input**, **a 280mV internal feedback voltage**. Connect a current sense resistor from FB to GND. If the FB voltage is higher than 580mV for 1μs, short-load protection is triggered, and the IC latches off.
8	OVP	**Over-voltage protection input.** Connect a resistor divider from the output to OVP to program the OVP threshold. When the OVP voltage reaches the high threshold, the over-voltage protection is triggered. The IC recovers once OVP decreases to the low threshold.

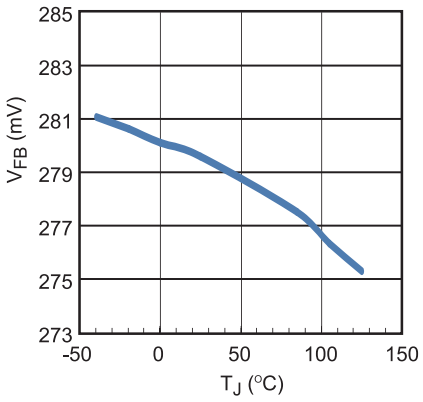
TYPICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

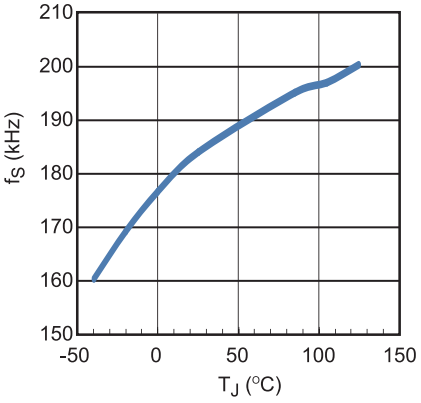
Quiescent Current vs. T_J



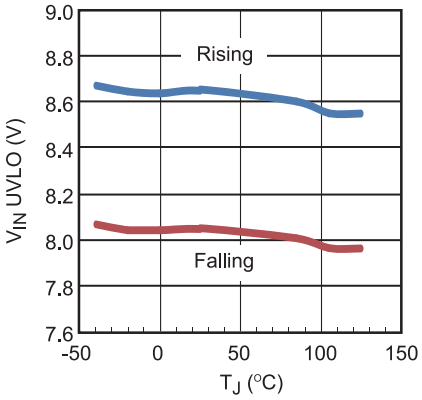
FB Voltage vs. T_J



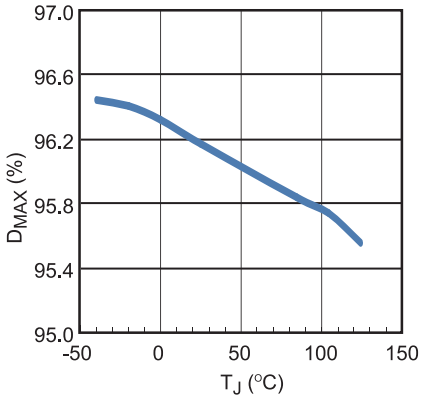
Switching Frequency vs. T_J



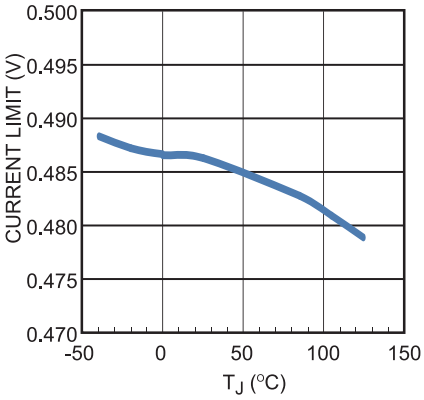
V_{IN} UVLO Threshold vs. T_J



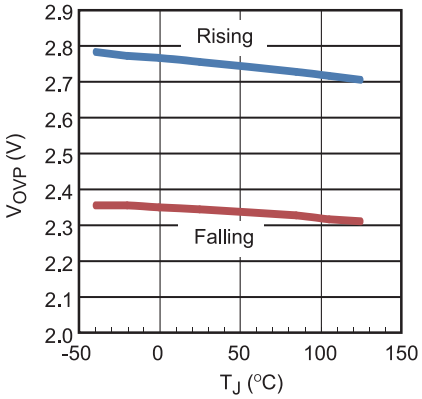
Maximum Duty vs. T_J



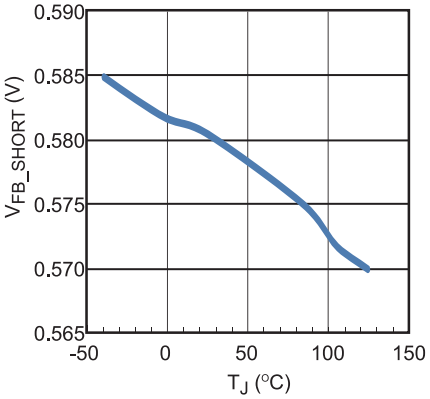
Current Limit Threshold vs. T_J



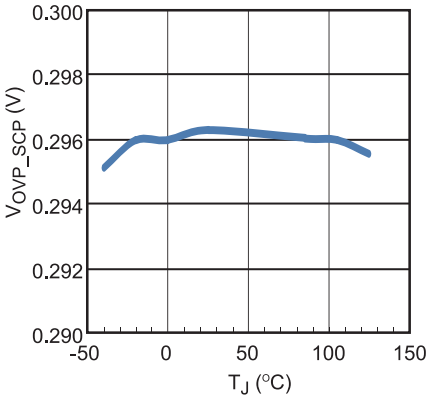
OVP Treshold vs. T_J



FB Short Protection Threshold vs. T_J



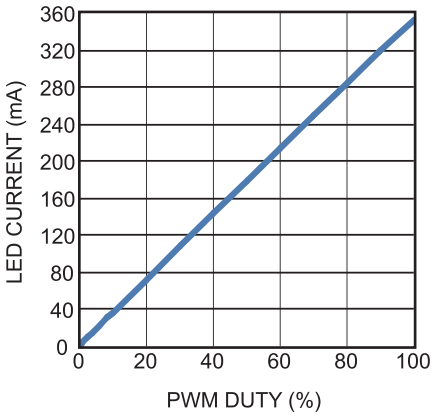
OVP SCP Threshold vs. T_J



TYPICAL PERFORMANCE CHARACTERISTICS

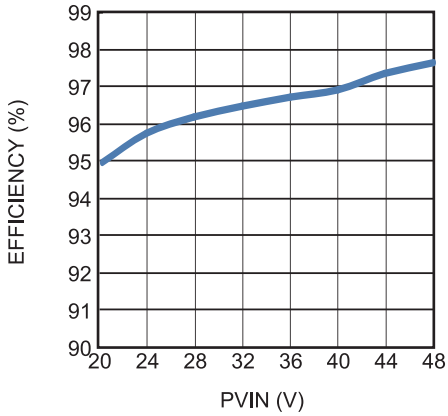
V_{IN} = 12V, PV_{IN} = 20V, V_{LED} = 70V, ILED = 350mA, L = 100µH, T_A = 25°C, unless otherwise noted.

PWM Dimming Curve



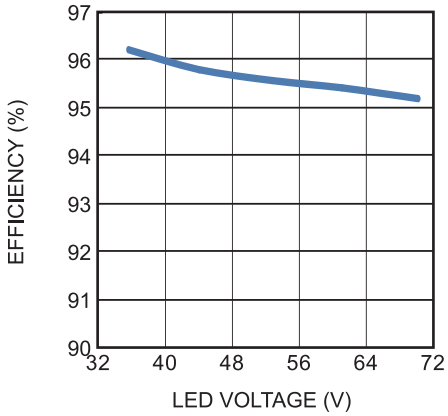
Efficiency vs. PVIN

V_{IN}=12V, V_{LED}=70V



Efficiency vs. V_{LED}

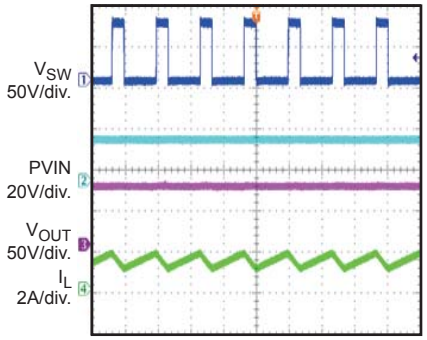
V_{IN}=12V, PVIN=20V



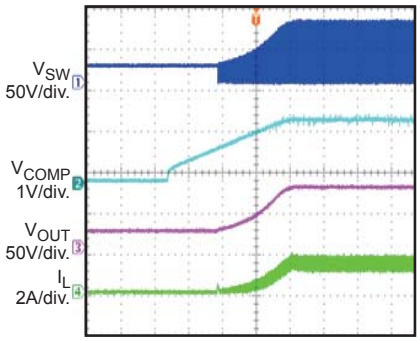
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, PV_{IN} = 20V, V_{LED} = 70V, ILED = 350mA, L = 100µH, T_A = 25°C, unless otherwise noted.

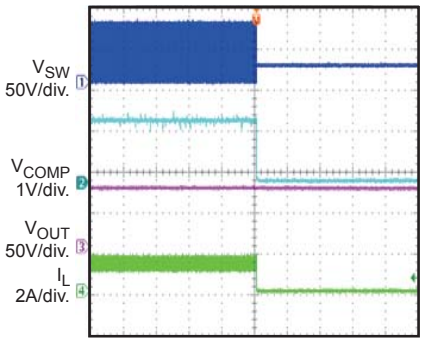
Steady State



V_{IN} Start-Up

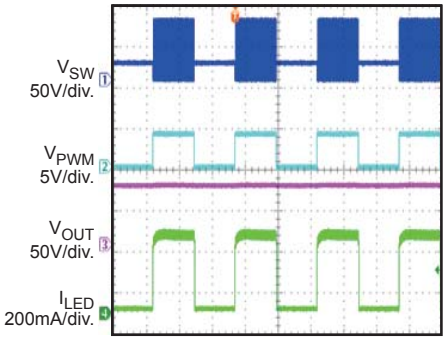


V_{IN} Off

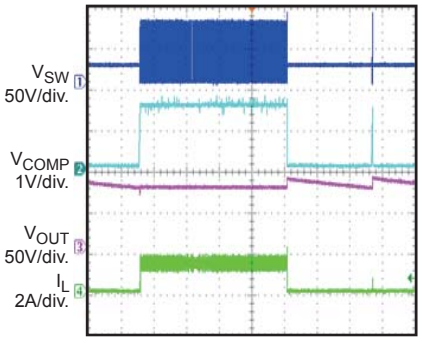


PWM Dimming

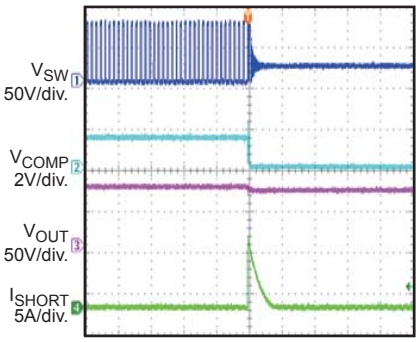
f_{PWM}=200Hz, Duty=50%



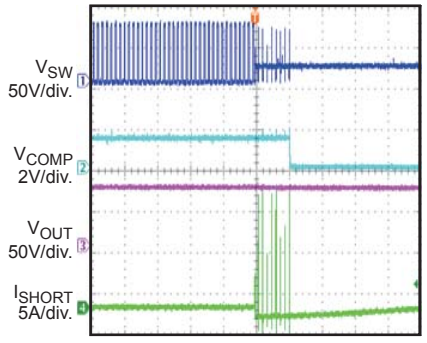
Open-Load Protection



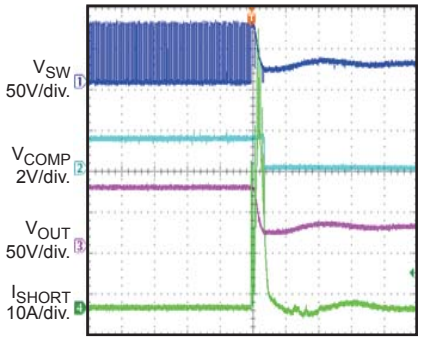
Short-Load Protection



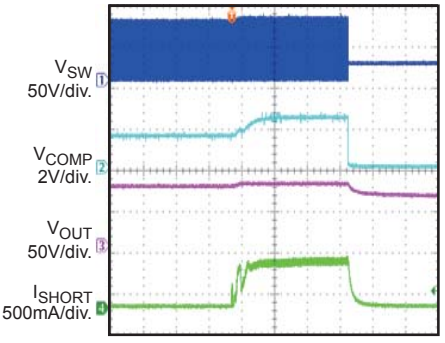
Short-Inductor Protection



Short-Diode Protection



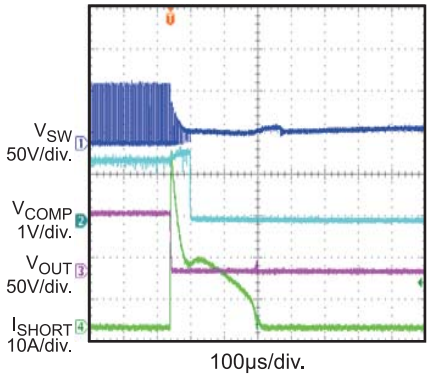
Short LED- to GND Protection



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, PV_{IN} = 20V, V_{LED} = 70V, ILED = 350mA, L = 100µH, T_A = 25°C, unless otherwise noted.

Short LED+ to GND Protection



OPERATION

The MP4008 drives an external MOSFET with current mode architecture to regulate the LED current, which is measured through an external current sense resistor.

The MP4008 employs a special circuit for regulating the internal power supply, which covers a wide input voltage from 9V to 28V. The switching frequency is fixed at 180 kHz.

The slope compensation is integrated to avoid sub-harmonic resonance when the duty cycle is greater than 0.5. The cycle-by-cycle current limit can be programmed by the sense resistor on CS.

The MP4008 integrates under-voltage lockout, over-voltage protection, over-current protection, short LED protection, short-circuit protection, short inductor/diode protection, and OTP.

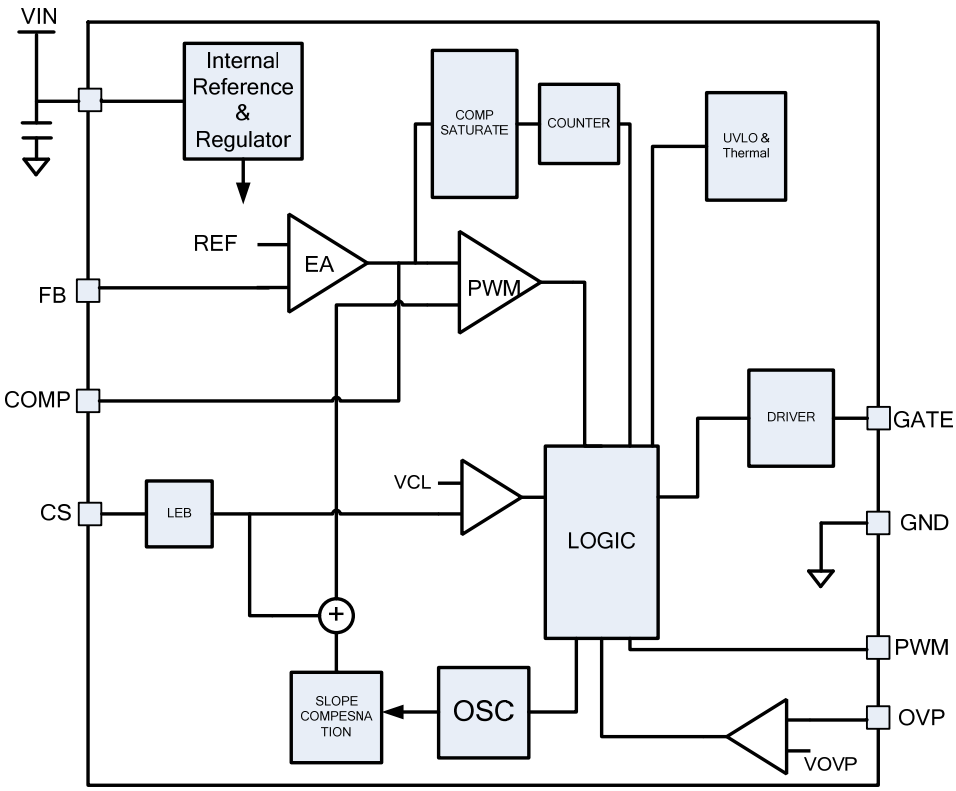


Figure 1: Functional Block Diagram

Soft Start

The MP4008 implements a soft start by limiting the current capability of the internal error amplifier during start-up. The COMP voltage jumps to its clamp voltage (~0.3V) at the beginning of start-up. The sourcing/sinking current of the internal error amplifier is limited to 21μA until the FB voltage reaches 0.8 of the internal reference voltage during start-up (see Figure 2).

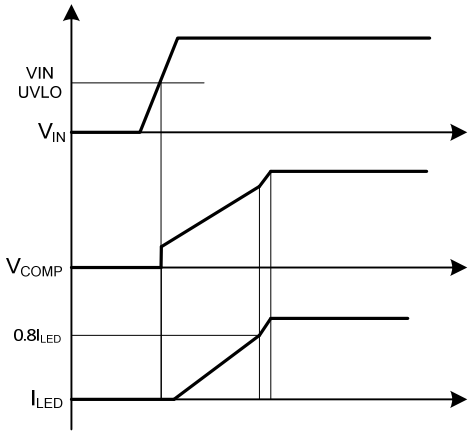


Figure 2: Soft-Start Process

PWM Dimming

PWM dimming is achieved by applying a PWM signal on the PWM pin.

When the PWM signal is high, GATE is enabled, and the external dimming MOSFET is turned on by the driving signal, which is filtered from GATE (see Figure 3). The output of the internal error amplifier is connected to the external compensation network, and the LED current is regulated accurately.

When the PWM signal goes low, the GATE signal is disabled. Meanwhile, the output of the internal error amplifier is disconnected from the compensation network, and the COMP voltage is held by the external capacitor. The dimming MOSFET turns off to prevent the output voltage from being discharged.

The internal oscillator is synchronized by the PWM dimming signal to achieve good performance with a small dimming ratio.

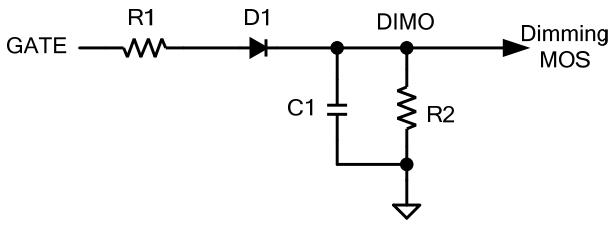


Figure 3: Dimming Signal Filtered from GATE

Protection

The MP4008 includes under-voltage lockout, over-voltage protection, short-load protection, short-circuit protection, over-current protection, and short inductor/diode protection. If fault conditions are detected, GATE and COMP are pulled down.

A. Under-Voltage Lockout

The MP4008 integrates VIN UVLO. The internal circuit does not work until the VIN voltage reaches the UVLO rising threshold. The hysteresis of VIN UVLO is 600mV.

B. Over-Voltage Protection

Over-voltage protection is detected by the voltage of OVP. When the OVP voltage rises to its high threshold, the over-voltage protection is triggered, and GATE and COMP are pulled low. The IC recovers once the OVP voltage decreases to its low threshold.

C. Short-Load Protection

In a short-load condition, a large short current is detected by the FB sense resistor. If the FB sensed voltage is higher than 580mV and lasts for 1μs, the short-load protection is triggered; GATE and COMP are pulled low, and the IC latches off.

D. Short-Circuit Protection

In a short-circuit condition, the output voltage is pulled low and no current is sensed on FB. If the following conditions are satisfied, OVP < 280mV, FB < 0.3*REF, and COMP > 1V, the short-circuit protection is triggered. GATE and COMP are pulled low, and the IC latches off.

Figure 4 shows the circuit for short-circuit protection. It uses a PMOS for both PWM dimming and short-circuit protection. When LED+ is shorted to GND, GATE pulls low, and the PMOS turns off to cut off the short loop.

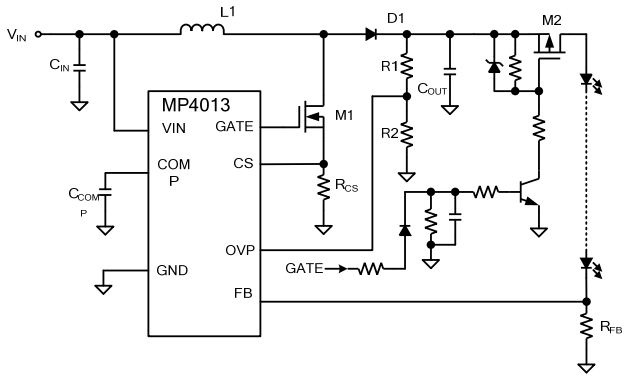


Figure 4: Short-Circuit Protection Scheme

E. Over-Current Protection (Short Inductor/ Diode Protection)

The MP4008 implements a cycle-by-cycle current limit function for protection. In normal operation, the over-current protection is recoverable.

In unexpected cases (inductor or diode shorts), when the voltage of CS, which is detected by an external CS sense resistor, hits the latch-off current limit value within the 300ns turn-on time for 7 consecutive cycles, the over-current protection is triggered; GATE and COMP are pulled low, and the IC latches off.

F. LED- to GND Short Protection

In an LED- to GND short condition, the FB senses no current which causes the COMP to charge to its saturated value. If COMP remains saturated for 2048 switching cycles, and FB is below 30% of the internal reference, protection is triggered; GATE and COMP are pulled low, and the IC latches off.

APPLICATION INFORMATION

LED Current Setting

The LED current is set by the LED current sense resistor (R_{FB}). See Equation (1):

$$R_{FB} = \frac{280mV}{I_{LED}} \quad (1)$$

Selecting the Inductor

Select an inductor that allows the circuit to work in continuous conduction mode (CCM). See Equation (2):

$$L = \frac{V_{IN} \times (V_O - V_{IN})}{V_O \times \Delta I_L \times f_S} \quad (2)$$

Where, ΔI_L is the peak-to-peak current of the inductor current. Design the ΔI_L to be 30% to 60% of the inductor average current. See Equation (3):

$$I_{L\_AVG} = \frac{V_O \times I_{LED}}{V_{IN}} \quad (3)$$

Ensure the inductor saturated current is greater than the inductor peak current. See Equation (4):

$$I_{L\_PK} = I_{L\_AVG} + \frac{1}{2}\Delta I_L \quad (4)$$

Current Sense Resistor Setting

The cycle-by-cycle current limit and slope compensation are both integrated. The current limit value is programmed by the external CS resistor, which connects from CS to GND. The maximum value of the CS sense resistor can be set using Equation (5):

$$R_{CS1}(\Omega) = \frac{0.435\text{-}0.27 \times D}{I_{L\_pk}} \quad (5)$$

Where, D is the duty cycle of the GATE signal in CCM. See Equation (6):

$$D = 1 - \frac{V_{IN}}{V_O} \quad (6)$$

I_{L_PK} is the peak current of the inductor.

The slope compensation is integrated to avoid sub-harmonic resonance when the duty is larger than 0.5 in CCM. Equation (7) must be satisfied:

$$R_{CS2}(\Omega) \le 9.7 \times 10^{-2} \times \frac{L(\mu H)}{V_L(V)} \quad (7)$$

Where, V_L is the voltage across the inductor when GATE is off. See Equation (8):

$$V_L(V) = V_{O\,max} - V_{IN\,min} \quad (8)$$

The CS resistance must be less than R_{CS1} and R_{CS2}.

Over-Voltage Protection Setting

Choose a voltage divider (R1 and R2 in typical application) to set the over-voltage protection threshold. See Equation (9):

$$V_{OVP} = 2.75V \times \frac{R1 + R2}{R2} \quad (9)$$

Set the OVP point 10%-20% higher than the maximum output voltage in normal operation.

Selecting the MOSFET and Diode

There are two MOSFETs for MP4008 application: One is for the boost converter (the power MOSFET), and the other is for PWM dimming (the dimming MOSFET).

Choose a power MOSFET with breakdown voltage at least 20% higher than the OVP point to ensure safety in all conditions.

The RMS current of the MOSFET can be calculated using Equation (10):

$$I_{RMS} = \sqrt{D \times (I_{L\_AVG}^2 + \frac{1}{12}\Delta I_L^2)} \quad (10)$$

Where, D is the duty cycle.

Choose a dimming MOSFET with a voltage rating 20% higher than the OVP point, and a current rating about 3-5 of the LED current.

Choose a diode with a voltage rating greater than the OVP point (at least 20% higher), and a current rating greater than the LED current.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. Use a ceramic capacitor with an X7R dielectric, low ESR, and small temperature coefficient.

Select a capacitor to limit the input voltage ripple(ΔV_{IN}) to less than 5% to 10% of its DC value. See Equation (11):

$$C_{IN} \geq \frac{\Delta I_L}{8 \times \Delta V_{IN} \times f_s} \quad (11)$$

Selecting the Output Capacitor

The output capacitor limits the output voltage ripple ΔV_O (normally less than 1% to 5% of its DC value) and ensures feedback loop stability. See Equation (12):

$$C_{OUT} \geq \frac{I_{LED} \times (V_O - V_{IN})}{\Delta V_O \times f_s \times V_O} \quad (12)$$

Compensation Network Setting

The MP4008 implements peak-current-mode control to regulate the LED current through a compensation network on COMP. Usually, an RCC network is adopted for most applications (see Figure 5).

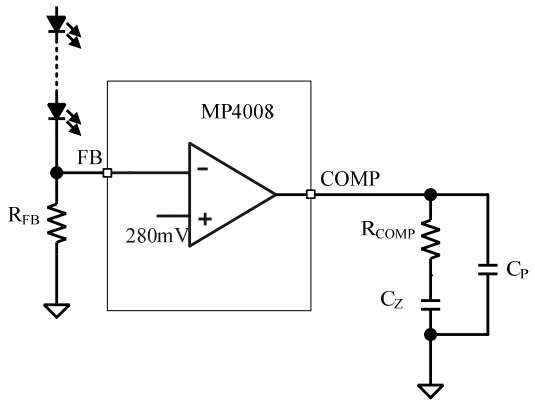


Figure 5: Compensation Network

The transfer function of the compensation network is calculated using Equation (13). Assume C_Z>>C_P.

$$EA(s) \approx \frac{G_{EA} \times R_{FB}}{R_{FB}+R_{LED\_AC}} \times \frac{1}{s \times C_Z} \times \frac{1+s \times C_Z \times R_{COMP}}{1+s \times C_P \times R_{COMP}} \quad (13)$$

Where, G_{EA} is the transconductance of the internal error amplifier (G_{EA} = 440μA/V), and R_{LED_AC} is the dynamic resistor of the LED load. R_{LED_AC} is calculated using Equation (14):

$$R_{LED\_AC} = \frac{\Delta V_{LED}}{\Delta I_{LED}} \quad (14)$$

The zero of the compensation network is calculated using Equation (15):

$$f_{Z\_EA} = \frac{1}{2\pi \times C_Z \times R_{COMP}} \quad (15)$$

The pole of this compensation network is calculated using Equation (16):

$$f_{P\_EA} = \frac{1}{2\pi \times C_P \times R_{COMP}} \quad (16)$$

The power stage of the boost converter is calculated using Equation (17):

$$f_{P\_PS} = \frac{1}{2\pi \times (\frac{V_O}{I_{LED}} // (R_{LED\_AC} + R_{FB})) \times C_{OUT}} \quad (17)$$

Where, V_O is the output voltage, I_{LED} is the LED current, and C_{OUT} is the output capacitance.

The right-half-plane (RHP) zero of the boost converter stage is calculated using Equation (18):

$$f_{RHP\_Z} = \frac{(1-D)^2 \times \frac{V_O}{I_{LED}}}{2\pi \times L} \quad (18)$$

Choose a cross frequency (fc) below 1/5 of f_{RHP_Z} to get the R_{COMP} value. See Equation (19):

$$R_{COMP} = \frac{R_{LED\_AC}+R_{FB}}{R_{FB}} \frac{fc \times C_{OUT} \times 2\pi}{G_{EA} \times (1-D) \times G_{CS}} \quad (19)$$

Where, G_{CS} is the conductance of the CS circuit.

The zero of the compensation network is used to compensate the power-stage pole. See Equation (20):

$$C_Z = \frac{1}{2\pi \times f_{PS\_P} \times R_{COMP}} \quad (20)$$

The pole of the compensation network is used to compensate the RHP zero. See Equation (21):

$$C_P = \frac{1}{2\pi \times f_{RHP\_Z} \times R_{COMP}} \quad (21)$$

TYPICAL APPLICATION CIRCUIT

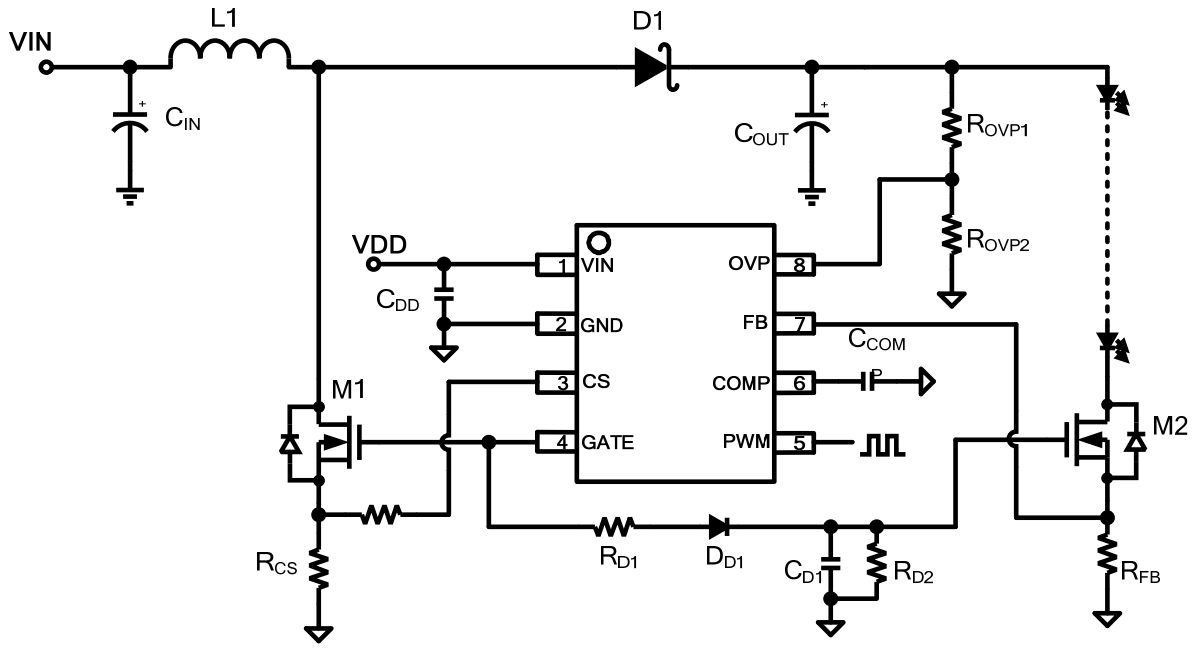


Figure 6: Boost Application

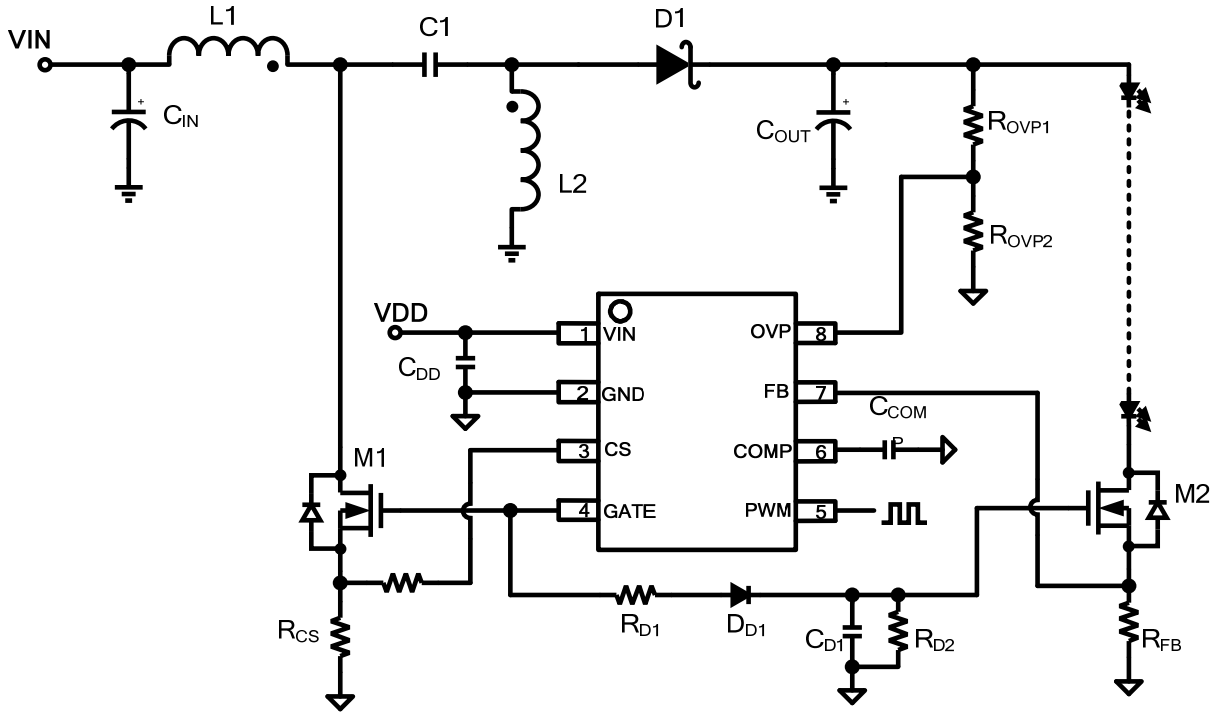
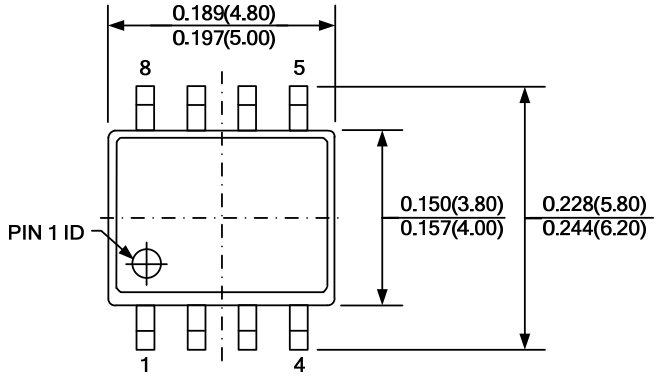


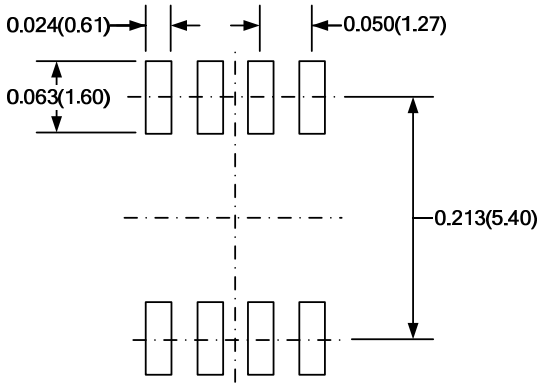
Figure 7: SEPIC Application

PACKAGE INFORMATION

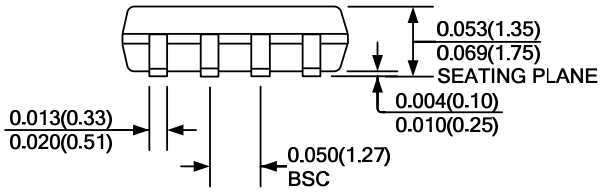
SOIC-8



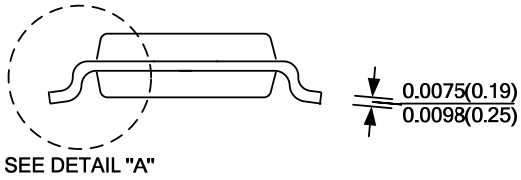
TOP VIEW



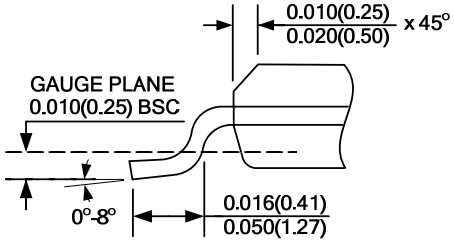
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.