DC to 30GHz Broadband MMIC Low-Power Amplifier

Features

- Integrated LFX technology:
  - Simplified low-cost assembly
  - Drain bias inductor not required
- Broadband 45GHz performance:
  - Good gain (10 ± 1.25dB)
  - 14.5dBm Psat, 11.5dBm P1dB
  - Low Noise Figure (5.5dB)
- >30dB dynamic gain control
- Integrated power detector
- 100% DC, RF, and visually tested
- Size: 1640x1100um (64.6x43.3mil)
- ECCN 3A001.b.2.d

Description

The MMA033AA is a seven stage traveling wave amplifier. The amplifier features Microsemi active LFX (Low Frequency eXtension) circuitry designed to reduce the integration cost of the amplifier. LFX eliminates the need for an off-chip bias choke (drain inductor) for low-frequency operation, simplifying and greatly reducing the cost of assembly.

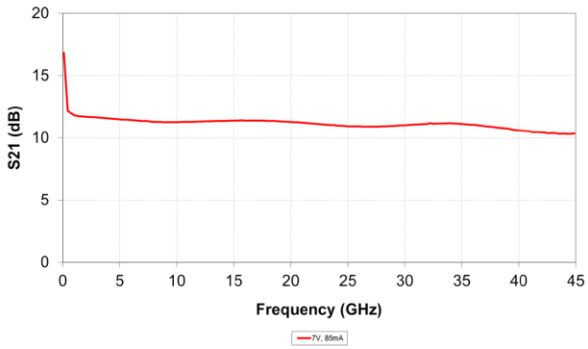
Application

The MMA033AA Broadband MMIC Amplifier with LFX is designed for inexpensive integration in broadband applications in RF and microwave communications, test equipment and military systems.

Key Characteristics: Vdd=7V, Idd=85mA, Zo=50Ω
Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

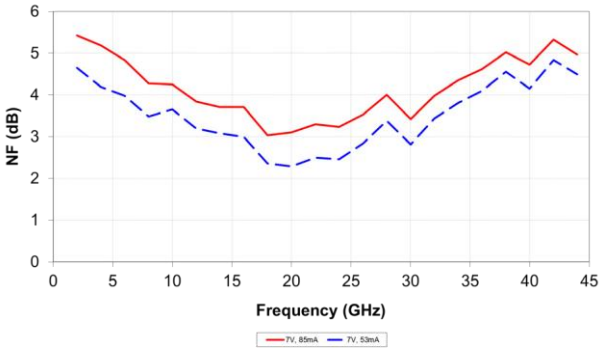
		1.5 - 40GHz			0.04 - 45GHz		
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
S21 (dB)	Small Signal Gain	9	10.5	-	8.5	10	-
Flatness (±dB)	Gain Flatness	-	1	1.5	-	1.25	1.75
S11 (dB	Input Match	-	-10	-8	-	-10	-8
S22 (dB)	Output Match	-	-12	-10	-	-12	-10
S12 (dB)	Reverse Isolation	-	-26	-20	-	-24	-20
P1dB (dBm)	1dB Compressed Output Power	11.5	13	-	10	11.5	-
Psat (dBm)	Saturated Output Power	14	15.5	-	13	14.5	-
NF (dB)	Noise Figure	-	5.5	-	-	5.5	-
RFdet (mV/mW)	RF Detector Sensitivity	-	0.7	-	-	0.7	-

S21



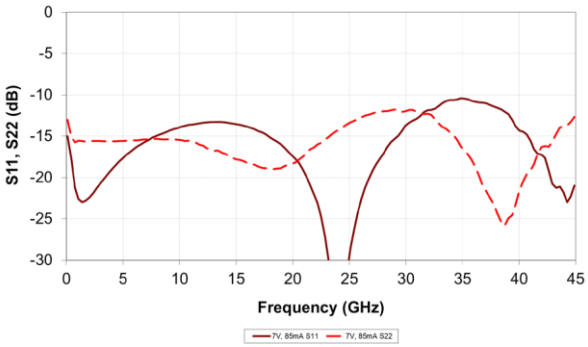
Typical IC performance measured on-wafer

Noise Figure



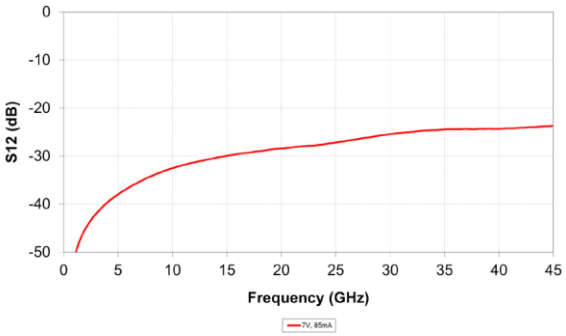
Typical IC performance with package de-embedded

S11, S22



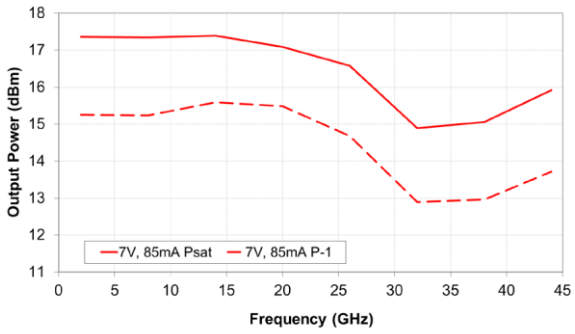
Typical IC performance measured on-wafer

S12



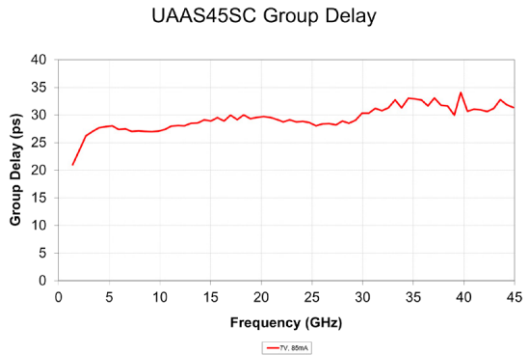
Typical IC performance measured on-wafer

Output Power



Typical IC performance measured on-wafer

Group Delay



Typical IC performance measured on-wafer

Table 1: Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd	Drain Bias Voltage	5V	7V	7.5V
Idd	Drain Bias Current	-	85mA	120mA
Vg1	1st Gate Bias Voltage	-4V	-	+0.5V
Vg2	2nd Gate Bias Voltage	Vdd-Vg2<7V	N/C	+4V
P_{in}	Input Power (CW)	-	-	20dBm
P_{dc}	Power Dissipation	-	0.595W	-
T_{ch}	Channel Temperature	-	-	150°C
Q_{ch}	Thermal Resistance (Tcase=85°C)	-	22°C/W	-

Caution, ESD
Sensitive Device

DC Bias:

The MMA033AA features a patented on-chip active bias circuit called 'LFX'. This circuit provides DC bias to the TWA drains without affecting RF performance; traditional biasing requires off-chip decoupling that increases the assembly complexity and cost.

The device is biased by applying a positive voltage to the drain (Vdd), then setting the drain current (Idd) using a negative voltage on the gate (Vg1). The nominal bias is Vdd=7.0V, Idd=85mA; this will typically bring RFout (and the drain sense) to 4.5V.

Improved performance can be achieved with gate bias adjustment; use the drain termination bypass to alter the output voltage (detected from the drain voltage sense).

Gain Control:

Dynamic gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to the second gate (Vg2) reduces amplifier gain.

RF Power Detection:

RF output power can be calculated from the difference between the RF detector voltage and the DC detector voltage, minus a DC offset. Please consult the power detector application note available from the Microsemi webpage.

Low-Frequency Use:

The MMA033AA has been designed so that the bandwidth can be extended to low frequencies. The low end corner frequency of the device is primarily determined by the external biasing and AC coupling circuitry.

Matching:

The amplifier incorporates an on- chip termination resistor on the RF input, which is RF grounded with a small on-chip capacitor that goes open at frequencies below 1GHz. Gate termination bypass pads are provided for an external capacitor required for input match during low-frequency operation.

The RF output is RF grounded through the bypass capacitor connected to the drain bias pad (Vdd). This capacitor will maintain the output match to low-MHz operating frequencies.

For operation below 1GHz, a second bypass capacitor must be connected to the drain termination bypass, as shown in the assembly diagrams.

DC Blocks:

The amplifier is DC coupled to the RF input and output pads; DC voltage on these pads must be isolated from external circuitry.

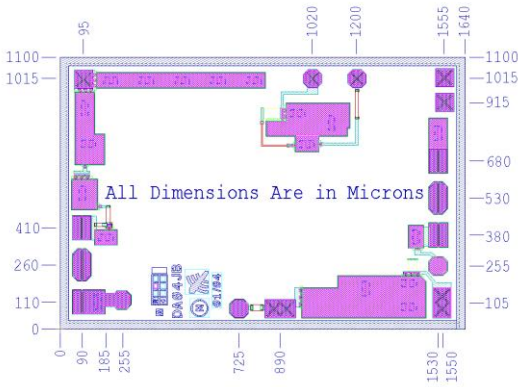
For operation above 2GHz, a series DC-blocking capacitor with minimum value of 20pF is recommended; operation at 40MHz requires a minimum of 120pF.

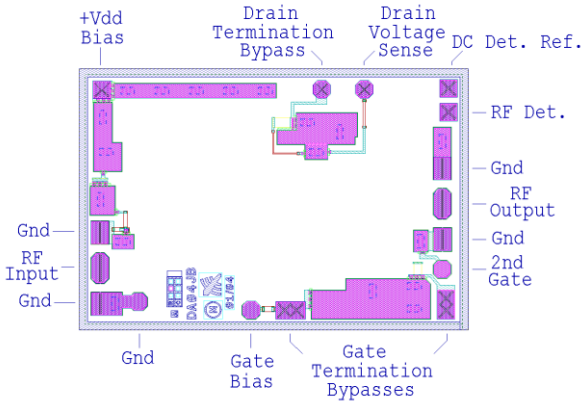
Bias Inductor:

The patented on-chip LFX circuit eliminates the need for a drain bias choke; the amplifier requires a bypass capacitor close to the chip and bonded to the drain bias pad. The drain bias supply is connected directly to the bypass capacitor.

Die size, pad locations, and pad descriptions

Chip size: 1640x1100um (64.6x43.3mil)
Chip size tolerance: ±5um (0.2mil)
Chip thickness: 100 ±10um (4 ±0.4mil)
Pad dimensions: 80x80um (3.1x3.1mil)





Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center;** handle from edges or with a collet.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please review our application note MM-APP-0001 on our website for more handling, die attach and bonding information.

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