

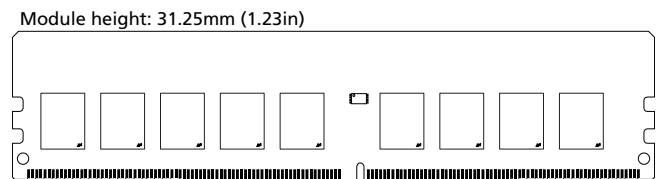
# DDR4 SDRAM UDIMM

## MTA16ATF1G64AZ – 8GB

### Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC4-2400, PC4-2133, or PC4-1866
- 8GB (1 Gig x 64)
- $V_{DD} = 1.20V$  (typical)
- $V_{PP} = 2.5V$  (typical)
- $V_{DDSPD} = 2.2\text{--}3.6V$
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die  $V_{REFDQ}$  generation and calibration
- Dual-rank
- On-board serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 288-Pin UDIMM (MO-309, R/C-B)**



### Options

- Operating temperature
  - Commercial ( $0^{\circ}C \leq T_{OPER} \leq 95^{\circ}C$ )
- Package
  - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
  - 0.83ns @ CL = 16 (DDR4-2400)
  - 0.93ns @ CL = 15 (DDR4-2133)
  - 1.07ns @ CL = 13 (DDR4-1866)

### Marking

None  
Z  
-2G4  
-2G1  
-1G9

**Table 1: Key Timing Parameters**

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								$t_{RCD}$ (ns)	$t_{RP}$ (ns)	$t_{RC}$ (ns)
		CL = 18	CL = 16	CL = 15	CL = 14	CL = 13	CL = 12	CL = 11	CL = 9			
-2G4	PC4-2400	2400	2400	2133	1866	1866	1600	1600	1333	13.32	13.32	45.32
-2G1	PC4-2133	–	2133	2133	1866	1866	1600	1600	1333	13.5	13.5	46.5
-1G9	PC4-1866	–	–	–	1866	1866	1600	1600	1333	13.5	13.5	47.5



## 8GB (x64, DR) 288-Pin DDR4 UDIMM Features

**Table 2: Addressing**

Parameter	8GB
Row address	32K A[14:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	4Gb (512 Meg x 8), 16 banks
Module rank address	2 CS_n[1:0]

**Table 3: Part Numbers and Timing Parameters – 8GB Modules**

Base device: MT40A512M8,<sup>1</sup> 4Gb DDR4 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MTA16ATF1G64AZ-2G4__	8GB	1 Gig x 64	19.2 GB/s	0.83ns/2400 MT/s	16-16-16
MTA16ATF1G64AZ-2G1__	8GB	1 Gig x 64	17.0 GB/s	0.93ns/2133 MT/s	15-15-15
MTA16ATF1G64AZ-1G9__	8GB	1 Gig x 64	14.9 GB/s	1.07ns/1866 MT/s	13-13-13

- Notes:
1. The data sheet for the base device can be found on Micron's web site.
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA16ATF1G64AZ-2G1A1.



## 8GB (x64, DR) 288-Pin DDR4 UDIMM Pin Assignments

### Pin Assignments

Table 4: Pin Assignments

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V <sub>SS</sub>	73	V <sub>DD</sub>	109	V <sub>SS</sub>	145	NC	181	DQ29	217	V <sub>DD</sub>	253	DQ41
2	V <sub>SS</sub>	38	DQ24	74	CK0 <sub>t</sub>	110	DM5 <sub>n</sub> / DBI5 <sub>n</sub> , NC	146	V <sub>REFCA</sub>	182	V <sub>SS</sub>	218	CK1 <sub>t</sub>	254	V <sub>SS</sub>
3	DQ4	39	V <sub>SS</sub>	75	CK0 <sub>c</sub>	111	NC	147	V <sub>SS</sub>	183	DQ25	219	CK1 <sub>c</sub>	255	DQS5 <sub>c</sub>
4	V <sub>SS</sub>	40	DM3 <sub>n</sub> / DBI3 <sub>n</sub> , NC	76	V <sub>DD</sub>	112	V <sub>SS</sub>	148	DQ5	184	V <sub>SS</sub>	220	V <sub>DD</sub>	256	DQS5 <sub>t</sub>
5	DQ0	41	NC	77	V <sub>TT</sub>	113	DQ46	149	V <sub>SS</sub>	185	DQS3 <sub>c</sub>	221	V <sub>TT</sub>	257	V <sub>SS</sub>
6	V <sub>SS</sub>	42	V <sub>SS</sub>	78	EVENT <sub>n</sub> , NF	114	V <sub>SS</sub>	150	DQ1	186	DQS3 <sub>t</sub>	222	PARITY	258	DQ47
7	DM0 <sub>n</sub> / DBI0 <sub>n</sub> , NC	43	DQ30	79	A0	115	DQ42	151	V <sub>SS</sub>	187	V <sub>SS</sub>	223	V <sub>DD</sub>	259	V <sub>SS</sub>
8	NC	44	V <sub>SS</sub>	80	V <sub>DD</sub>	116	V <sub>SS</sub>	152	DQS0 <sub>c</sub>	188	DQ31	224	BA1	260	DQ43
9	V <sub>SS</sub>	45	DQ26	81	BA0	117	DQ52	153	DQS0 <sub>t</sub>	189	V <sub>SS</sub>	225	A10 <sub>AP</sub>	261	V <sub>SS</sub>
10	DQ6	46	V <sub>SS</sub>	82	RAS <sub>n</sub> / A16	118	V <sub>SS</sub>	154	V <sub>SS</sub>	190	DQ27	226	V <sub>DD</sub>	262	DQ53
11	V <sub>SS</sub>	47	CB4/ NC	83	V <sub>DD</sub>	119	DQ48	155	DQ7	191	V <sub>SS</sub>	227	NC	263	V <sub>SS</sub>
12	DQ2	48	V <sub>SS</sub>	84	CS0 <sub>n</sub>	120	V <sub>SS</sub>	156	V <sub>SS</sub>	192	CB5, NC	228	WE <sub>n</sub> / A14	264	DQ49
13	V <sub>SS</sub>	49	CB0/ NC	85	V <sub>DD</sub>	121	DM6 <sub>n</sub> / DBI6 <sub>n</sub> , NC	157	DQ3	193	V <sub>SS</sub>	229	V <sub>DD</sub>	265	V <sub>SS</sub>
14	DQ12	50	V <sub>SS</sub>	86	CAS <sub>n</sub> / A15	122	NC	158	V <sub>SS</sub>	194	CB1, NC	230	NC	266	DQS6 <sub>c</sub>
15	V <sub>SS</sub>	51	DM8 <sub>n</sub> / DBI8 <sub>n</sub> , NC	87	ODT0	123	V <sub>SS</sub>	159	DQ13	195	V <sub>SS</sub>	231	V <sub>DD</sub>	267	DQS6 <sub>t</sub>
16	DQ8	52	NC	88	V <sub>DD</sub>	124	DQ54	160	V <sub>SS</sub>	196	DQS8 <sub>c</sub>	232	A13	268	V <sub>SS</sub>
17	V <sub>SS</sub>	53	V <sub>SS</sub>	89	CS1 <sub>n</sub>	125	V <sub>SS</sub>	161	DQ9	197	DQS8 <sub>t</sub>	233	V <sub>DD</sub>	269	DQ55
18	DMI <sub>n</sub> / DBI1 <sub>n</sub> , NC	54	CB6/ DBI8 <sub>n</sub> , NC	90	V <sub>DD</sub>	126	DQ50	162	V <sub>SS</sub>	198	V <sub>SS</sub>	234	NC	270	V <sub>SS</sub>
19	NC	55	V <sub>SS</sub>	91	ODT1	127	V <sub>SS</sub>	163	DQS1 <sub>c</sub>	199	CB7, NC	235	NC	271	DQ51
20	V <sub>SS</sub>	56	CB2/ NC	92	V <sub>DD</sub>	128	DQ60	164	DQS1 <sub>t</sub>	200	V <sub>SS</sub>	236	V <sub>DD</sub>	272	V <sub>SS</sub>
21	DQ14	57	V <sub>SS</sub>	93	NC	129	V <sub>SS</sub>	165	V <sub>SS</sub>	201	CB3, NC	237	NC	273	DQ61
22	V <sub>SS</sub>	58	RESET <sub>n</sub>	94	V <sub>SS</sub>	130	DQ56	166	DQ15	202	V <sub>SS</sub>	238	SA2	274	V <sub>SS</sub>
23	DQ10	59	V <sub>DD</sub>	95	DQ36	131	V <sub>SS</sub>	167	V <sub>SS</sub>	203	CKE1	239	V <sub>SS</sub>	275	DQ57
24	V <sub>SS</sub>	60	CKE0	96	V <sub>SS</sub>	132	DM7 <sub>n</sub> / DBI7 <sub>n</sub> , NC	168	DQ11	204	V <sub>DD</sub>	240	DQ37	276	V <sub>SS</sub>
25	DQ20	61	V <sub>DD</sub>	97	DQ32	133	NC	169	V <sub>SS</sub>	205	NC	241	V <sub>SS</sub>	277	DQS7 <sub>c</sub>
26	V <sub>SS</sub>	62	ACT <sub>n</sub>	98	V <sub>SS</sub>	134	V <sub>SS</sub>	170	DQ21	206	V <sub>DD</sub>	242	DQ33	278	DQS7 <sub>t</sub>
27	DQ16	63	BG0	99	DM4 <sub>n</sub> / DBI4 <sub>n</sub> , NC	135	DQ62	171	V <sub>SS</sub>	207	BG1	243	V <sub>SS</sub>	279	V <sub>SS</sub>



## 8GB (x64, DR) 288-Pin DDR4 UDIMM Pin Assignments

**Table 4: Pin Assignments (Continued)**

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
28	V <sub>SS</sub>	64	V <sub>DD</sub>	100	NC	136	V <sub>SS</sub>	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DM2_n/ DBI2_n, NC	65	A12/BC_n	101	V <sub>SS</sub>	137	DQ58	173	V <sub>SS</sub>	209	V <sub>DD</sub>	245	DQS4_t	281	V <sub>SS</sub>
30	NC	66	A9	102	DQ38	138	V <sub>SS</sub>	174	DQS2_c	210	A11	246	V <sub>SS</sub>	282	DQ59
31	V <sub>SS</sub>	67	V <sub>DD</sub>	103	V <sub>SS</sub>	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V <sub>SS</sub>
32	DQ22	68	A8	104	DQ34	140	SA1	176	V <sub>SS</sub>	212	V <sub>DD</sub>	248	V <sub>SS</sub>	284	V <sub>DDSPD</sub>
33	V <sub>SS</sub>	69	A6	105	V <sub>SS</sub>	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V <sub>DD</sub>	106	DQ44	142	V <sub>PP</sub>	178	V <sub>SS</sub>	214	A4	250	V <sub>SS</sub>	286	V <sub>PP</sub>
35	V <sub>SS</sub>	71	A3	107	V <sub>SS</sub>	143	V <sub>PP</sub>	179	DQ19	215	V <sub>DD</sub>	251	DQ45	287	V <sub>PP</sub>
36	DQ28	72	A1	108	DQ40	144	NC	180	V <sub>SS</sub>	216	A2	252	V <sub>SS</sub>	288	V <sub>PP</sub>



## Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. See Functional Block Diagram for pins specific to this module.

**Table 5: Pin Descriptions**

Symbol	Type	Description
Ax	Input	<b>Address inputs:</b> Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	<b>Auto precharge:</b> A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	<b>Burst chop:</b> A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chopped.) See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	<b>Command input:</b> ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
Bx	Input	<b>Bank address inputs:</b> Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	<b>Bank group address inputs:</b> Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	<b>Chip ID:</b> These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	<b>Clock:</b> Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

**Table 5: Pin Descriptions (Continued)**

Symbol	Type	Description
CKEx	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After $V_{REFCA}$ has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CSx_n	Input	<b>Chip select:</b> All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. (CS2_n and CS3_n are not used on UDIMMs.)
ODTx	Input	<b>On-die termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT ( $R_{TT}$ ) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, $R_{TT}$ is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable $R_{TT}$ .
PARITY	Input	<b>Parity for command and address:</b> This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	<b>Command inputs:</b> RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	<b>Active LOW asynchronous reset:</b> Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAX	Input	<b>Serial address inputs:</b> Used to configure the temperature sensor/SPD EEPROM address range on the I <sup>2</sup> C bus.
SCL	Input	<b>Serial clock for temperature sensor/SPD EEPROM:</b> Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
DQx, CBx	I/O	<b>Data input/output and check bit input/output:</b> Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal $V_{REF}$ level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.

**Table 5: Pin Descriptions (Continued)**

Symbol	Type	Description
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIL_n)	I/O	<b>Input data mask and data bus inversion:</b> DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. (TDQS is not valid for UDIMMs.)
SDA	I/O	<b>Serial Data:</b> Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	<b>Data strobe:</b> Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	<b>Alert output:</b> Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V <sub>DD</sub> on DIMMs.
EVENT_n	Output	<b>Temperature event:</b> The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c  (x8 DRAM-based RDIMM only)	Output	<b>Termination data strobe:</b> When enabled via the mode register, the DRAM device enables the same R <sub>TT</sub> termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet. (TDQS_t and TDQS_c are not valid for UDIMMs.)
V <sub>DD</sub>	Supply	<b>Module power supply:</b> 1.21V (TYP).
V <sub>PP</sub>	Supply	<b>DRAM activating power supply:</b> 2.5V –0.125V / +0.250V.
V <sub>REPCA</sub>	Supply	Reference voltage for control, command, and address pins.
V <sub>SS</sub>	Supply	Ground.
V <sub>TT</sub>	Supply	Power supply for termination of address, command, and control V <sub>DD</sub> /2.
V <sub>DDSPD</sub>	Supply	Power supply used to power the I <sup>2</sup> C bus for SPD.
RFU	–	Reserved for future use.
NC	–	<b>No connect:</b> No internal electrical connection is present.



## 8GB (x64, DR) 288-Pin DDR4 UDIMM Pin Descriptions

**Table 5: Pin Descriptions (Continued)**

Symbol	Type	Description
NF	–	<b>No function:</b> May have internal connection present, but has no function.





## DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3	157	U2	0	11	168
	1	1	150		1	9	161
	2	2	12		2	10	23
	3	0	5		3	8	16
	4	7	155		4	15	166
	5	5	148		5	13	159
	6	6	10		6	14	21
	7	4	3		7	12	14
U3	0	19	179	U4	0	27	190
	1	17	172		1	25	183
	2	18	34		2	26	45
	3	16	27		3	24	38
	4	23	177		4	31	188
	5	21	170		5	29	181
	6	22	32		6	30	43
	7	20	25		7	28	36
U5	0	39	247	U6	0	47	258
	1	36	95		1	44	106
	2	38	102		2	46	113
	3	37	240		3	45	251
	4	34	104		4	42	115
	5	32	97		5	40	108
	6	35	249		6	43	260
	7	33	242		7	41	253
U7	0	55	269	U8	0	63	280
	1	52	117		1	60	106
	2	54	124		2	62	113
	3	53	262		3	61	251
	4	50	126		4	58	115
	5	48	119		5	56	108
	6	51	271		6	59	260
	7	49	264		7	57	253

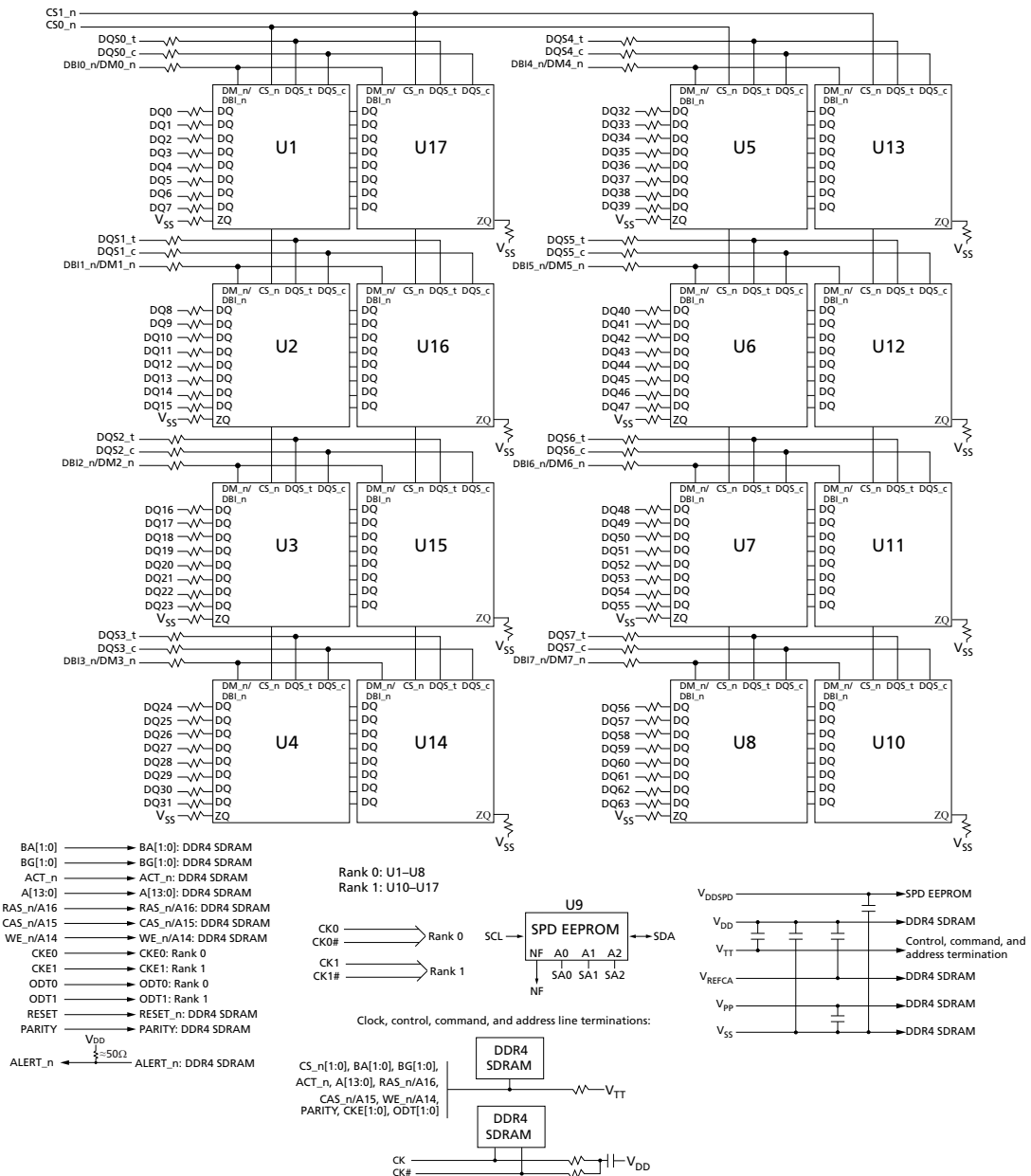


**Table 6: Component-to-Module DQ Map (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	60	128	U11	0	52	117
	1	63	280		1	55	269
	2	61	273		2	53	252
	3	62	135		3	54	124
	4	56	130		4	48	119
	5	58	137		5	50	126
	6	57	275		6	49	264
	7	59	282		7	51	271
U12	0	44	106	U13	0	36	95
	1	47	258		1	39	247
	2	45	251		2	37	240
	3	46	113		3	38	102
	4	40	108		4	32	97
	5	42	115		5	34	104
	6	41	253		6	33	242
	7	43	260		7	35	249
U14	0	25	183	U15	0	17	172
	1	27	190		1	19	179
	2	24	38		2	16	27
	3	26	45		3	18	34
	4	29	181		4	21	170
	5	31	188		5	23	177
	6	28	36		6	20	25
	7	30	43		7	22	32
U16	0	9	161	U17	0	1	150
	1	11	168		1	3	157
	2	8	16		2	0	5
	3	10	23		3	2	12
	4	13	159		4	5	148
	5	15	166		5	7	155
	6	12	14		6	4	3
	7	14	21		7	6	10

## Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

## General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single  $8n$ -bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS\_t and DQS\_c to capture data and CK\_t and CK\_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

## SPD EEPROM Operation

DDR4 SDRAM modules incorporate serial presence detect (SPD). The SPD data is stored in a 512-byte JEDEC JC-42.4-compliant EEPROM that is segregated into four 128-byte, write-protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module-specific parameters
2	256–319	100h–13Fh	Reserved; all bytes coded as 00h
	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I<sup>2</sup>C serial interface and is not integrated with the memory bus in any way. It operates as a slave device in the I<sup>2</sup>C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.2–3.6V.

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0–383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and unprotected.

## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 7: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units	Notes
V <sub>DD</sub>	V <sub>DD</sub> supply voltage relative to V <sub>SS</sub>	-0.4	1.5	V	1
V <sub>DDQ</sub>	V <sub>DDQ</sub> supply voltage relative to V <sub>SS</sub>	-0.4	1.5	V	1
V <sub>PP</sub>	Voltage on V <sub>PP</sub> pin relative to V <sub>SS</sub>	-0.4	3.0	V	2
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.4	1.5	V	

**Table 8: Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units	Notes
V <sub>DD</sub>	V <sub>DD</sub> supply voltage	1.14	1.2	1.26	V	1
V <sub>PP</sub>	DRAM activating power supply	2.375	2.5	2.75	V	2
V <sub>REFCA(DC)</sub>	Input reference voltage command/ address bus	0.49 × V <sub>DD</sub>	0.5 × V <sub>DD</sub>	0.51 × V <sub>DD</sub>	V	3
I <sub>VTT</sub>	Termination reference current from V <sub>TT</sub>	-750	-	750	mA	
V <sub>TT</sub>	Termination reference voltage (DC) – command/address bus	0.49 × V <sub>DD</sub> - 20mV	0.5 × V <sub>DD</sub>	0.51 × V <sub>DD</sub> + 20mV	V	4
I <sub>I</sub>	Input leakage current; any input excluding ZQ; 0V < V <sub>IN</sub> < 1.1V	-2.0	-	2.0	μA	5
I <sub>I/O</sub>	DQ leakage; 0V < V <sub>in</sub> < V <sub>DD</sub>	-4.0	-	4.0	μA	5
I <sub>I</sub>	Input leakage current; ZQ	-3.0	-	3.0	μA	5, 6
I <sub>OZpd</sub>	Output leakage current; V <sub>OUT</sub> = V <sub>DD</sub> ; DQ is disabled	-	-	5.0	μA	
I <sub>OZpu</sub>	Output leakage current; V <sub>OUT</sub> = V <sub>SS</sub> ; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	-	-	5.0	μA	
I <sub>VREFCA</sub>	V <sub>REFCA</sub> leakage; V <sub>REFCA</sub> = V <sub>DD</sub> /2 (after DRAM is ini- tialized)	-2.0	-	2.0	μA	5

- Notes:
1. V<sub>DDQ</sub> tracks with V<sub>DD</sub>; V<sub>DDQ</sub> and V<sub>DD</sub> are tied together.
  2. V<sub>PP</sub> must be greater than or equal to V<sub>DD</sub> at all times.
  3. V<sub>REFCA</sub> must not be greater than 0.6 × V<sub>DD</sub>. When V<sub>DD</sub> is less than 500mV, V<sub>REF</sub> may be less than or equal to 300mV.
  4. V<sub>TT</sub> termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
  5. Multiply by the number of DRAM die on the module.
  6. Tied to ground. Not connected to edge connector.



**Table 9: Thermal Characteristics**

Symbol	Parameter/Condition	Value	Units	Notes
$T_C$	Commercial operating case temperature	0 to 85	°C	1, 2, 3
$T_C$		>85 to 95	°C	1, 2, 3, 4
$T_{OPER}$	Normal operating temperature range	0 to 85	°C	5, 6
$T_{OPER}$	Extended temperature operating range (optional)	>85 to 95	°C	5, 6

- Notes:
1. Maximum operating case temperature;  $T_C$  is measured in the center of the package.
  2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum  $T_C$  during operation.
  3. Device functionality is not guaranteed if the DRAM device exceeds the maximum  $T_C$  during operation.
  4. If  $T_C$  exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
  5. The refresh rate must double when  $85^\circ\text{C} < T_{OPER} \leq 95^\circ\text{C}$ .
  6. For additional information, refer to technical note TN-00-08: "Thermal Applications" available on [micron.com](http://micron.com).



## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available on [micron.com](http://micron.com). Module speed grades correlate with component speed grades, as shown below.

**Table 10: Module and Component Speed Grades**

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G4	-083E
-2G1	-093E
-1G9	-107E

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.





## I<sub>DD</sub> Specifications

**Table 11: DDR4 I<sub>DD</sub> Specifications and Conditions – 8GB (Die Revision A)**

Values are for the MT40A512M8 DDR4 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	2400	2133	1866	Units
One bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub> <sup>1</sup>	768	720	704	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I <sub>pp</sub> current	I <sub>PP0</sub> <sup>1</sup>	56	56	56	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>DD1</sub> <sup>1</sup>	800	760	744	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	800	736	704	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	720	672	640	mA
Precharge power-down current	I <sub>DD2P</sub> <sup>2</sup>	512	480	480	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	656	624	624	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	1072	1008	976	mA
Active standby I <sub>pp</sub> current	I <sub>PP3N</sub> <sup>2</sup>	48	48	48	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	704	704	704	mA
Burst read current	I <sub>DD4R</sub> <sup>1</sup>	1536	1440	1360	mA
Burst read I <sub>DDQ</sub> current	I <sub>DDQ4R</sub> <sup>1</sup>	576	528	496	mA
Burst write current	I <sub>DD4W</sub> <sup>1</sup>	1696	1520	1392	mA
Burst refresh current (1x REF)	I <sub>DD5B</sub> <sup>1</sup>	1792	1760	1760	mA
Burst refresh I <sub>pp</sub> current (1x REF)	I <sub>PP5B</sub> <sup>1</sup>	200	200	200	mA
Self refresh current: Normal temperature range (0–85°C)	I <sub>DD6N</sub> <sup>2</sup>	320	320	320	mA
Self refresh current: Extended temperature range (0–95°C)	I <sub>DD6E</sub> <sup>2</sup>	432	432	432	mA
Self refresh current: Reduced temperature range (0–45°C)	I <sub>DD6R</sub> <sup>2</sup>	160	160	160	mA
Auto self refresh current (25°C)	I <sub>DD6A</sub> <sup>2</sup>	144	144	144	mA
Auto self refresh current (45°C)	I <sub>DD6A</sub> <sup>2</sup>	160	160	160	mA
Auto self refresh current (75°C)	I <sub>DD6A</sub> <sup>2</sup>	256	256	256	mA
Bank interleave read current	I <sub>DD7</sub> <sup>1</sup>	1936	1720	1520	mA
Bank interleave read I <sub>pp</sub> current	I <sub>PP7</sub> <sup>1</sup>	136	120	104	mA
Maximum power-down current	I <sub>DD8</sub> <sup>2</sup>	288	288	288	mA

- Notes: 1. One module rank in the active I<sub>DD/PP</sub>, the other rank in I<sub>DD2P/PP3N</sub>.  
2. All ranks in this I<sub>DD/PP</sub> condition.

## SPD EEPROM Operating Conditions

For the latest SPD data, refer to Micron's SPD page: [micron.com/spd](http://micron.com/spd).

**Table 12: SPD EEPROM DC Operating Conditions**

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	$V_{DDSPD}$	2.2	3.6	V
Input low voltage: logic 0; all inputs	$V_{IL}$	-0.5	$V_{DDSPD} \times 0.3$	V
Input high voltage: logic 1; all inputs	$V_{IH}$	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 0.5$	V
Output low voltage: 3mA sink current $V_{DDSPD} > 2V$	$V_{OL}$	-	0.4	V
Input leakage current: (SCL, SDA) $V_{IN} = V_{DDSPD}$ or $V_{SSSPD}$	$I_{LI}$	-	$\pm 5$	$\mu A$
Output leakage current: $V_{OUT} = V_{DDSPD}$ or $V_{SSSPD}$ , SDA in High-Z	$I_{LO}$	-	$\pm 5$	$\mu A$

- Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
  2. All voltages referenced to  $V_{DDSPD}$ .

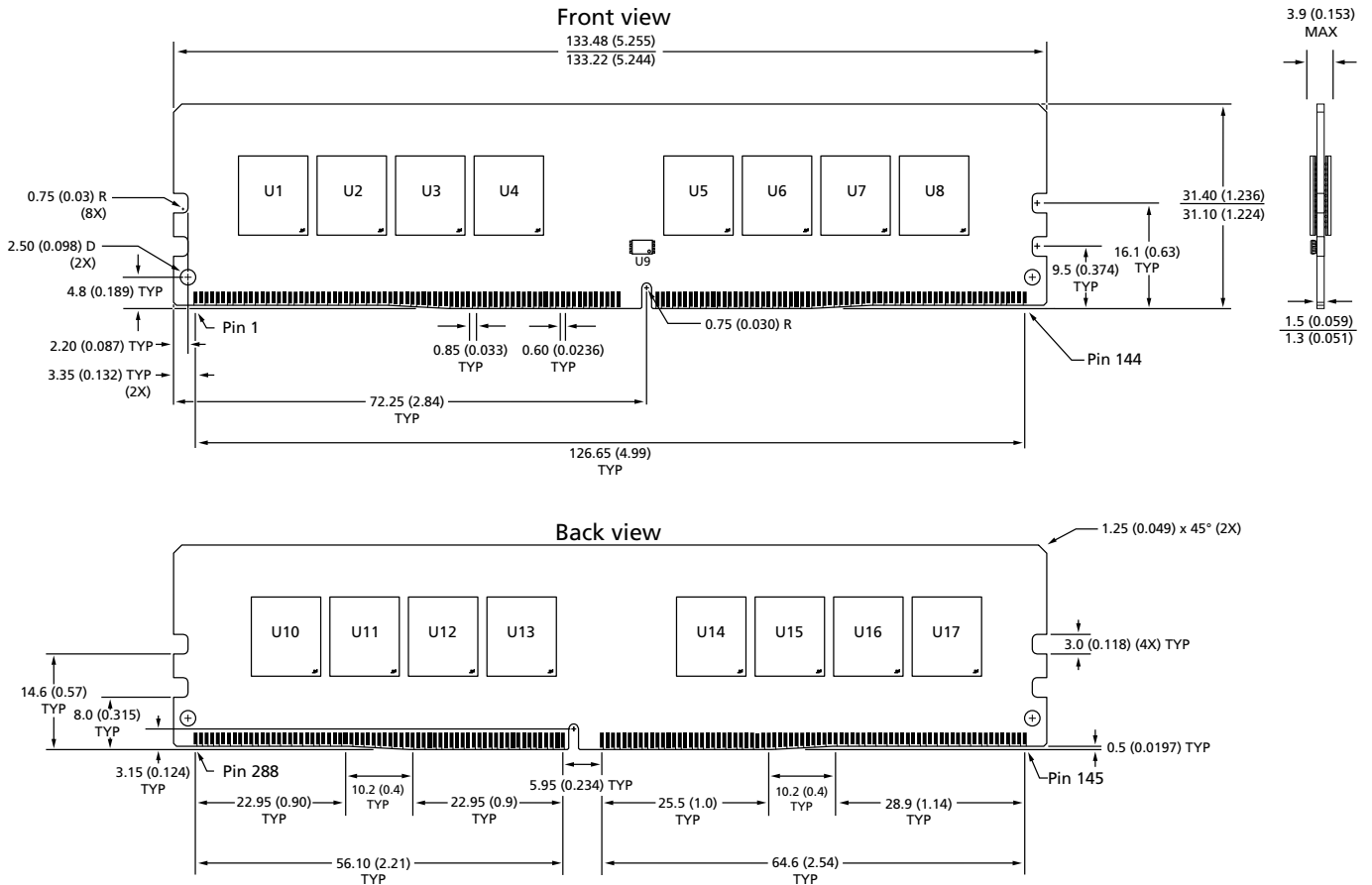
**Table 13: SPD EEPROM AC Operating Conditions**

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	$t_{SCL}$	10	1000	kHz
Clock pulse width HIGH time	$t_{HIGH}$	260	-	ns
Clock pulse width LOW time	$t_{LOW}$	500	-	ns
Detect clock LOW timeout	$t_{TIMEOUT}$	25	35	ms
SDA rise time	$t_R$	-	120	ns
SDA fall time	$t_F$	-	120	ns
Data-in setup time	$t_{SU:DAT}$	50	-	ns
Data-in hold time	$t_{HD:DI}$	0	-	ns
Data out hold time	$t_{HD:DAT}$	0	350	ns
Start condition setup time	$t_{SU:STA}$	260	-	ns
Start condition hold time	$t_{HD:STA}$	260	-	ns
Stop condition setup time	$t_{SU:STO}$	260	-	ns
Time the bus must be free before a new transition can start	$t_{BUF}$	500	-	ns
Write time	$t_W$	-	5	ms
Warm power cycle time off	$t_{POFF}$	1	-	ms
Time from power on to first command	$t_{INIT}$	10	-	ms

- Note:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

## Module Dimensions

Figure 3: 288-Pin DDR4 UDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
2. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.