SDRAM Unbuffered DIMM (UDIMM)

MT4LSDT464A – 32MB

MT4LSDT864A(I) – 64MB

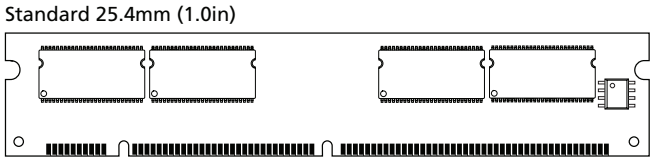
MT4LSDT1664A(I) – 128MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 168-pin, dual in-line memory module (DIMM)
- PC100- and PC133-compliant
- Unbuffered
- 32MB (4 Meg x 64)[2], 64MB (8 Meg x 64), 128MB (16 Meg x 64)
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes CONCURRENT AUTO PRECHARGE and auto refresh modes
- Self refresh mode: 64ms, 4,096-cycle refresh for 32MB and 64MB; 64ms, 8,192-cycle refresh for 128MB
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Gold edge contacts

Figure 1: 168-Pin DIMM (MO-161)



Options	Marking
• Package	
– 168-pin DIMM (standard)	G
– 168-pin DIMM (Pb-free)	Y
• Operating temperature range	
– Commercial (0°C to +65°C)	None
– Industrial (–40°C to +85°C)[1, 3]	I
• Frequency/CAS Latency	
– 7.5ns (133 MHz)/CL = 2	-13E
– 7.5ns (133 MHz)/CL = 3	-133
– 8ns (100 MHz)/CL = 2[2]	-10E
• PCB	
– Standard 25.40mm (1.0in)	

Notes: 1. Contact Micron for product availability.
2. Not recommended for new designs.
3. Industrial temperature option available in -133 MHz only.

Table 1: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Industry Nomenclature	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-13E	PC133	5.4ns	–	-13E	133 MHz
-133	PC133	–	5.4ns	-133	133 MHz
-10E[2]	PC100	9ns	7.5ns	-10E	100 MHz

Table 2: Addressing

	32MB	64MB	128MB
Refresh count	4K	4K	8K
Device banks	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	64Mb (4 Meg x 16)	128Mb (8 Meg x 16)	256Mb (16 Meg x 16)
Row addressing	4K (A0–A11)	4K (A0–A11)	8K (A0–A12)
Column addressing	256 (A0–A7)	512 (A0–A8)	512 (A0–A8)
Module ranks	1 (S0#, S2#)	1 (S0#, S2#)	1 (S0#, S2#)

Table 3: Part Numbers and Timing Parameters

Part Number[3]	Module Density	Configuration	System Bus Speed
MT4LSDT464AG-13E_[1]	32MB	4 Meg x 64	133 MHz
MT4LSDT464AY-13E_[2]	32MB	4 Meg x 64	133 MHz
MT4LSDT464AG-133_[2]	32MB	4 Meg x 64	133 MHz
MT4LSDT464AY-133_[2]	32MB	4 Meg x 64	133 MHz
MT4LSDT464AG-10E_[2]	32MB	4 Meg x 64	100 MHz
MT4LSDT464AY-10E_[1]	32MB	4 Meg x 64	100 MHz
MT4LSDT864AG-13E_[1]	64MB	8 Meg x 64	133 MHz
MT4LSDT864AY-13E_	64MB	8 Meg x 64	133 MHz
MT4LSDT864AIG-133_[1]	64MB	8 Meg x 64	133 MHz
MT4LSDT864AG-133_[1]	64MB	8 Meg x 64	133 MHz
MT4LSDT864AIY-133_[1]	64MB	8 Meg x 64	133 MHz
MT4LSDT864AY-133_	64MB	8 Meg x 64	133 MHz
MT4LSDT864AG-10E_[2]	64MB	8 Meg x 64	100 MHz
MT4LSDT864AY-10E_[1]	64MB	8 Meg x 64	100 MHz
MT4LSDT1664AG-13E_	128MB	16 Meg x 64	133 MHz
MT4LSDT1664AY-13E_	128MB	16 Meg x 64	133 MHz
MT4LSDT1664AIG-133_[1]	128MB	16 Meg x 64	133 MHz
MT4LSDT1664AG-133_	128MB	16 Meg x 64	133 MHz
MT4LSDT1664AIY-133_[1]	128MB	16 Meg x 64	133 MHz
MT4LSDT1664AY-133_	128MB	16 Meg x 64	133 MHz
MT4LSDT1664AG-10E_[2]	128MB	16 Meg x 64	100 MHz
MT4LSDT1664AY-10E_[2]	128MB	16 Meg x 64	100 MHz

Notes:
1. Contact Micron for product availability.
2. Not recommended for new designs.
3. The designators for component and PCB revision are the last two characters of each part number. Consult factory for current revision codes. Example: MT4LSDT464AG-133G1

Pin Assignments and Descriptions

Table 4: Pin Assignments

168-Pin DIMM Front								168-Pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	22	DNU	43	VSS	64	VSS	85	VSS	106	DNU	127	VSS	148	VSS
2	DQ0	23	VSS	44	NC	65	DQ21	86	DQ32	107	VSS	128	CKE0	149	DQ53
3	DQ1	24	NC	45	S2#	66	DQ22	87	DQ33	108	NC	129	DNU	150	DQ54
4	DQ2	25	NC	46	DQM2	67	DQ23	88	DQ34	109	NC	130	DQM6	151	DQ55
5	DQ3	26	VDD	47	DQM3	68	VSS	89	DQ35	110	VDD	131	DQM7	152	VSS
6	VDD	27	WE#	48	NC	69	DQ24	90	VDD	111	CAS#	132	DNU	153	DQ56
7	DQ4	28	DQM0	49	VDD	70	DQ25	91	DQ36	112	DQM4	133	VDD	154	DQ57
8	DQ5	29	DQM1	50	NC	71	DQ26	92	DQ37	113	DQM5	134	NC	155	DQ58
9	DQ6	30	S0#	51	NC	72	DQ27	93	DQ38	114	DNU	135	NC	156	DQ59
10	DQ7	31	NC	52	DNU	73	VDD	94	DQ39	115	RAS#	136	DNU	157	VDD
11	DQ8	32	VSS	53	DNU	74	DQ28	95	DQ40	116	VSS	137	DNU	158	DQ60
12	VSS	33	A0	54	VSS	75	DQ29	96	VSS	117	A1	138	VSS	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	VSS	99	DQ43	120	A7	141	DQ50	162	VSS
16	DQ12	37	A8	58	DQ19	79	CK2	100	DQ44	121	A9	142	DQ51	163	DNU
17	DQ13	38	A10	59	VDD	80	NC	101	DQ45	122	BA0	143	VDD	164	NC
18	VDD	39	BA1	60	DQ20	81	NC	102	VDD	123	A11	144	DQ52	165	SA0
19	DQ14	40	VDD	61	NC	82	SDA	103	DQ46	124	VDD	145	NC	166	SA1
20	DQ15	41	VDD	62	NC	83	SCL	104	DQ47	125	DNU	146	NC	167	SA2
21	DNU	42	CK0	63	NC	84	VDD	105	DNU	126	NC/A12[1]	147	NC	168	VDD

Notes: 1. Pin 126 is NC for 32MB and 64MB modules, or A12 for the 128MB module.

Figure 2: Pin Locations (168-Pin DIMM)

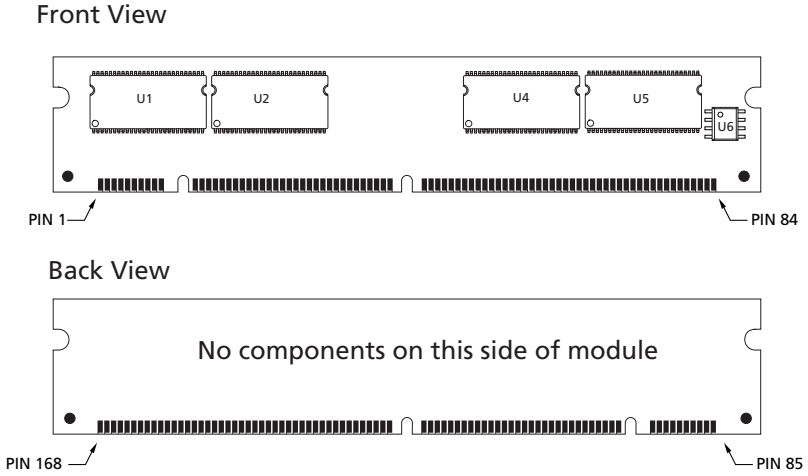


Table 5: Pin Descriptions

Pins may not correlate with symbols; refer to Table 4 on page 3 for more information

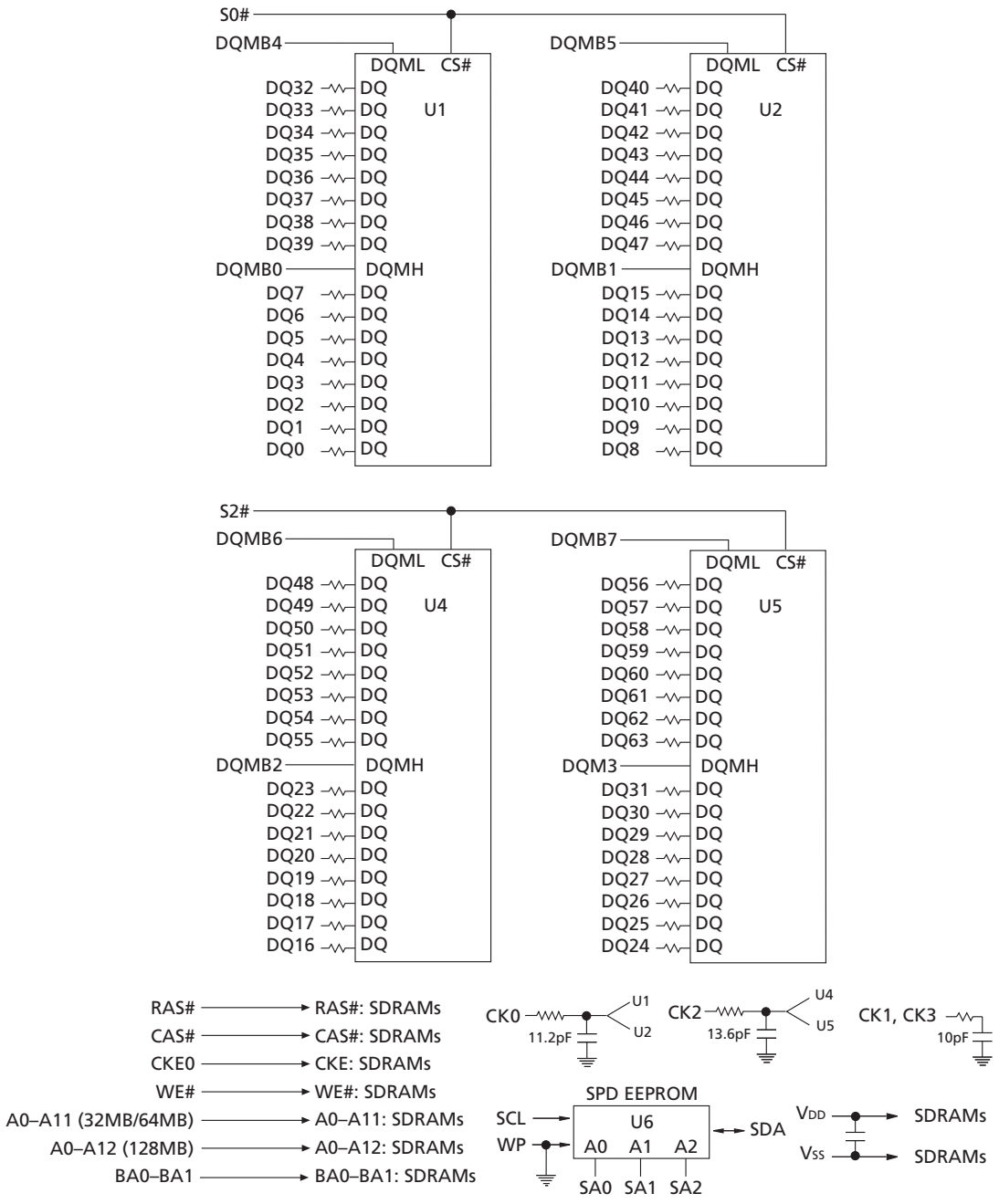
Pin Numbers	Symbol	Type	Description
27, 111, 115	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
42, 79	CK0, CK2	Input	**Clock:** CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
128	CKE0	Input	**Clock enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle) or CLOCK SUSPEND OPERATION (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
30, 45	S0#, S2#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
28, 29, 46, 47, 112, 113, 130, 131	DQMB0–DQMB7	Input	**Input/output mask:** DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	**Bank address:** BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
33–38, 117–121, 123, 126 (128MB)	A0–A11 (32MB, 64MB) A0–A12 (128MB)	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.
83	SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
165–167	SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
82	SDA	Input/Output	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
2–5, 7–11, 13–17, 19–20, 55–58, 60, 65–67, 69–72, 74–77, 86–89, 91–95, 97–101, 103–104, 139–142, 144, 149–151, 153–156, 158–161	DQ0–DQ63	Input/Output	**Data I/Os:** Data bus.

Table 5: Pin Descriptions (Continued)
Pins may not correlate with symbols; refer to Table 4 on page 3 for more information

Pin Numbers	Symbol	Type	Description
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	VDD	Supply	**Power supply:** +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	VSS	Supply	**Ground.**
21, 22, 52, 53, 105, 106, 114, 125, 129, 132, 163	DNU	–	**Do not use:** These pins are not used on these modules, but are assigned pins on other modules in this product family.
24, 25, 31, 44, 48, 50, 51, 61, 62, 63, 80, 81, 108, 109, 126 (32MB, 64MB), 134, 135, 145–147, 164	NC	–	**Not connected:** These pins are not connected on these modules.

Functional Block Diagram

Figure 3: Functional Block Diagram



Notes:
1. All resistor values are 10Ω unless otherwise specified.
2. Per industry standard, Micron modules use various component speed grades as referenced in the module part numbering guide found on Micron's Web site: www.micron.com/support.
3. Standard modules use the following SDRAM devices: MT48LC4M16A2TG(IT) (32MB); MT48LC8M16A2TG(IT) (64MB); MT48LC16M16A2TG(IT) (128MB).
4. Pb-free modules use the following SDRAM devices: MT48LC4M16A2P(IT) (32MB); MT48LC8M16A2P(IT) (64MB); MT48LC16M16A2P(IT) (128MB).

General Description

The Micron MT4LSDT464A, MT4LSDT864A(I), and MT4LSDT1664A(I) are high-speed CMOS, dynamic random access, 32MB, 64MB, and 128MB memory modules organized in a x64 configuration. These modules use SDRAM devices which are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0–A11 for 32MB and 64MB; A0–A12 for 128MB select the device row). The address bits registered coincident with the READ or WRITE command (A0–A7 for 32MB; A0–A8 for 64MB and 128MB) are used to select the starting device column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the PRECHARGE cycles and provide seamless, high-speed, random access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs, and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheets.

Serial Presence-Detect Operation

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is

defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode, and a write burst mode, as shown in Figure 4 on page 10. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. For the 128MB module, address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4 on page 10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 6 on page 11. The block is uniquely selected by A1–A*i* when BL = 2, A2–A*i* when BL = 4, and A3–A*i* when BL = 8. See note 8 of Table 6 on page 11 for A*i* values. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in Table 6 on page 11.

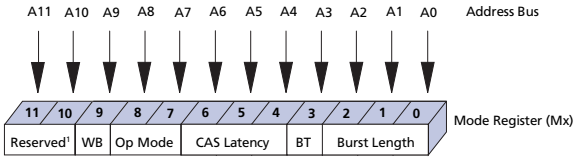
Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

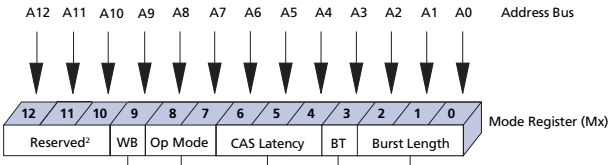
The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 6 on page 11.

Figure 4: Mode Register Definition Diagram

32MB and 64MB Modules



128MB Module



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6–M0	Operating Mode
0	0	Defined	Standard operation
–	–	–	All other states reserved

M9	Write Burst Mode
0	Programmed BL
1	Single location access

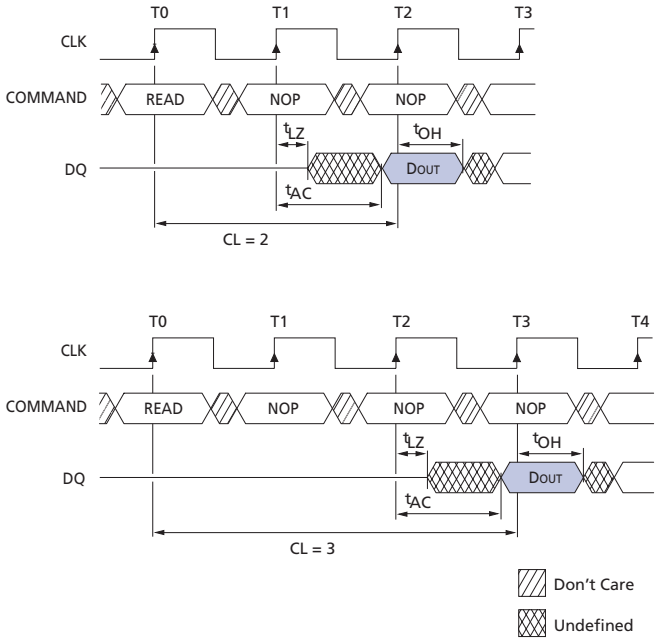
Notes:
1. M11 and M10 should be programmed = “0, 0” to ensure compatibility with future devices.
2. M12, M11, and M10 should be programmed = “0, 0, 0” to ensure compatibility with future devices.

Table 6: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-4-5-6-7-0-1-2
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page (y)	n = A0–A*i* (location 0–*y)*			Cn, Cn + 1, Cn + 2, Cn + 3, Cn + 4. . . Cn - 1, Cn . . .	Not supported

Notes:
1. For full-page accesses: *y* = 256 (32MB); *y* = 512 (64MB/128MB).
2. For BL = 2, A1–A*i* select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A*i* select the block-of-four burst; A0–A1 select the starting column within the block.
4. For BL = 8, A3–A*i* select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A*i* select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, A0–A*i* select the unique column to be accessed, and mode register bit M3 is ignored.
8. *i* = 7 for 32MB; *i* = 8 for 64MB and 128MB.

Figure 5: CAS Latency Diagram



CAS Latency (CL)

CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQ will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 5. Table 7 on page 13 indicates the operating frequencies at which each CL setting can be used.

Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Table 7: CAS Latency Table

Speed	Allowable Operating Clock Frequency (MHz)	
	CL = 2	CL = 3
-13E	≤133	≤143
-133	≤100	≤133
-10E	≤100	n/a

Commands

This truth table provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheet.

Table 8: Truth Table – Commands and DQMB Operation

Notes appear below; CKE is HIGH for all commands shown except SELF REFRESH

Name (Function)	CS#	RAS#	CAS#	WE#	DQMB	Address	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	1
READ (select bank and column, and start READ burst)	L	H	L	H	L/H[7]	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H[7]	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	X	Code	X	4
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	5, 6
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	1
Write enable/output enable	–	–	–	–	L	–	Active	7
Write inhibit/output High-Z	–	–	–	–	H	–	High-Z	7

Notes:
1. A0–A11 define the op-code written to the mode register, and for the 128MB module, A12 should be driven LOW.
2. A0–A11 (32MB and 64MB) or A0–A12 (128MB) provide device row address, and BA0, BA1 determine which device bank is made active.
3. A0–A7 (32MB) or A0–A8 (64MB and 128MB) provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent) while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
4. A10 LOW: BA0, BA1 determine the device bank being precharged. A10 HIGH: All device banks precharged and BA0, BA1 are "Don't Care."
5. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
6. Internal refresh counter controls device row addressing; all inputs and I/Os are "Don't Care" except for CKE.
7. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Voltage on V_{DD}, $V_{DD}Q$ supply relative to V_{SS}		–1.0	+4.6	V
Voltage on inputs, NC or I/O pins relative to V_{SS}		–1.0	+4.6	V
Operating temperature T_{OPR} (commercial - ambient)		0	+65	°C
Operating temperature T_{OPR} (industrial - ambient)		–40	+85	°C
Storage temperature (plastic)		–55	+150	°C

Capacitance

Table 10: Capacitance
Notes 1, 2; notes appear on page 20

Parameter	Symbol	Min	Max	Units
Input capacitance: Address and command	C_{I1}	10	15.2	pF
Input capacitance: S#	C_{I2}	5	7.6	pF
Input capacitance: CK0	C_{I3_a}	16.2	18.2	pF
Input capacitance: CK2	C_{I3_b}	18.6	20.6	pF
Input capacitance: DQMB	C_{I4}	2.5	3.8	pF
Input/output capacitance: DQ	C_{IO}	4	6	pF

Timing and Operating Conditions

Table 11: AC Functional Characteristics
Notes: 5, 6, 8, 9, 11, 31; notes appear on page 20

Parameter	Symbol	-13E	-133	-10E	Units	Notes
READ/WRITE command to READ/WRITE command	^{t}CCD	1	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode	$^{t}CKED$	1	1	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode	^{t}PED	1	1	1	^{t}CK	14
DQM to input data delay	^{t}DQD	0	0	0	^{t}CK	17
DQM to data mask during WRITEs	^{t}DQM	0	0	0	^{t}CK	17
DQM to data high-impedance during READs	^{t}DQZ	2	2	2	^{t}CK	17
WRITE command to input data delay	^{t}DWD	0	0	0	^{t}CK	17
Data-in to ACTIVE command	^{t}DAL	4	5	4	^{t}CK	15, 21
Data-in to PRECHARGE command	^{t}DPL	2	2	2	^{t}CK	16, 21
Last data-in to burst STOP command	^{t}BDL	1	1	1	^{t}CK	17
Last data-in to new READ/WRITE command	^{t}CDL	1	1	1	^{t}CK	17
Last data-in to PRECHARGE command	^{t}RDL	2	2	2	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command	^{t}MRD	2	2	2	^{t}CK	26

Table 11: AC Functional Characteristics (Continued)
Notes: 5, 6, 8, 9, 11, 31; notes appear on page 20

Parameter		Symbol	-13E	-133	-10E	Units	Notes
Data-out to high-impedance from PRECHARGE command	CL = 3	tROH(3)	3	3	3	tCK	17
	CL = 2	tROH(2)	2	2	2	tCK	17

Table 12: Electrical Characteristics and Recommended AC Operating Conditions
Notes: 5, 6, 8, 9, 11, 31; notes appear on page 20; VDD, VDDQ = +3.3V ±0.3V

AC Characteristics			-13E		-133		-10E			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Access time from CLK (positive edge)	CL = 3	tAC(3)	–	5.4	–	5.4	–	–	ns	27
	CL = 2	tAC(2)	–	5.4	–	6	–	6	ns	
Address hold time		tAH	0.8	–	0.8	–	1	–	ns	
Address setup time		tAS	1.5	–	1.5	–	2	–	ns	
CLK high-level width		tCH	2.5	–	2.5	–	3	–	ns	
CLK low-level width		tCL	2.5	–	2.5	–	3	–	ns	
Clock cycle time	CL = 3	tCK(3)	7	–	7.5	–	8	–	ns	23
	CL = 2	tCK(2)	7.5	–	10	–	10	–	ns	23
CKE hold time		tCKH	0.8	–	0.8	–	1	–	ns	
CKE setup time		tCKS	1.5	–	1.5	–	2	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	0.8	–	0.8	–	1	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	1.5	–	1.5	–	2	–	ns	
Data-in hold time		tDH	0.8	–	0.8	–	1	–	ns	
Data-in setup time		tDS	1.5	–	1.5	–	2	–	ns	
Data-out high-impedance time	CL = 3	tHZ(3)	–	5.4	–	5.4	–	6	ns	10
	CL = 2	tHZ(2)	–	5.4	–	6	–	6	ns	10
Data-out low-impedance time		tLZ	1	–	1	–	1	–	ns	
Data-out hold time (load)		tOH	3	–	3	–	3	–	ns	
Data-out hold time (no load)		tOHN	1.8	–	1.8	–	1.8	–	ns	28
ACTIVE to PRECHARGE command		tRAS	37	120,000	44	120,000	50	120,000	ns	32
ACTIVE to ACTIVE command period		tRC	60	–	66	–	70	–	ns	
ACTIVE to READ or WRITE delay		tRCD	15	–	20	–	20	–	ns	
Refresh period (8,192 rows)		tREF	–	64	–	64	–	64	ms	
AUTO REFRESH period		tRFC	66	–	66	–	70	–	ns	
PRECHARGE command period		tRP	15	–	20	–	20	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		tRRD	14	–	15	–	20	–	ns	
Transition time		tT	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		tWR	1 CLK + 7ns	–	1 CLK + 7.5ns	–	1 CLK + 7ns	–	ns	24
			14	–	15	–	15	–	ns	25
Exit SELF REFRESH to ACTIVE command		tXSR	67	–	75	–	80	–	ns	20

Table 13: DC Electrical Characteristics and Operating Conditions

Notes: 1, 5, 6; notes appear on page 20; V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V_{DD}, $V_{DD}Q$	3	3.6	V	
Input high voltage: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
Input low voltage: Logic 0; All inputs	V_{IL}	–0.3	0.8	V	22
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (all other pins not under test = 0V)	I_I	–20	20	µA	33
		–10	10		
		–5	5		
Output leakage current: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	–5	5	µA	33
Output levels: Output high voltage (I_{OUT} = –4mA)	V_{OH}	2.4	–	V	
Output low voltage: (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

IDD Specifications

Table 14: IDD Specifications and Conditions – 32MB

Notes: 1, 5, 6, 11, 13; notes appear on page 20; VDD, VDDQ = +3.3V ±0.3V; DRAM components only

Parameter/Condition		Symbol	Max			Units	Notes
			-13E	-133	-10E		
Operating current: Active mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		IDD1	500	460	380	mA	3, 18, 19, 29
Standby current: Power-down mode; All device banks idle; CKE = LOW		IDD2	8	8	8	mA	29
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD met; No accesses in progress		IDD3	180	180	140	mA	3, 12, 19, 29
Operating current: Burst mode; Continuous burst; READ or WRITE; All device banks active		IDD4	600	560	480	mA	3, 18, 19, 29
Auto refresh current: CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5	920	840	760	mA	3, 12, 18, 19, 29, 30
	^{t}RFC = 15.62µs	IDD6	12	12	12	mA	
Self refresh current: CKE ≤ 0.2V		IDD7	4	4	4	mA	4

Table 15: IDD Specifications and Conditions – 64MB

Notes: 1, 5, 6, 11, 13; notes appear on page 20; VDD, VDDQ = +3.3V ±0.3V; DRAM components only

Parameter/Condition		Symbol	Max			Units	Notes
			-13E	-133	-10E		
Operating current: Active mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		IDD1	640	600	560	mA	3, 18, 19, 29
Standby current: Power-down mode; All device banks idle; CKE = LOW		IDD2	8	8	8	mA	29
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD met; No accesses in progress		IDD3	200	200	160	mA	3, 12, 19, 29
Operating current: Burst mode; Continuous burst; READ or WRITE; All device banks active		IDD4	660	600	560	mA	3, 18, 19, 29
Auto refresh current: CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5	1,320	1,240	1,080	mA	3, 12, 18, 19, 29, 30
	^{t}RFC = 15.62µs	IDD6	12	12	12	mA	
Self refresh current: CKE ≤ 0.2V		IDD7	8	8	8	mA	4

Table 16: IDD Specifications and Conditions – 128MB

Notes: 1, 5, 6, 11, 13; notes appear on page 20; VDD, VDDQ = +3.3V ±0.3V; DRAM components only

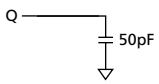
Parameter/Condition	Symbol	Max			Units	Notes
		-13E	-133	-10E		
Operating current: Active mode; burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)	IDD1	540	500	500	mA	3, 18, 19, 29
Standby current: Power-down mode; All device banks idle; CKE = LOW	IDD2	8	8	8	mA	29
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD met; No accesses in progress	IDD3	160	160	160	mA	3, 12, 19, 29
Operating current: Burst mode; Continuous burst; READ or WRITE; All device banks active	IDD4	540	540	540	mA	3, 18, 19, 29

Table 16: IDD Specifications and Conditions – 128MB (Continued)
Notes: 1, 5, 6, 11, 13; notes appear on page 20; VDD, VDDQ = +3.3V ±0.3V; DRAM components only

Parameter/Condition		Symbol	Max			Units	Notes
			-13E	-133	-10E		
Auto refresh current: CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5	1,140	1,080	1,080	mA	3, 12, 18, 19, 29, 30
	^{t}RFC = 7.81µs	IDD6	14	14	14	mA	
Self refresh current: CKE ≤ 0.2V		IDD7	10	10	10	mA	4

Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz; T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ T_A ≤ +70°C for commercial, –40°C ≤ T_A ≤ +85°C for industrial).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated anytime the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the ISV crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 10ns for -10E; ^{t}CK = 7.5ns for -133 and -13E.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤3ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –2V for a pulse width ≤3ns.

23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7ns for -13E; 7.5ns for -133; and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^{t}AC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For -13E, CL = 2 and ^{t}CK = 7.5ns; for -133, CL = 3 and ^{t}CK = 7.5ns; for -10E, CL = 2 and ^{t}CK = 10ns.
30. CKE is HIGH during refresh command period ^{t}RFC (MIN), else CKE is LOW. The IDD6 limit is actually a nominal value and does not result in a fail value.
31. Refer to device data sheet for timing waveforms.
32. The value of ^{t}RAS used in -13E speed grade modules is calculated from ^{t}RC - ^{t}RP.
33. Leakage number reflects the worst-case leakage possible through the module pin, not what each memory device contributes.

Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions, as indicated in Figure 6 on page 22 and Figure 7 on page 23.

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data, as indicated in Figure 8 on page 23.

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode, the SPD device will transmit eight bits of data, release the SDA line, and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 6: Data Validity

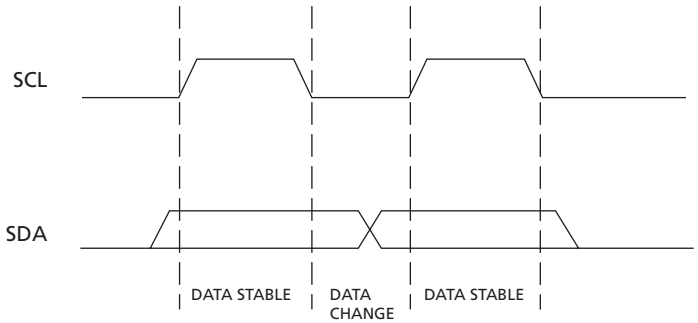


Figure 7: Definition of Start and Stop

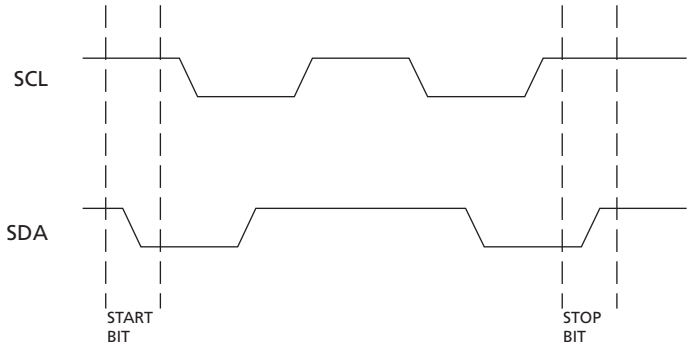


Figure 8: Acknowledge Response from Receiver

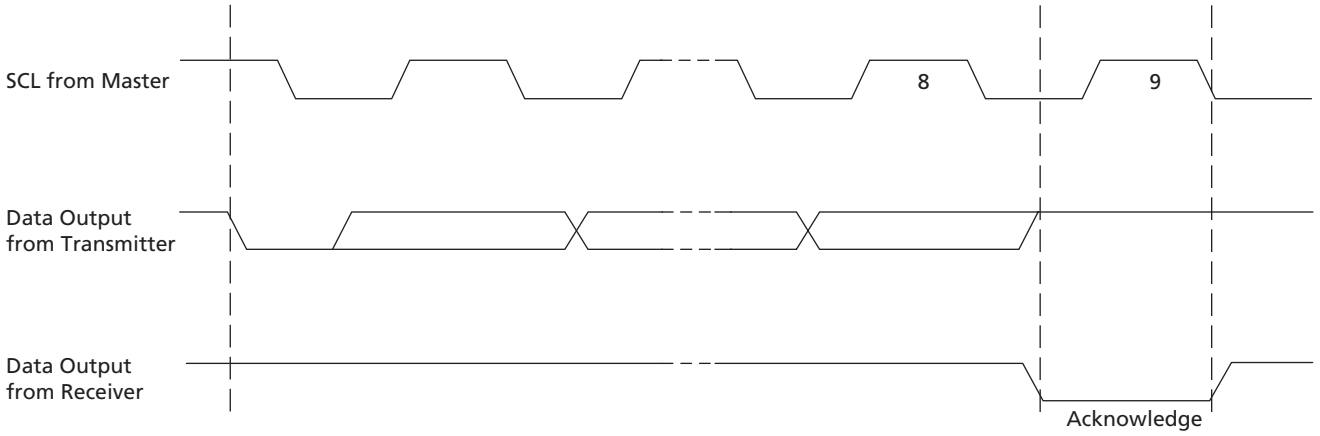


Table 17: EEPROM Device Select Code

The most significant bit (b7) is sent first

	Device Type Identifier				Chip Enable			RW#
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW#
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW#

Table 18: EEPROM Operating Modes

Mode	RW# Bit	W#C	Bytes	Initial Sequence
Current address read	1	VIH or VIL	1	Start, device select, RW# = '1'
Random address read	0	VIH or VIL	1	Start, device select, RW# = '0', address
	1	VIH or VIL	1	Restart, device select, RW# = '1'
Sequential read	1	VIH or VIL	≥1	Similar to current or random address read
Byte write	0	VIL	1	Start, device select, RW# = '0'
Page write	0	VIL	≤16	Start, device select, RW# = '0'

Figure 9: SPD EEPROM Timing Diagram

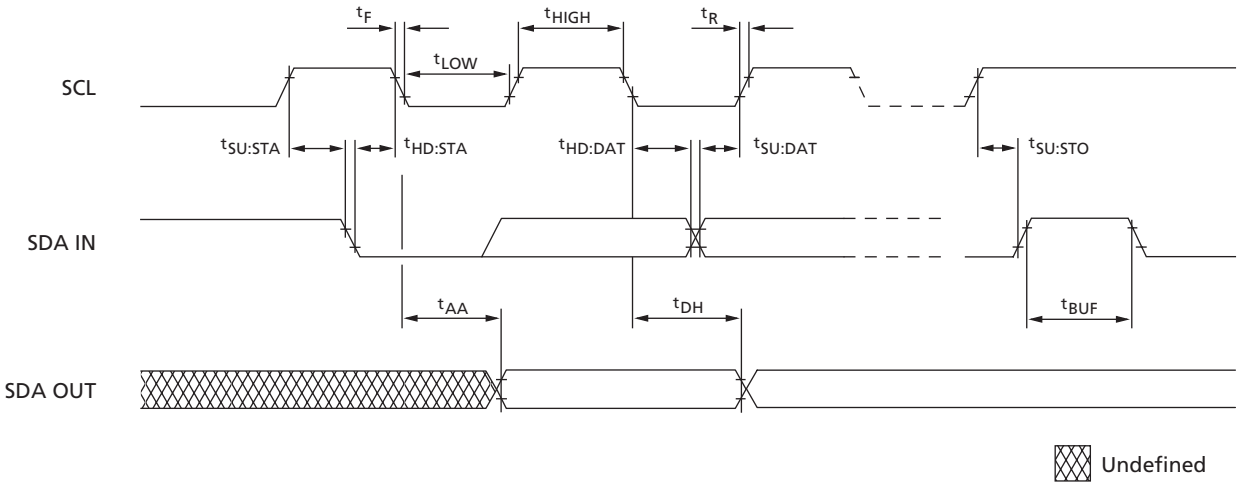


Table 19: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DD}	3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–1	V_{DD} x 0.3	V
Output low voltage: I_{OUTL} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V ±10%	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

Table 20: Serial Presence-Detect EEPROM AC Operating Conditions
Notes appear below; All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t_{AA}	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	t_{BUF}	1.3	–	µs	
Data-out hold time	t_{DH}	200	–	ns	
SDA and SCL fall time	t_F	–	300	ns	2
Data-in hold time	$t_{HD:DAT}$	0	–	µs	
Start condition hold time	$t_{HD:STA}$	0.6	–	µs	
Clock HIGH period	t_{HIGH}	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	t_I	–	50	ns	
Clock LOW period	t_{LOW}	1.3	–	µs	
SDA and SCL rise time	t_R	–	0.3	µs	2
SCL clock frequency	f_{SCL}	–	400	KHz	
Data-in setup time	$t_{SU:DAT}$	100	–	ns	
Start condition setup time	$t_{SU:STA}$	0.6	–	µs	3
Stop condition setup time	$t_{SU:STO}$	0.6	–	µs	

Table 20: Serial Presence-Detect EEPROM AC Operating Conditions (Continued)
Notes appear below; All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 21: Serial Presence-Detect Matrix

"1"/"0": Serial data, "driven to HIGH"/"driven to LOW."

Byte	Description	Entry (Version)	32MB	64MB	128MB
0	Number of bytes used by Micron	128	80	80	80
1	Total number of SPD memory bytes	256	08	08	08
2	Memory type	SDRAM	04	04	04
3	Number of row addresses	12 or 13	0C	0C	0D
4	Number of column addresses	8 or 9	08	09	09
5	Number of banks	1	01	01	01
6	Module data width	64	40	40	40
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	LVTTL	01	01	01
9	SDRAM cycle time, ^{t}CK (CL = 3)	7ns (-13E) 7.5ns (-133) 8ns (-10E)	70 75 80	70 75 80	70 75 80
10	SDRAM access from clock, ^{t}AC (CL = 3)	5.4ns (-13E/-133) 6ns (-10E)	54 60	54 60	54 60
11	Module configuration type	None	00	00	00
12	Refresh rate/type	(80) 15.6µs/SELF (82) 7.81µs/SELF	80	80	82
13	SDRAM width (primary SDRAM)	16	10	10	10
14	Error-checking SDRAM data width	None	00	00	00
15	Minimum clock delay, ^{t}CCD	1	01	01	01
16	Burst lengths supported	1, 2, 4, 8, page	8F	8F	8F
17	Number of internal banks on SDRAM device	4	04	04	04
18	CAS latencies supported	2, 3	06	06	06
19	CS latency	0	01	01	01
20	WE latency	0	01	01	01
21	SDRAM module attributes	Unbuffered	00	00	00
22	SDRAM device attributes: general	0E	0E	0E	0E
23	SDRAM cycle time, ^{t}CK (CL = 2)	7.5ns (-13E) 10ns (-133/-10E)	75 A0	75 A0	75 A0
24	SDRAM access from CK, ^{t}AC (CL = 2)	5.4ns (-13E) 6ns (-133/-10E)	54 60	54 60	54 60
25	SDRAM cycle time, ^{t}CK (CL = 1)	–	00	00	00
26	SDRAM access from CK, ^{t}AC (CL = 1)	–	00	00	00
27	Minimum row precharge time, ^{t}RP	15ns (-13E) 20ns (-133/-10E)	0F 14	0F 14	0F 14
28	Minimum row active to row active, ^{t}RRD	14ns (-13E) 15ns (-133) 20ns (-10E)	0E 0F 14	0E 0F 14	0E 0F 14
29	Minimum RAS# to CAS# delay, ^{t}RCD	15ns (-13E) 20ns (-133/-10E)	0F 14	0F 14	0F 14
30	Minimum RAS# pulse width, ^{t}RAS (see note 1)	45ns (-13E) 44ns (-133) 50ns (-10E)	2D 2C 32	2D 2C 32	2D 2C 32
31	Module rank density	32MB, 64MB, or 128MB	08	10	20
32	Command and address setup time	1.5ns (-13E/-133) 2ns (-10E)	15 20	15 20	15 20

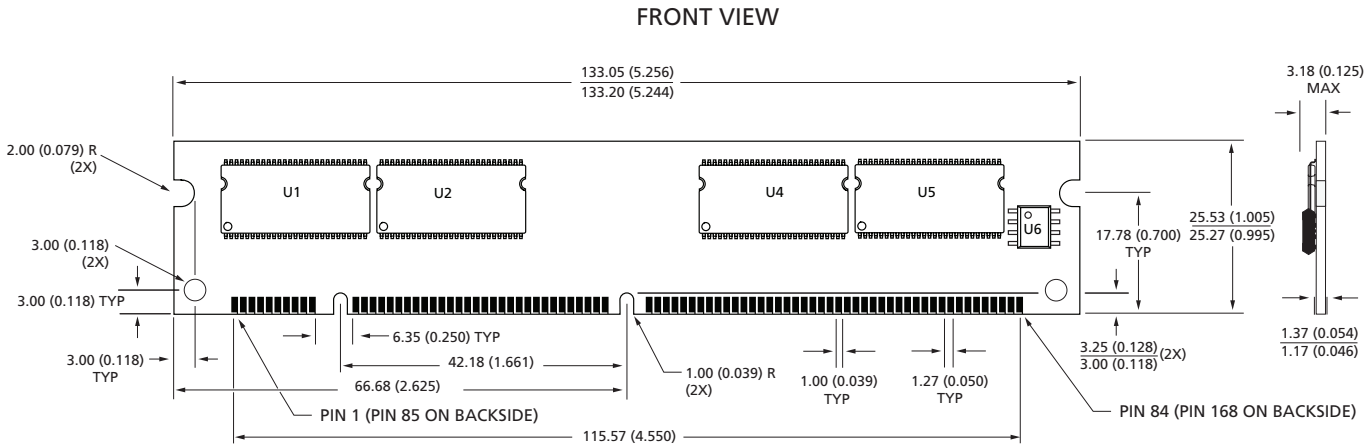
Table 21: Serial Presence-Detect Matrix (Continued)
"1"/"0": Serial data, "driven to HIGH"/"driven to LOW."

Byte	Description	Entry (Version)	32MB	64MB	128MB
33	Command and address hold time	0.8ns (-13E/-133) 1ns (-10E)	08 10	08 10	08 10
34	Data Signal input setup time	1.5ns (-13E/-133) 2ns (-10E)	15 20	15 20	15 20
35	Data signal input hold time	0.8ns (-13E/-133) 1ns (-10E)	08 10	08 10	08 10
36–61	Reserved		00	00	00
41	Device minimum active/auto-refresh time, ^{t}RC	60ns (-13E) 66ns (-133) 70ns (10E)	3C 42 46	3C 42 46	3C 42 46
42–61	Reserved		00	00	00
62	SPD revision	2	02	02	02
63	Checksum for bytes 0–62	-13E -133 -10E	82 CE 1A	8B D7 23	9E EA 36
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65–71	Manufacturer's JEDEC ID code (continued)		FF	FF	FF
72	Manufacturing location	1–12	01–0C	01–0C	01–0C
73–90	Module part number (ASCII)		Variable data	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable data	Variable data	Variable data
94	Week of manufacture in BCD		Variable data	Variable data	Variable data
95–98	Module serial number		Variable data	Variable data	Variable data
99–125	Manufacturer-specific data (reserved)		Variable data	Variable data	Variable data
126	System frequency	100/133 MHz	64	64	64
127	SDRAM component and clock detail		AF	AF	AF

Notes: 1. The value of ^{t}RAS used for the -13E part is calculated from ^{t}RC - ^{t}RP. Actual device specification value is 37ns.

Module Dimensions

Figure 10: 168-Pin DIMM



Notes:
1. All dimensions in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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