

# DDR2 SDRAM SODIMM

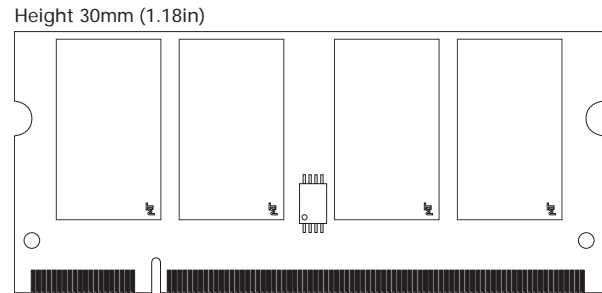
MT8HTF3264H(I) – 256MB  
 MT8HTF6464H(I) – 512MB  
 MT8HTF12864H(I) – 1GB

For component data sheets, refer to Micron's Web site: [www.micron.com/products/dram/ddr2](http://www.micron.com/products/dram/ddr2)

## Features

- 200-pin, small outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 256MB (32 Meg x 64), 512GB (64 Meg x 64), 1GB (128 Meg x 64)
- VDD = VDDQ = +1.8V
- VDDSPD = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 t<sub>CK</sub>
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 1: 200-pin SODIMM (MO-224 R/C "B")



## Options

- Operating temperature
- Commercial (0°C ≤ T<sub>C</sub> ≤ +85°C)
- Industrial (-40°C ≤ T<sub>C</sub> ≤ +95°C)<sup>1,2</sup>
- Package
  - 200-pin SODIMM (Pb-free)
- Frequency/CAS latency<sup>3</sup>
  - 2.5ns @ CL = 5 (DDR2-800)<sup>4</sup>
  - 2.5ns @ CL = 6 (DDR2-800)<sup>4</sup>
  - 3ns @ CL = 5 (DDR2-667)
  - 3.75ns @ CL = 4 (DDR2-533)
  - 5.0ns @ CL = 3 (DDR2-400)
- PCB Height
  - 30mm (1.18in)

## Marking

- I
- Y
- 80E
- 800
- 667
- 53E
- 40E

- Notes: 1. Industrial temperatures apply to DRAM only.  
 2. Contact Micron for product availability.  
 3. CL = CAS (READ) latency  
 4. Not available in 256MB density

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				t <sub>RCD</sub> (ns)	t <sub>RP</sub> (ns)	t <sub>RC</sub> (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	-	800	533	-	12.5	12.5	55
-800	PC2-6400	800	667	533	-	15	15	55
-667	PC2-5300	-	667	533	400	15	15	55
-53E	PC2-4200	-	-	533	400	15	15	55
-40E	PC2-3200	-	-	400	400	15	15	55



**Table 2: Addressing**

	256MB	512MB	1GB
Refresh count	8K	8K	8K
Row address	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)	1 (S0#)

**Table 3: Part Numbers and Timing Parameters – 256MB Modules**

Base device: MT47H32M8, 256Mb DDR2 SDRAM

Part Number <sup>1</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - t <sub>RCD</sub> - t <sub>RP</sub> )
MT8HTF3264HY-667__	256MB	32 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF3264HY-53E__	256MB	32 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF3264HY-40E__	256MB	32 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

**Table 4: Part Numbers and Timing Parameters – 512GB Modules**

Base device: MT47H64M8, 512Mb DDR2 SDRAM

Part Number <sup>1</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - t <sub>RCD</sub> - t <sub>RP</sub> )
MT8HTF6464HY-80E__	512MB	64 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT8HTF6464HY-800__	512MB	64 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT8HTF6464HY-667__	512MB	64 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF6464HY-53E__	512MB	64 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF6464HY-40E__	512MB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

**Table 5: Part Numbers and Timing Parameters – 1GB Modules**

Base device: MT47H128M8, 1Gb DDR2 SDRAM

Part Number <sup>1</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - t <sub>RCD</sub> - t <sub>RP</sub> )
MT8HTF12864HY-80E__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT8HTF12864HY-800__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT8HTF12864HY-667__	1GB	128 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF12864HY-53E__	1GB	128 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF12864HY-40E__	1GB	128 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

- Notes:
1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8HTF6464HY-40EC2.
  2. For the latest component data sheets, see Micron's Web site:  
[www.micron.com/products/dram/ddr2](http://www.micron.com/products/dram/ddr2)



## Module Pin Assignments and Descriptions

Table 6: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol		
1	VREF	51	DQS2	101	A1	151	DQ42	2	Vss	52	DM2	102	A0	152	DQ46
3	Vss	53	Vss	103	VDD	153	DQ43	4	DQ4	54	Vss	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	Vss	6	DQ5	56	DQ22	106	BA1	156	Vss
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	Vss	58	DQ23	108	RAS#	158	DQ52
9	Vss	59	Vss	109	WE#	159	DQ49	10	DM0	60	Vss	110	SO#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	Vss	12	Vss	62	DQ28	112	VDD	162	Vss
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	Vss	65	Vss	115	S1#	165	Vss	16	DQ7	66	Vss	116	NC/A13	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	Vss	68	DQS3#	118	VDD	168	Vss
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	Vss	71	Vss	121	Vss	171	Vss	22	DQ13	72	Vss	122	Vss	172	Vss
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	Vss	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	Vss	77	Vss	127	Vss	177	Vss	28	Vss	78	Vss	128	Vss	178	Vss
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	Vss	182	DQ61
33	Vss	83	NC	133	Vss	183	Vss	34	Vss	84	NC	134	DQ38	184	Vss
35	DQ10	85	NC/BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	Vss	38	DQ15	88	VDD	138	Vss	188	DQS7
39	Vss	89	A12	139	Vss	189	DQ58	40	Vss	90	A11	140	DQ44	190	Vss
41	Vss	91	A9	141	DQ40	191	DQ59	42	Vss	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	Vss	44	DQ20	94	A6	144	Vss	194	DQ63
45	DQ17	95	VDD	145	Vss	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	Vss
47	Vss	97	A5	147	DM5	197	SCL	48	Vss	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	Vss	199	VDDSPD	50	NC	100	A2	150	Vss	200	SA1

- Notes: 1. Pin 85 is NC for 256MB and 512GB, BA2 for 1GB.  
2. Pin 116 is NC for 256MB, A13 for 512MB and 1GB.

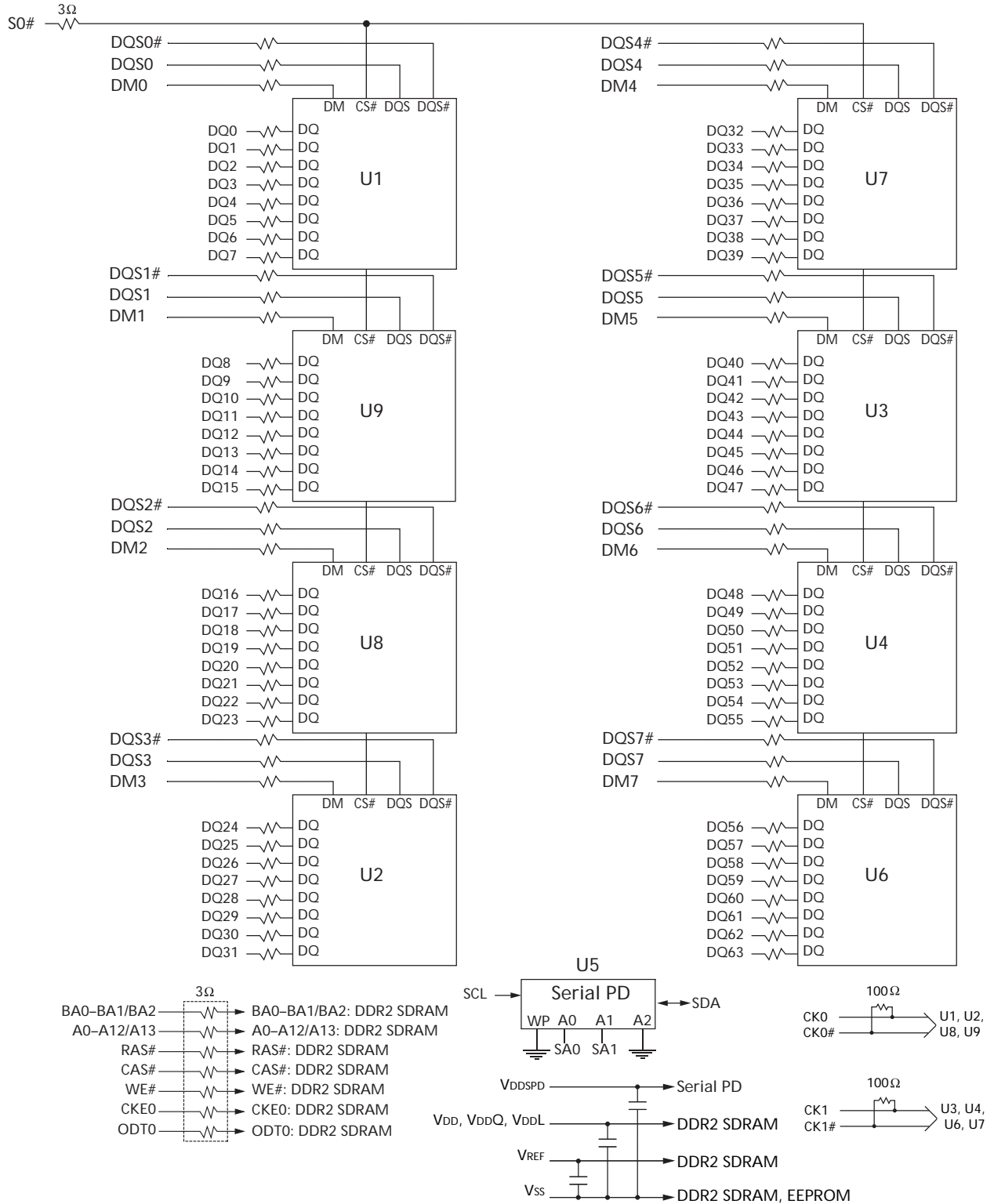


## 256MB, 512MB, 1GB: (x64, SR) 200-Pin DDR2 SDRAM SODIMM Module Pin Assignments and Descriptions

**Table 7: Pin Descriptions**

Symbol	Type	Description
ODT0, ODT1	Input	<b>On-die termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0# CK1, CK1#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CEK1	Input	<b>Clock enable:</b> CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all device banks idle), or ACTIVE power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once VDD is applied during first power-up. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation VREF must be maintained to this input.
S0#, S1#	Input	<b>Chip select:</b> S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1 (256MB, 512MB) BA0–BA2 (1GB)	Input	<b>Bank address inputs:</b> BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
A0–A12 (256MB), A0–A13 (512MB, 1GB)	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
DM0–DM7	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
SCL	Input	<b>Serial clock for presence-detect:</b> SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA1	Input	<b>Presence-detect address inputs:</b> These pins are used to configure the presence-detect device.
DQ0–DQ63	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQS0–DQS7, DQS0#–DQS7#	I/O	<b>Data strobe:</b> Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	<b>Serial presence-detect data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
VDD	Supply	<b>Power supply:</b> +1.8V ±0.1V.
VREF	Supply	SSTL_18 reference voltage.
VSS	Supply	Ground.
VDDSPD	Supply	<b>Serial EEPROM positive power supply:</b> +1.7V to +3.6V.

**Figure 2: Functional Block Diagram**



Notes: 1. Unless otherwise noted, resistor values are 22Ω.

## General Description

The MT8HTF3264H, MT8HTF6464H, and MT8HTF12864H DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x64 configuration. DDR2 SDRAM modules use internally configured quad-bank (256Mb, 512Mb) or eight-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single  $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during reads and by the memory controller during writes. DQS is edge-aligned with data for reads and center-aligned with data for writes.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

## Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 8: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units	
VDD	VDD supply voltage relative to Vss	-1.0	+2.3	V	
VDDQ	VDDQ supply voltage relative to Vss	-0.5	+2.3	V	
VDDL	VDDL supply voltage relative to Vss	-0.5	+2.3	V	
VIN, VOUT	Voltage on any pin relative to Vss	-0.5	+2.3	V	
I <sub>I</sub>	Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤ 0.95V; (all other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE, ODT	-40	+40	μA
		CK, CK#	-20	+20	
		DM	-5	+5	
I <sub>OZ</sub>	Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	-5	+5	μA	
I <sub>VREF</sub>	VREF leakage current; VREF = Valid VREF level	-16	+16	μA	
T <sub>CASE</sub>	DDR2 SDRAM device operating temperature <sup>1</sup>	Commercial	0	+85	°C
		Industrial <sup>2</sup>	-40	+95	°C

- Notes: 1. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site at [www.micron.com/technotes](http://www.micron.com/technotes).  
2. Refresh rate must double when T<sub>CASE</sub> exceeds 85°C.

## Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

## Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets, available at Micron's Web site. Module speed grades correlate with component speed grades as shown in Table 9:

**Table 9: Module and Component Speed Grade Table**

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-53E



**Table 10: DDR2 IDD Specifications and Conditions – 256MB**  
Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-667	-53E	-40E	Units
<b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} MIN (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	720	640	600	mA
<b>Operating one bank active-read-precharge current;</b> $I_{OUT} = 0mA$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} MIN (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	800	720	680	mA
<b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	40	40	40	mA
<b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	320	280	200	mA
<b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	320	280	240	mA
<b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	240	200	160	mA
		Slow PDN Exit MR[12] = 1	48	48	48
<b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} MAX (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	400	320	240	mA
<b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} MAX (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1,520	1,280	1,000	mA
<b>Operating burst read current;</b> All device banks open, continuous burst reads, $I_{OUT} = 0mA$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} MAX (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1,440	1,200	920	mA
<b>Burst refresh current;</b> $t_{CK} = t_{CK} (IDD)$ ; Refresh the command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	1,440	1,360	1,320	mA
<b>Self refresh current;</b> CK and CK# at 0V; $CKE \leq 0.2V$ ; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	40	40	40	mA
<b>Operating bank interleave read current;</b> All device banks interleaving reads, $I_{OUT} = 0mA$ ; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$ ; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RRD} = t_{RRD} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail	IDD7	2,080	1,920	1,840	mA





**Table 11: DDR2 IDD Specifications and Conditions – 512GB**  
Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	-40E	Units	
<b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	800	720	640	640	mA	
<b>Operating one bank active-read-precharge current;</b> $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	920	840	760	720	mA	
<b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	56	56	56	56	mA	
<b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	400	360	320	280	mA	
<b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	440	400	360	320	mA	
<b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	320	280	240	200	mA
		Slow PDN Exit MR[12] = 1	96	96	96	96	mA
<b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	560	520	440	360	mA	
<b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1560	1360	1120	920	mA	
<b>Operating burst read current;</b> All device banks open, continuous burst reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1640	1440	1160	920	mA	
<b>Burst refresh current;</b> $t_{CK} = t_{CK} (IDD)$ ; Refresh the command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	1840	1440	1360	1320	mA	
<b>Self refresh current;</b> CK and CK# at 0V; $CKE \leq 0.2\text{V}$ ; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	56	56	56	56	mA	
<b>Operating bank interleave read current;</b> All device banks interleaving reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$ ; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RRD} = t_{RRD} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselections; Data bus inputs are switching; See IDD7 conditions for detail	IDD7	2400	1920	1800	1760	mA	



**Table 12: DDR2 IDD Specifications and Conditions – 1GB (die revision A)**  
Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	-40E	Units	
<b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	800	720	640	560	mA	
<b>Operating one bank active-read-precharge current;</b> $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	880	800	760	640	mA	
<b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	56	56	56	56	mA	
<b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	520	440	328	280	mA	
<b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	560	480	360	320	mA	
<b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	360	320	280	280	mA
		Slow PDN Exit MR[12] = 1	112	112	112	112	mA
<b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	600	560	440	360	mA	
<b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1480	1280	1,040	880	mA	
<b>Operating burst read current;</b> All device banks open, continuous burst reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1520	1280	1040	880	mA	
<b>Burst refresh current;</b> $t_{CK} = t_{CK} (IDD)$ ; Refresh the command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	2240	2080	2000	1760	mA	
<b>Self refresh current;</b> CK and CK# at 0V; CKE $\leq 0.2\text{V}$ ; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	56	56	56	56	mA	
<b>Operating bank interleave read current;</b> All device banks interleaving reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$ ; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RRD} = t_{RRD} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselections; Data bus inputs are switching; See IDD7 conditions for detail	IDD7	2680	2400	2320	2080	mA	



**Table 13: DDR2 IDD Specifications and Conditions – 1GB (die revision E)**  
Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	-40E	Units	
<b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	720	680	560	560	mA	
<b>Operating one bank active-read-precharge current;</b> $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	880	800	760	720	mA	
<b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	56	56	56	56	mA	
<b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	400	320	320	280	mA	
<b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	400	320	320	280	mA	
<b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	320	240	240	240	mA
		Slow PDN Exit MR[12] = 1	80	80	80	80	mA
<b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	480	440	360	320	mA	
<b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1280	1080	1000	840	mA	
<b>Operating burst read current;</b> All device banks open, continuous burst reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1280	1080	1000	840	mA	
<b>Burst refresh current;</b> $t_{CK} = t_{CK} (IDD)$ ; Refresh the command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	1880	1720	1680	1640	mA	
<b>Self refresh current;</b> CK and CK# at 0V; CKE $\leq 0.2\text{V}$ ; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	56	56	56	56	mA	
<b>Operating bank interleave read current;</b> All device banks interleaving reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$ ; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RRD} = t_{RRD} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselections; Data bus inputs are switching; See IDD7 conditions for detail	IDD7	2680	2240	2160	2080	mA	

## Serial Presence-Detect

**Table 14: Serial Presence-Detect EEPROM DC Operating Conditions**

All voltages referenced to V<sub>SS</sub>; V<sub>DDSPD</sub> = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V <sub>DDSPD</sub>	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V <sub>IH</sub>	V <sub>DDSPD</sub> × 0.7	V <sub>DDSPD</sub> + 0.5	V
Input low voltage: Logic 0; All inputs	V <sub>IL</sub>	-0.6	V <sub>DDSPD</sub> × 0.3	V
Output low voltage: I <sub>OUT</sub> = 3mA	V <sub>OL</sub>	-	0.4	V
Input leakage current: V <sub>IN</sub> = GND to V <sub>DD</sub>	I <sub>LI</sub>	0.10	3	μA
Output leakage current: V <sub>OUT</sub> = GND to V <sub>DD</sub>	I <sub>LO</sub>	0.05	3	μA
Standby current	I <sub>SB</sub>	1.6	4	μA
Power supply current, READ: SCL clock frequency = 100 KHz	I <sub>CC<sub>R</sub></sub>	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	I <sub>CC<sub>W</sub></sub>	2	3	mA

**Table 15: Serial Presence-Detect EEPROM AC Operating Conditions**

All voltages referenced to V<sub>SS</sub>; V<sub>DDSPD</sub> = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t <sup>AA</sup>	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t <sup>BUF</sup>	1.3	-	μs	
Data-out hold time	t <sup>DH</sup>	200	-	ns	
SDA and SCL fall time	t <sup>F</sup>	-	300	ns	2
Data-in hold time	t <sup>HD:DAT</sup>	0	-	μs	
Start condition hold time	t <sup>HD:STA</sup>	0.6	-	μs	
Clock HIGH period	t <sup>HIGH</sup>	0.6	-	μs	
Noise suppression time constant at SCL, SDA inputs	t <sup>I</sup>	-	50	ns	
Clock LOW period	t <sup>LOW</sup>	1.3		μs	
SDA and SCL rise time	t <sup>R</sup>	-	0.3	μs	2
SCL clock frequency	f <sup>SCL</sup>	-	400	KHz	
Data-in setup time	t <sup>SU:DAT</sup>	100	-	ns	
Start condition setup time	t <sup>SU:STA</sup>	0.6	-	μs	3
Stop condition setup time	t <sup>SU:STO</sup>	0.6	-	μs	
WRITE cycle time	t <sup>WRC</sup>	-	10	ms	4

- Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
  2. This parameter is sampled.
  3. For a reSTART condition, or following a WRITE cycle.
  4. The SPD EEPROM WRITE cycle time (t<sup>WRC</sup>) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.



**Table 16: Serial Presence-Detect Matrix**

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 15

Byte	Description	Entry (Version)	MT8HTF3264H	MT8HTF6464H	MT8HTF12864H
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on assembly	13, 14	0D	0E	0E
4	Number of column addresses on assembly	10	0A	0A	0A
5	DIMM height and module ranks	30mm, Single Rank	60	60	60
6	Module data width	64	40	40	40
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	SDRAM cycle time, <sup>t</sup> CK (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	- 30 3D 50	25 30 3D 50	25 30 3D 50
10	SDRAM access from clock, <sup>t</sup> AC (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	- 45 50 60	40 45 50 60	40 45 50 60
11	Module configuration type		00	00	00
12	Refresh rate/type	7.81µs/SELF	82	82	82
13	SDRAM device width (primary SDRAM)	8	08	08	08
14	Error-checking SDRAM data width	n/a	00	00	00
15	Minimum clock delay, back-to-back random column access	1 clock	00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	04	08
18	CAS latencies supported	-80E (5, 4) -800 (6, 5, 4) -667 (5, 4, 3) -53E/-40E (4, 3)	- - 38 18	30 70 38 18	30 70 38 18
19	Module thickness		01	01	01
20	DDR2 DIMM type	SODIMM	04	04	04
21	SDRAM module attributes		00	00	00
22	SDRAM device attributes: Weak driver (01) and 50Ω ODT (03)	-80E/-800/-667 -53E/-40E	-/03 <sup>2</sup> 01	03 01	03 01
23	SDRAM cycle time, <sup>t</sup> CK, MAX CL - 1	-80E/-667 -800 -53E/-40E	-/3D <sup>2</sup> - 50	3D 30 50	3D 30 50
24	SDRAM access from CK, <sup>t</sup> AC, MAX CL - 1	-80E/-800 -667 -53E -40E	- 45 50 60	40 45 50 60	40 45 50 60
25	SDRAM cycle time, <sup>t</sup> CK, MAX CL - 2	-80E(N/S) -800 -667 -53E/-40E(N/S)	00 - 50 -/00 <sup>2</sup>	00 3D 50 00	00 3D 50 00



**Table 16: Serial Presence-Detect Matrix**

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 15

Byte	Description	Entry (Version)	MT8HTF3264H	MT8HTF6464H	MT8HTF12864H
26	SDRAM access from CK, $t_{AC}$ , MAX CL - 2	-80E(N/S) -800 -667 -53E/-40E(N/S)	00 - 45 -/00 <sup>2</sup>	00 40 45 00	00 40 45 00
27	Minimum row precharge time, $t_{RP}$	-80E -800/-667/-53E/-40E	- -/3C <sup>2</sup>	32 3C	32 3C
28	Minimum row active to row active, $t_{RRD}$		1E	1E	1E
29	Minimum RAS#-to-CAS# delay, $t_{RCD}$	-80E -800/-667/-53E/-40E	- -/3C <sup>2</sup>	32 3C	32 3C
30	Minimum RAS# pulse width, $t_{RAS}$	-80E/-800/-667/-53E -40E	-/2D <sup>2</sup> 28	2D 28	2D 28
31	Module rank density	256MB, 512MB, 1GB	40	80	01
32	Address and command setup time, $t_{IS_b}$	-80E/-800 -667 -53E -40E	- 20 25 35	17 20 25 35	17 20 25 35
33	Address and command hold time, $t_{IH_b}$	-80E/-800 -667 -53E -80E	- 27 37 47	25 27 37 47	25 27 37 47
34	Data/data mask input setup time, $t_{DS_b}$	-80E/-800 -667/-53E -40	- 10 15	05 10 15	05 10 15
35	Data/data mask input hold time, $t_{DH_b}$	-80E/-800 -667 -53E -40E	- 17 22 27	12 17 22 27	12 17 22 27
36	Write recovery time, $t_{WR}$		3C	3C	3C
37	WRITE-to-READ command delay, $t_{WTR}$	-80E/-667/-53E -800/-40E	-/1E <sup>2</sup> -/28 <sup>2</sup>	1E 28	1E 28
38	READ-to-PRECHARGE command delay, $t_{RTP}$		1E	1E	1E
39	Memory analysis probe		00	00	00
40	Extension for bytes 41 and 42	-80E -800/-667/-53E/-40E	- -/00 <sup>2</sup>	30 00	36 06
41	Minimum active auto refresh time, $t_{RC}$ (see note 1)	-80E -800/-667/-53E -40E	- -/3C <sup>2</sup> 37	39 3C 37	39 3C 37
42	Minimum AUTO REFRESH to ACTIVE/ AUTO REFRESH command period, $t_{RFC}$		-/4B <sup>2</sup>	69	7F
43	SDRAM device MAX cycle time, $t_{CK MAX}$		-/80 <sup>2</sup>	80	80
44	SDRAM device MAX DQS-DQ skew time, $t_{DQSQ}$	-80E/-800 -667 -53E -40E	- 18 1E 23	14 18 1E 23	14 18 1E 23
45	SDRAM device MAX read data hold skew factor, $t_{QHS}$	-80E/-800 -667 -53E -40E	- 22 28 2D	1E 22 28 2D	1E 22 28 2D

**Table 16: Serial Presence-Detect Matrix**

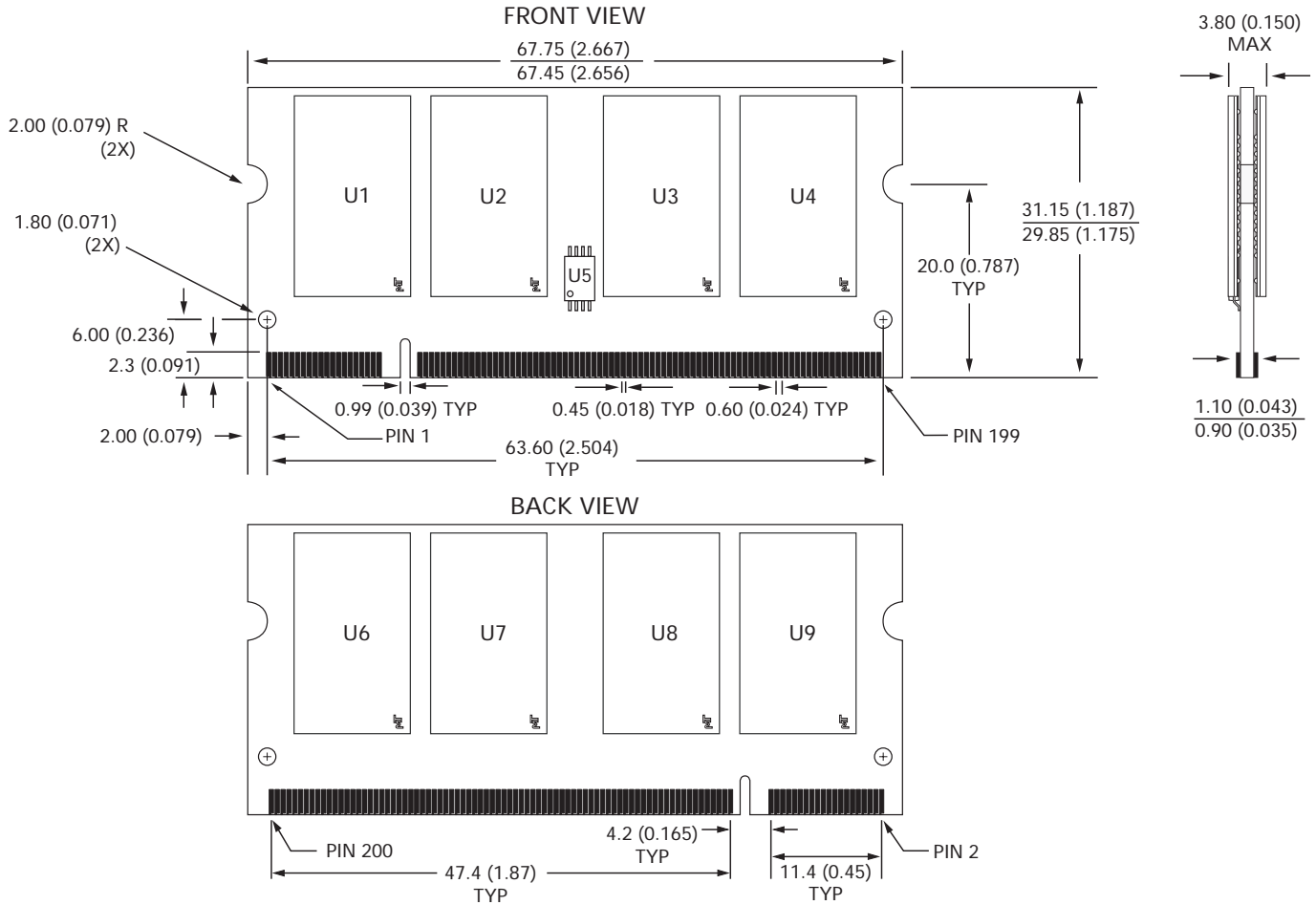
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 15

Byte	Description	Entry (Version)	MT8HTF3264H	MT8HTF6464H	MT8HTF12864H
46	PLL relock time		00	00	00
47–61	Optional features, not supported		00	00	00
62	SPD revision	version 1.2	12	12	12
63	Checksum for bytes 0–62	-80E	–	91	32
		-800	–	32	D3
		-667	EE	4D	EE
		-53E	99	F8	99
		-40E	00	5F	00
64	Manufacturer's JEDEC ID code	2C	2C	2C	2C
65–71	Manufacturer's JEDEC ID code	FF	FF	FF	FF
72	Manufacturing location	01–0C	01–0C	01–0C	01–0C
73–90	Module part number (ASCII)		Variable Data	Variable Data	Variable Data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	00	00	00	00
93	Year of manufacture in BCD		Variable Data	Variable Data	Variable Data
94	Week of manufacture in BCD		Variable Data	Variable Data	Variable Data
95–98	Module serial number		Variable Data	Variable Data	Variable Data
99–127	Manufacturer-specific data (RSVD)		00	00	00
128–255	Customer-specific data (RSVD)		FF	FF	FF

- Notes:
1. The <sup>t</sup>RC SPD values shown are based on the JEDEC standard values. The actual Micron device specification is <sup>t</sup>RC = 55ns.
  2. The 256MB module (MT8HTF3264H) is not available in -80E or -800 speed grades.

## Module Dimensions

Figure 3: 200-pin DDR2 SODIMM Module Dimensions



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
  2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.



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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.





## Revision History

<b>Rev. D, Released (No Mark)</b> .....	<b>10/06</b>
<ul style="list-style-type: none"><li>• Added -80E speed grade</li><li>• Added -800 speed grade</li><li>• Added IDD values for Rev E components (U48B die rev)</li><li>• Added industrial temperature availability</li><li>• Added support for CL4 @ 533; modified SPD to reflect this.</li><li>• Removed T storage&gt; clarified temperature ratings.</li><li>• Minor formatting changes</li></ul>	
<b>Rev. C, Released (No Mark)</b> .....	<b>1/06</b>
<ul style="list-style-type: none"><li>• Removed component specifications</li></ul>	
<b>Rev. A, Released (No Mark)</b> .....	<b>3/05</b>
<ul style="list-style-type: none"><li>• New data sheet (leveraged from HTF8C32_64_128X64HG)</li></ul>	