PD70224

Datasheet

IdealBridge™ Dual MOSFET-based Bridge Rectifier

August 2019

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in August 2019. The following is a summary of changes.

- Package marking was updated. For more information, see Ordering Information (see page 21).

1.2 Revision 2.0

Revision 2.0 was published in January 2018. The following is a summary of changes in revision 2.0 of this document:

- The formatting of this document was updated to the latest template.
- Updated SOA Graph to show Test Methodology and discuss protection recommendations.
- MSL3 compliance added
- Recommended Protection Scheme moved to the Application Note “ Design for PD System Surge Immunity"

1.3 Revision 1.1

Revision 1.1 was published in July 2015. In revision 1.1 of this document, maximum SUPP_Sx current, application information, adding SOA graph. Also, updated MSL level was added.

1.4 Revision 1.0

Revision 1.0 was published in March 2015. In revision 1.0 of this document, ESD was updated.

1.5 Revision 0.72

Revision 0.72 was published in May 2014. In revision 0.72 of this document, dimensions to recommended layout add IMAX_LOAD was added.

1.6 Revision 0.7

Revision 0.7 was published in May 2014. It was the first publication of this document.

2 Product Overview

PD70224 is a dual pack of MOSFET-based full-bridge rectifiers. It contains low-R_{DS} 0.16 Ω N-channel MOSFETs for much higher overall efficiency and higher output power, particularly when used in Powered Devices for Power over Ethernet (PoE) applications. The entire drive circuitry for driving the MOSFETs is on-chip, including a charge pump for driving the high-side N-channel MOSFETs. The total forward drop (bridge offset) introduced by the IdealBridge™ rectifier is only 192 mV at 0.6A, compared to a standard bridge rectifier that typically presents 2000 mV of forward drop.

PD70224 IdealBridge™ can support over 1A current, making it the ideal choice not only for modern energy-saving 2-pair applications compliant with IEEE802.3af and IEEE802.3at (Type 1 and Type 2), but also 4-pair Powered Devices such as 60 watt and POH (Power over HDBase-T, 95W).

In addition, PD70224 is capable of helping to identify at the physical layer itself whether a 2-pair PSE or a 4-pair PSE is providing power over the cable. It does that by sensing the voltage on the line (un-rectified) side of the pairs.

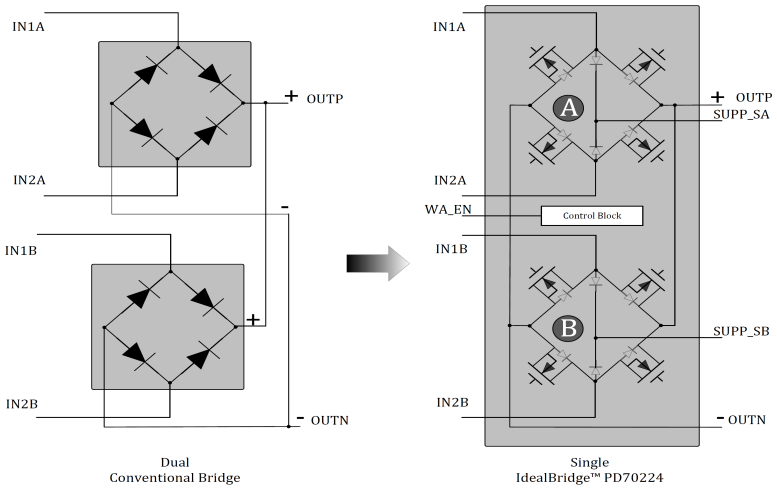
2.1 Features

- Active circuit with low forward-drop to replace dissipative passive diode bridges
- Self-contained drive circuitry for MOSFETs
- Designed to support IEEE802.3af/at, UPOE and Power over HDBase-T (PoH)
- Integrated 0.16 Ω N-Channel MOSFETs for 0.32 Ω total path resistance
- “Power present” indicator signals for identifying 4-pair bridge power
- Low leakage, < 10 µA during detection
- Wide operating voltage range up to 57 V
- -40°C to +85°C ambient
- Available in 40 pin package
- MSL3, RoHS Compliant

2.2 Applications

- Power over Ethernet (all IEEE compliant 2-pair modes)
- Proprietary 4-pair standards, UPOE (Universal PoE), IEEE802.3bt and POH

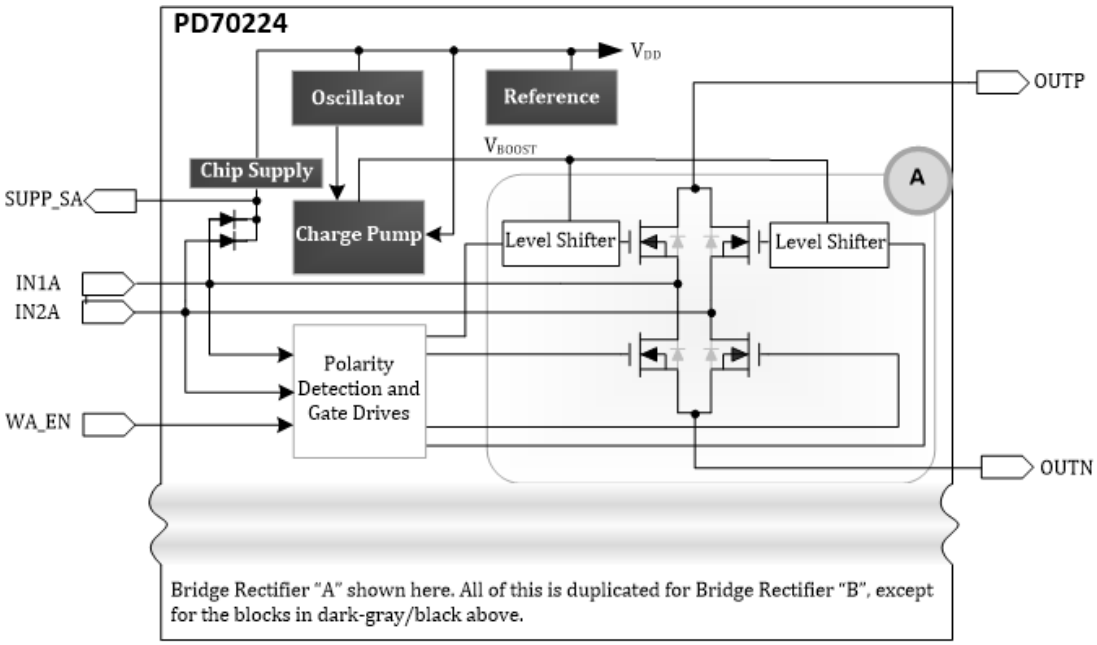
Figure 1 • Dual Conventional Bridge versus Single Ideal Bridge

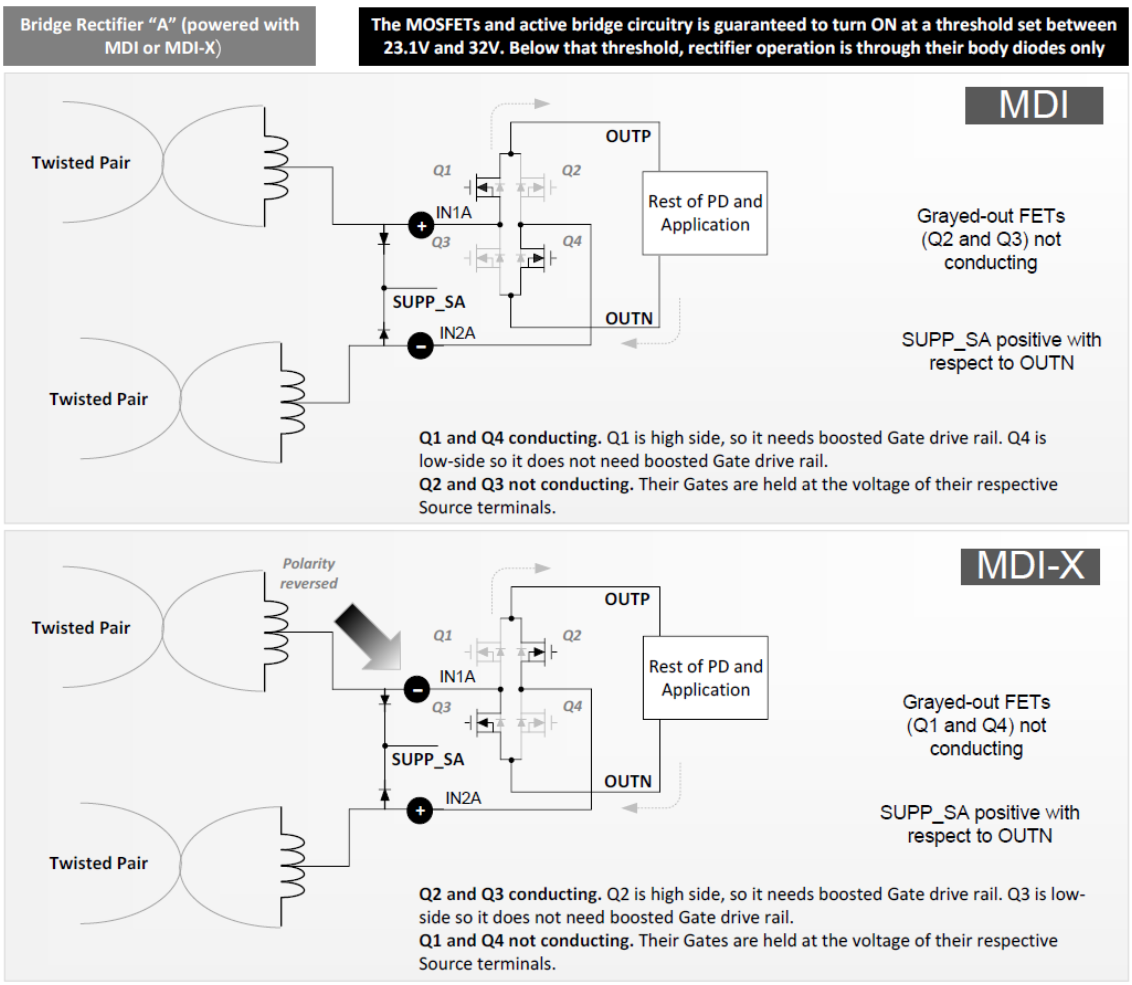


3 Functional Descriptions

The following figure shows the functional blocks of PD70224.

Figure 2 • Block Diagram





3.1 Purpose of Charge Pump

In the case that follows, the FETs connected to OUTP (the "high-side" FETs) are the ones that require a boosted Gate drive rail so they can be turned ON. The on-chip charge pump provides the boosted Gate drive rail for the high-side FETs. The FETs connected to OUTN ("low-side" FETs) do not need a boosted drive rail to be turned ON.

3.2 Purpose and Use of Supply Pins

Since the twisted pair set is delivering power, in the following case, SUPP_SA is positive with respect to OUTN. But if these two twisted pairs were not connected to a PSE, SUPP_SA would be low. For a standard 2-pair or 4-pair PDs with two bridge rectifiers (4-pairs), one connected to the data pairs, the other to the spare pairs, the presence of high voltage on SUPP_SA and/or SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUP_SA and/or SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUPP_SB can be used to indicate 2-pair or 4-pair PoE operation.

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

Table 1 • Absolute Maximum Ratings

Parameter		Min	Max	Units
IN1A, IN1B, IN2A, IN2B to OUTN		-0.3	74	V
IN1A to IN2A		-0.3	74	V
IN1B to IN2B		-0.3	74	V
IN1A, IN1B, IN2A, IN2B to OUTP		-74		V
IN1A, IN2A to IN1B		-0.3	74	V
IN1A, IN2A to IN2B		-0.3	74	V
OUTP to OUTN		-0.3	74	V
OUTP to IN1A, IN1B, IN2A, IN2B		-0.3	74	V
SUPP_SA, SUPP_SB to OUTN		-0.3	74	V
WA_EN to OUTN		-0.3	5.5	V
I_{INA}, I_{INB} (currents through bridge A or B)			1.5	A
Junction Temperature			150	°C
Lead Soldering Temperature (40s, reflow)			260	°C
Storage Temperature		-65	150	°C
ESD rating	HBM		±1250[1]	V
	MM		±100	V
	CDM		±2000	V

1. All pins pass 1250v, Except IN1A and IN2A that Pass 1000v

Note: EPAD1 is connected by copper plane on PCB to OUTP, and EPAD2 is similarly connected to OUTN. OUTN is ground for IC.

4.2 Operating Ratings

Performance is generally guaranteed over this range as provided under Electrical Characteristics (see page 7).

Table 2 • Operating Ratings

Parameter	Min	Max	Units
IN1A, IN1B to OUTN		57	V
IN2A, IN2B to OUTN		57	V
WA_EN to OUTN	-0.3	5	V
Junction Temperature	-40	125	°C
Port Current (I_{INx})	0	1.5	A

4.3 Electrical Characteristics

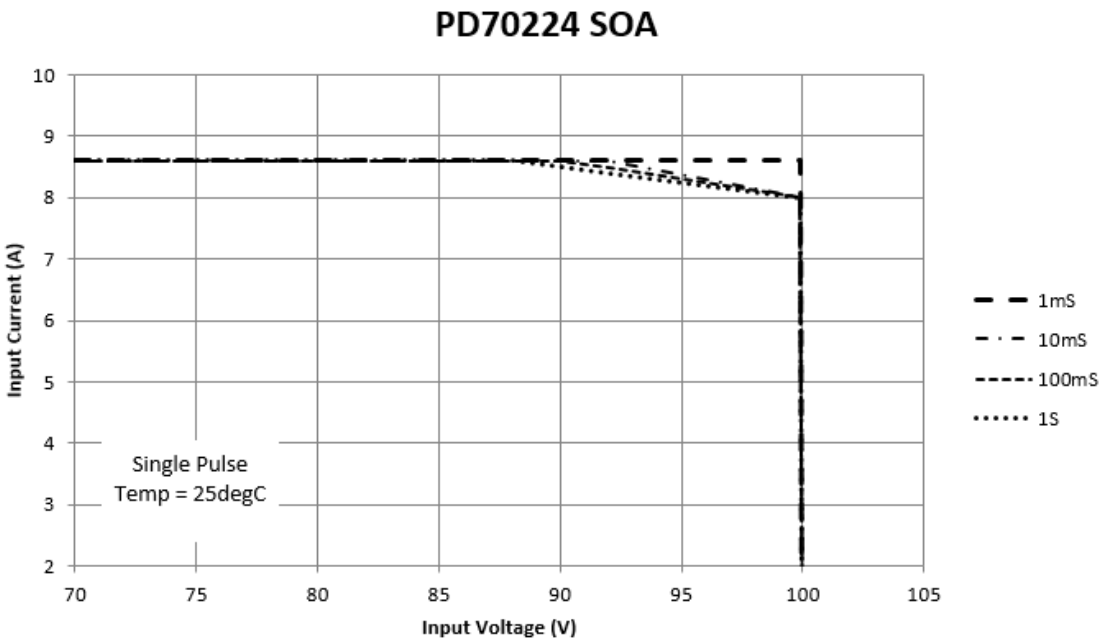
Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25°C ambient.

Table 3 • Typical Electrical Performance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{INx}	Input Voltage for Bridge “x”, where x is “A” or “B”.				57	V
ΔI_Q	Differential Quiescent Current I(Vin=10.1V) – I(Vin=2.5V);	2.5 V < V_{INx} < 10.1 V; No load between OUTP and OUTN; No load on SUPP_Sx pins.		6	10	µA
I_Q	Quiescent Current (single bridge)	10.2 V < V_{INx} < 23 V; No load between OUTP & OUTN; No load on SUPP_Sx pins.			85	µA
	Quiescent Current (both bridge combined)	V_{INx} = 55V; No load between OUTP & OUTN; No load on SUPP_Sx pins.			900	µA
V_{TURN_ON}	Active turn-on voltage of FETs		23.1	27.5	32	V
V_{HYST}	Turn-on voltage hysteresis			0.4		V

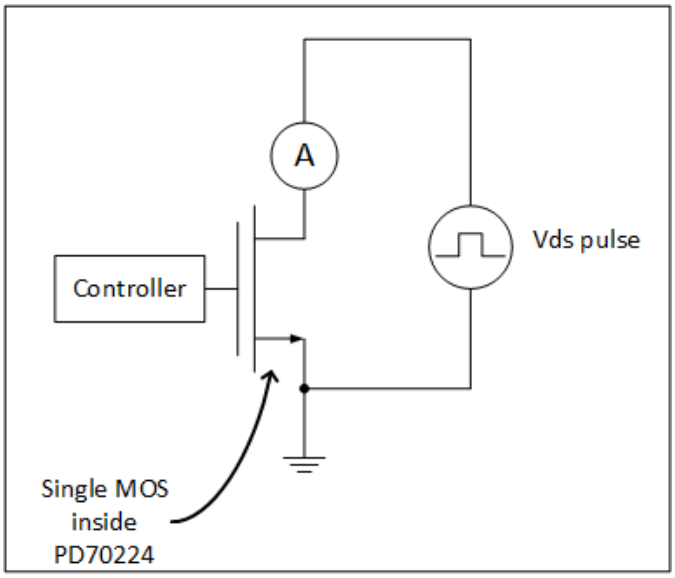
Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{ALT}	Alternate input voltage polarity – Delay time required (Vin = 0V) while alternating input voltage polarity		200			ms
V_{OFFSET}	Bridge offset @ Off state	V_{INx} < V_{TURN_ON}, two body diodes in series I_{INx} = 40mA			1.8	V
R_{DS}	FET Drain to Source Resistance	I_D = 0.6A T_J = 25°C		0.16	0.26	Ω
		I_D = 0.6A; - 40°C ≤ T_J ≤ 125°C			0.38	Ω
I_R	Leakage Current (Reverse)	V_{OUTP} – V_{OUTN} = 57V			80	µA
V_{BFD}	Backfeed Voltage	Between input terminals with 100 kΩ resistor across them and 57V between OUTP and OUTN			2.7	V
I_{MAX_Off}	Maximum Forward Current (per bridge) below V_{TURN_ON}				0.45	A
I_{MAX_On}	Maximum Forward Current (per bridge) above V_{TURN_ON}. Per bridge, while only one bridge out of the two is active.				1.5	A
I_{MAX_LOAD}	Maximum Load Current (per device) above V_{TURN_ON}. Per device while two bridges are active and each bridge is supporting half load				2	A
V_{D_SUPP}	Maximum voltage drop between INx to SUPP_Sx pins.	Supp_Sx Loaded with 100 kΩ resistor			2	V
I_{MAX_SUPP}	Maximum current to consume from SUPP_Sx pins.				10	mA
V_{IH}	WA_EN - Input high logic		1.35			V
V_{IL}	WA_EN - Input low logic				1.05	V

Figure 3 • Safe Operating Area



The PD70224 (PD70224L) SOA is based on measuring the SOA of a single NMOS device that is used to construct the diode bridge.

Figure 4 • SOA Test Setup



This data is provided for information purposes. For additional information on Surge Immunity and Microsemi Recommendations, see the Application Note “Design for PD System Surge Immunity”.

5 Pin Descriptions

The following illustration is a representation of PD70224 device, as seen from the top and bottom view.

Figure 5 • Internal Construction and Pinout

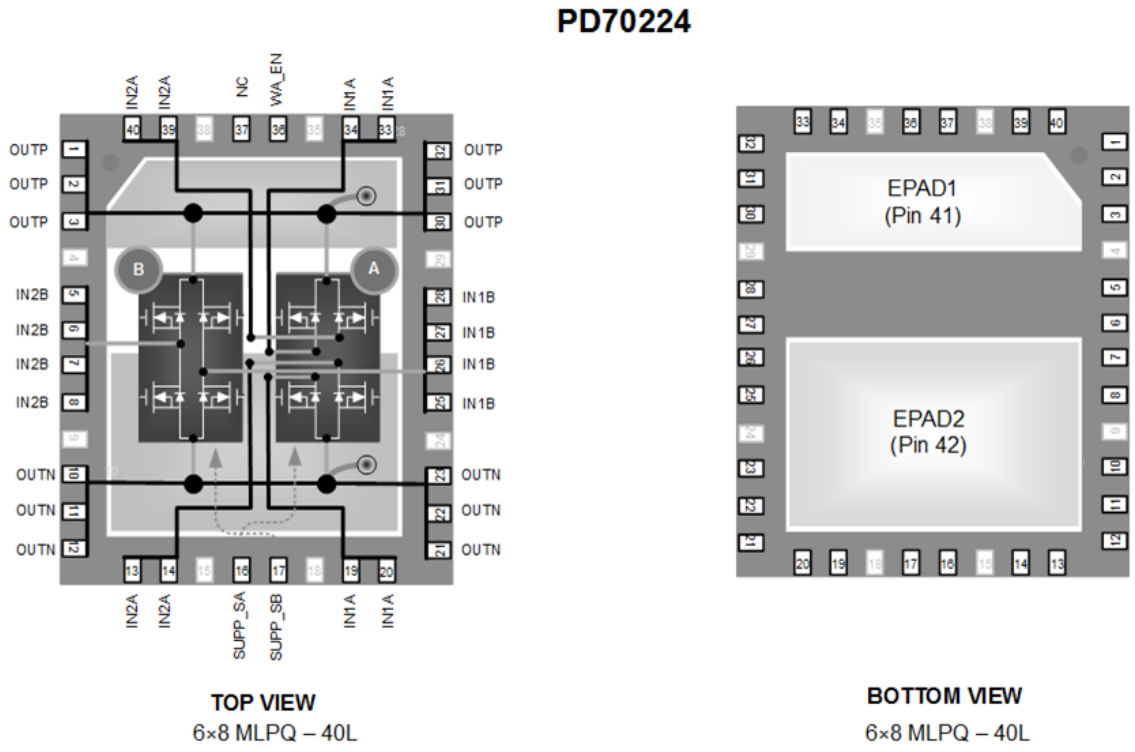


Table 4 • Pin Description

Pin Number PD70224 MLP-Quad 52 lead	Pin Designator	Description
1, 2, 3	**OUTP**	Rectified positive (upper) rail shared by both bridges
4	**N.A.**	Not applicable (pin not present)
5, 6, 7, 8	**IN2B**	Input “2” of bridge rectifier number B
9	**N.A.**	Not applicable (pin not present)
10, 11, 12	**OUTN**	Rectified negative (lower) rail shared by both bridges
13, 14	**IN2A**	Input “2” of bridge rectifier number A. Same as Pins 39 and 40. [1]
15	**N.A.**	Not applicable (pin not present)
16	**SUPP_SA**	Input power supply detect pin for bride rectifier number A. Goes high when pairs connected to this bridge are powered by the PSE.
	N.A.	Not applicable (pin not present)
17	**SUPP_SB**	Input power supply detect pin for bride rectifier number B. Goes high when pairs connected to this bridge are powered by the PSE.

Pin Number PD70224 MLP-Quad 52 lead	Pin Designator	Description
18	**N.A.**	Not applicable (pin not present)
19, 20	**IN1A**	Input “1” of bridge rectifier number A. [2]
21, 22, 23	**OUTN**	Rectified negative (lower) rail shared by both bridges, same as Pins 10, 11 and 12.
24	**N.A.**	Not applicable (pin not present)
25, 26, 27, 28	**IN1B**	Input “1” of bridge rectifier number B
29	**N.A.**	Not applicable (pin not present)
30, 31, 32	**OUTP**	Rectified positive (upper) rail shared by both bridges. Same as Pins 1, 2 and 3
33, 34	**IN1A**	Input “1” of bridge rectifier number A. Same as Pins 19 and 20. [3]
35	**N.A.**	Not applicable (pin not present)
36	**WA_EN**	While this input is low (referenced to OUTN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature, that is, turn OFF internal switches and act as regular diode bridge.
	N.A.	Not applicable (pin not present)
37	**N.C**	Not connected; do not connect externally (leave floating)
38	**N.A.**	Not applicable (pin not present)
39, 40	**IN2A**	Input “2” of bridge rectifier number A. Same as Pins 13 and 14. [4]
41	**EPAD1**	Connect to OUTP on PCB
42	**EPAD2**	Connect to OUTN on PCB

1. These pins are not shorted to pins 39 and 40 inside the device. The device functionality relies on a copper trace on the PCB, between pins 13, 14, 39 and 40.
2. These pins are not shorted to pins 33 and 34 inside the device. The device functionality relies on a copper trace on the PCB, between pins 33, 34, 19 and 20.
3. These pins are not shorted to pins 19 and 20 inside the device. The device functionality relies on a copper trace on the PCB, between pins 33, 34, 19 and 20.
4. These pins are not shorted to pins 13 and 14 inside the device. The device functionality relies on a copper trace on the PCB, between pins 13, 14, 39 and 40.

6 Package Information

6.1 Package Outline Drawing

Figure 6 • PD70224 Package Outline Drawing 40 Pin QFN 6x8 (mm)

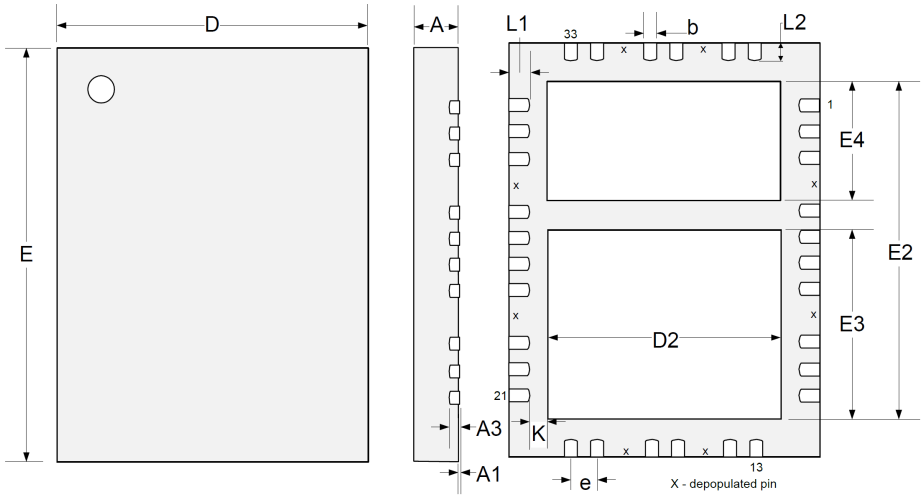


Table 5 • Package Measurements

Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.00 BSC		0.236 BSC	
E	8.00 BSC		0.315 BSC	
D2	4.25	4.50	0.167	0.177
E2	6.35	6.6	0.250	0.260
E3	3.50	3.75	0.138	0.148
E4	2.20	2.46	0.087	0.097
e	0.50 BSC		0.020 BSC	
K	1.016	-	0.040	-
L1	0.37	0.57	0.014	0.022
L2	0.30	0.50	0.012	0.020

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

6.2 Thermal Specifications

The following table lists the thermal specifications of PD70224.

Table 6 • Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		31		°C/W
θ_{JL}		2.5		°C/W
θ_{JC}		5		°C/W

Note: The θ_{JX} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

PD70224 Recommended PCB layout for 40 Pin QFN 6x8 (mm)

Recommended PCB layout pattern for PD70224 is described in the following three figures.

Pad of pins number 4, 9, 15, 18, 24, 29, 35 and 38 are missing from the layout because it do not exist in package.

Figure 7 • PD70224 Top layer Copper Recommended PCB Layout (mm)

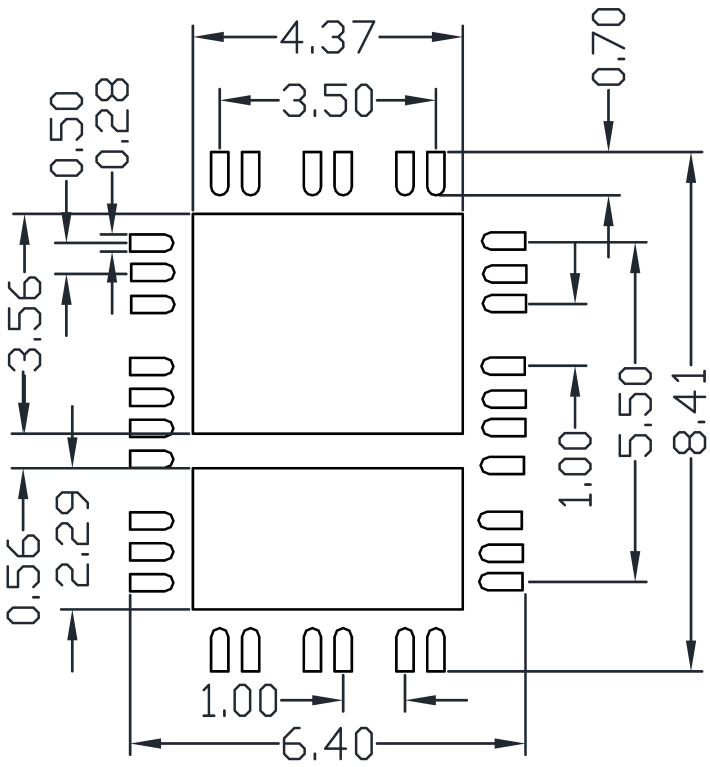


Figure 8 • PD70224 Top layer Solder Mask, Solder Paste and Vias Recommended PCB Layout (mm)

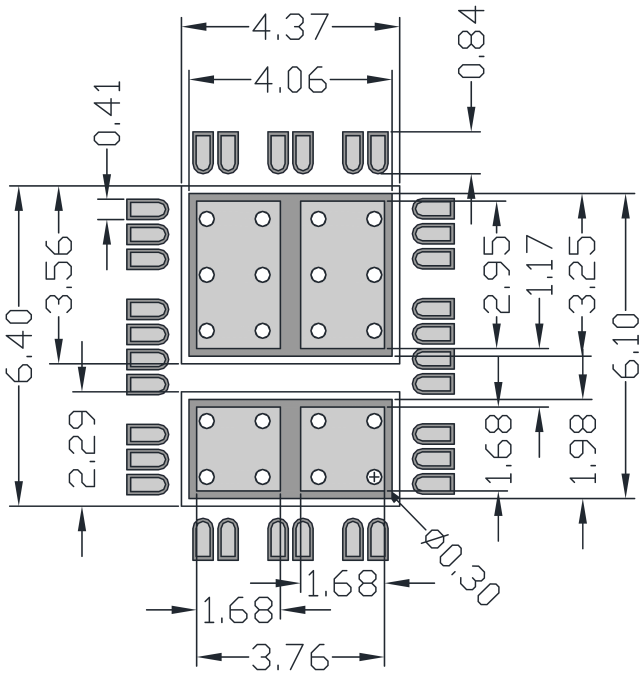
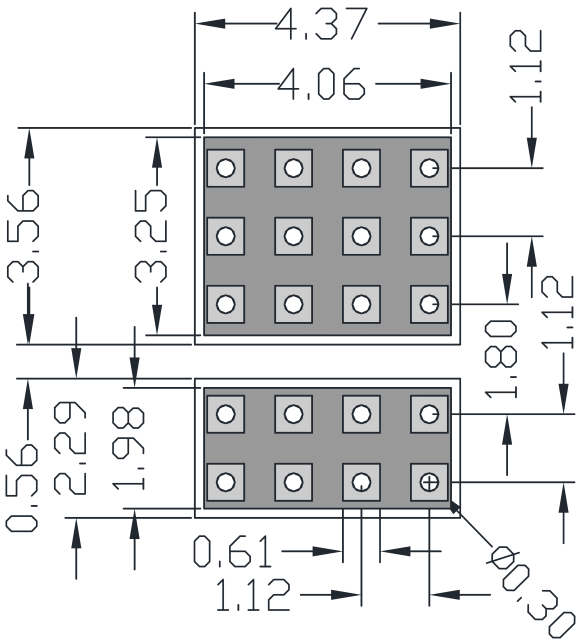


Figure 9 • PD70224 Bottom layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)



7 Application Information

PD70224 application is described in the following paragraph.

7.1 Peripheral devices

PD applications utilizing PD70224 IC should use 1nF/100V ceramic capacitor at Bridge A inputs and at Bridge B inputs.

A unidirectional 58V TVS should be placed between device output pins.

An 10K ohm resistor should be placed on SUPP_SA and SUPP_SB lines between PD70224 and PD70210A device.

When WA_EN function is not used connect WA_EN pin to OUTN Pin.

When WA_EN function is used connect a 10V/100nF capacitor between WA_EN pin and OUTN Pin.

The Devices are presented in Figure 6 and Figure 7.

7.2 Operation with an External DC Source

PD applications utilizing PD70224 IC may be operated with an external power source (DC wall adaptor). There are two cases of providing power with an external source, the cases are presented in the figures.

1. External source connected to application's low voltage supply rails. External source voltage level is dependent on DCDC output characteristics. This connection is not affected by the PD70224 use.
2. External source connected to PD device output connection toward the application (VPP to VPNOUT). External source voltage level is dependent on DCDC input requirements.

Figure 10 • External Power Input Connected to Application Supply Rails

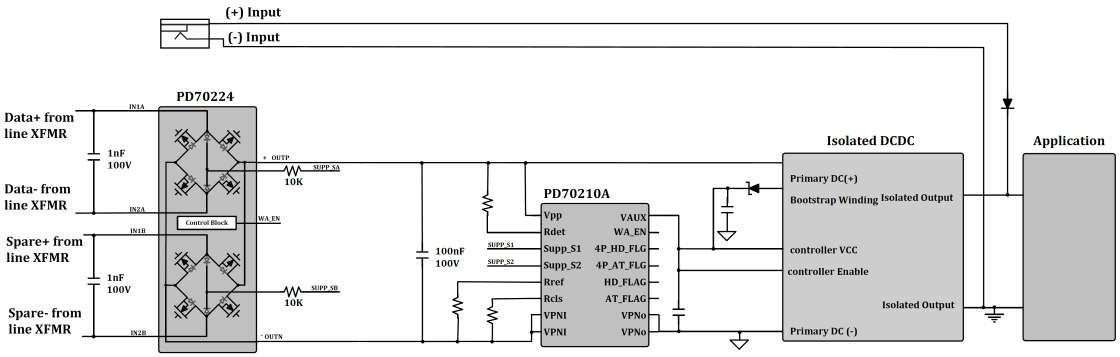
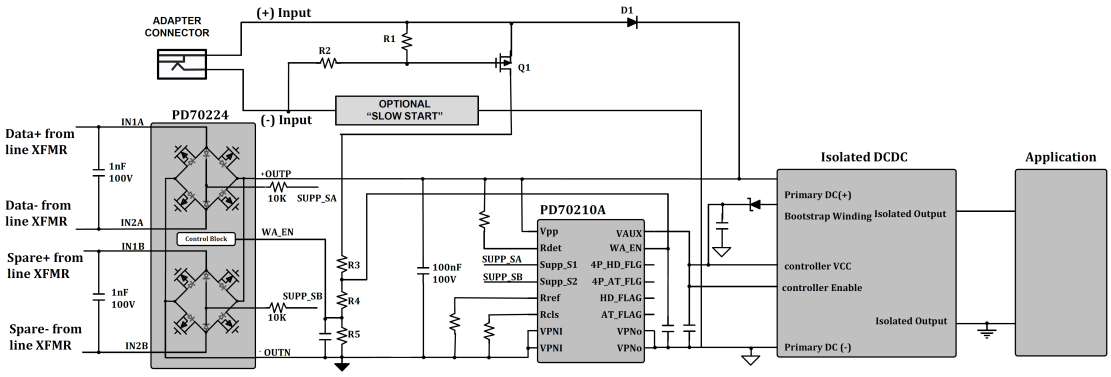


Figure 11 • External Power Input Connected to PD70210A Output



Note: In Figure 10 and Figure 11 protection is not shown - please refer to the Application Note “Design for PD System Surge Immunity " for recommended protection scheme.

External Source Connected to PD Device Output

PD70224 WA_EN pin will be used for protecting the PSE when an external adapter is connected.

In this mode the risk to PSE side exists, when a higher voltage external adapter is hot connected to the system.

When WA_EN input voltage is higher than its threshold level, PD70224 internal FETs are disabled, converting the device into standard diode bridge.

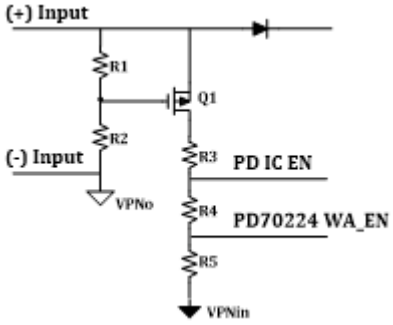
An optional “slow start” circuit prevents adapter jack contact arcing when an adapter is “hot plugged” by limiting its surge current. For the detailed circuit refer to TN_214 “Auxiliary Power for PDs”.

The PD70210A too has a specific input pin, to disable the isolation switch, when an External adapter is connected.

In this case WA_EN resistors divider depends on the “turn off” threshold of the PD70210A and of PD70224.

Zooming into the resistors to be selected in external adapter connection.

Figure 12 • External Power Input Resistors Dividers



R1 and R2 sets a rough threshold for PFET Q1 enable, to detect whether external adapter exists or not. It should be set to be lower threshold than PD70224 and PD70210A disable levels.

R3, R4 and R5 sets PD70210A disable threshold and PD70224 disable threshold.

PD70210A disable threshold should be set so that it will always be lower than PD70224 disable threshold.

1 Volt is a good choice for the margin between the two.

So, in case of 44V-57V external adapter, the disable setting can be selected as follows:

PFET enable threshold = 35V.

PD70224 disable threshold = 43V.

R1 and R2 setting should be so that the value of Q1 VGS < 20V at max voltage condition of external adapter.

While external adapter voltage is above 35V, Q1 will be above its VGSth value.

$$VGS = Vext\_adapter \times \frac{R1}{R1 + R2}$$

Suppose VGSth is 3.5V thus we will set VGS=5V.

R1 is selected as 2KΩ.

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

Using R1=2KΩ, Vext_adapter=30V and VGS= maximum VGS_{th} =3.5V. we get R2 value.

$$R2 = 15K\Omega$$

$$= PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4}{(R3 + R4)}$$

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

R3, R4 and R5 are set using the following two equations:

$$(I) \qquad PD70224\_Wa\_en = Vext\_adapter\_PD70224 \text{ x } \frac{R5}{(R3+R4+R5)}$$

$$(II) \qquad PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4+R5}{(R3+R4+R5)}$$

Set R3, R4 and R5 up to few KΩ.

At equation (I) set Vext_adapter_PD70224 =44V and from PD70224 data sheet PD70224 _WA_EN=1. 35V.

At equation (II) set Vext_adapter_PD70210A=(minimum Vext_adapter_PD70224 -1V) and from PD_IC data sheet PD70210A_WA_EN=2.4V.

R5 is selected as 620.

Solving the two equations plus accuracy and verifying that PD70210A is always disconnected before PD70224, we get the optimum resistors values for an adapter of adapter of 36V and above.

$$R3 = 15K\Omega$$

$$R4 = 820\Omega$$

$$R5 = 620\Omega$$

7.3 Design Example

Next four figures illustrates the layout of PD70224 EVB evaluation board for reference.

The board is two layers PCB. U2 is PD70224.

This board can be ordered from Microsemi.

Figure 13 • PD70224 EVB PCB Silk Top

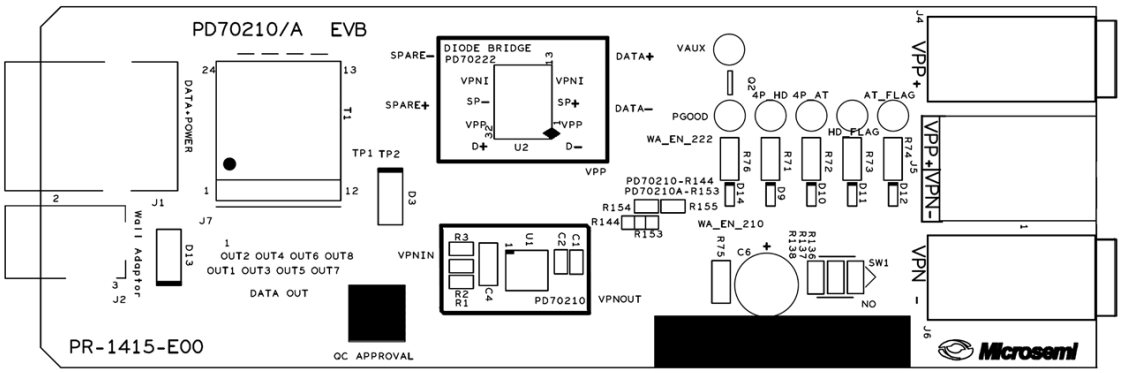


Figure 14 • PD70224 EVB PCB Silk Bottom

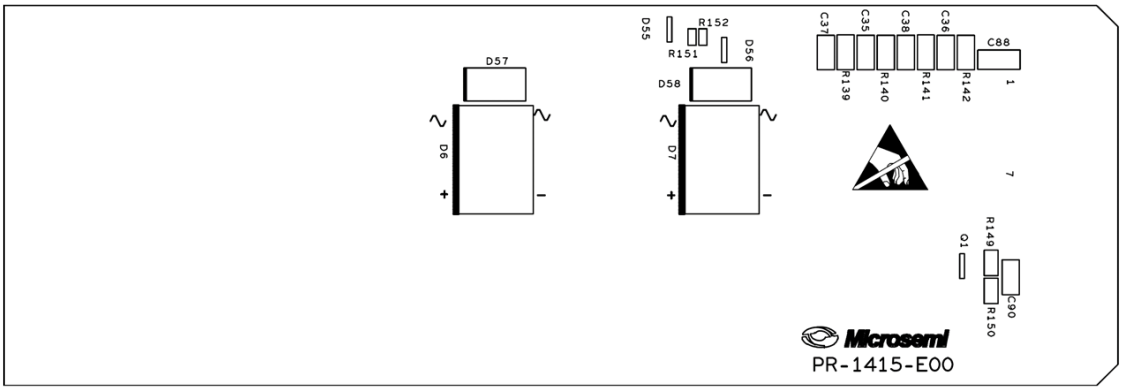


Figure 15 • PD70224 EVB PCB Top Copper

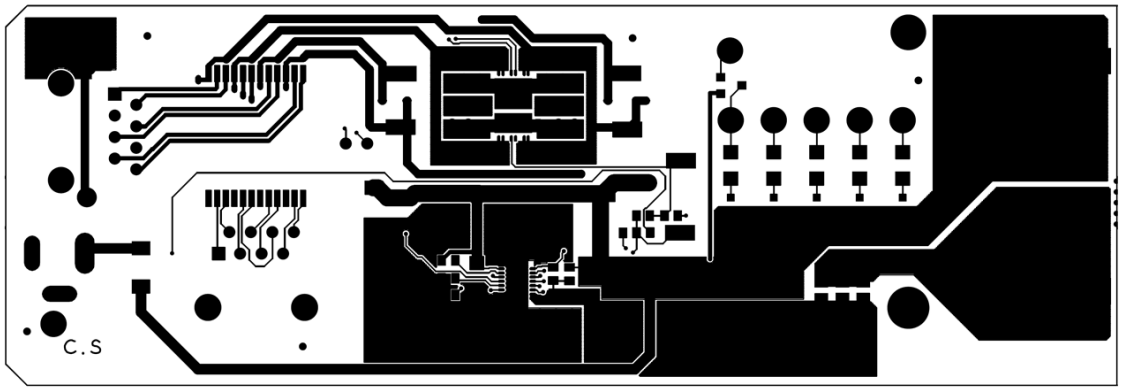
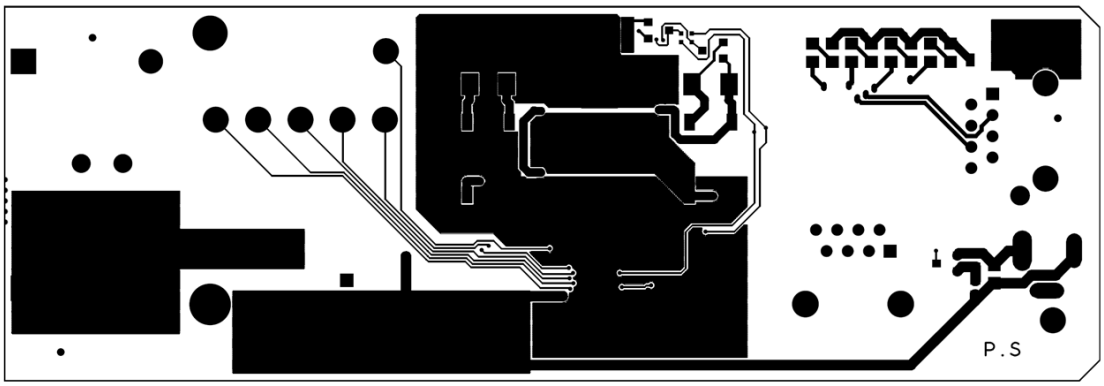


Figure 16 • PD70224 EVB PCB Bottom Copper



8 Ordering Information

The following table lists the ordering information of the PD70224 device.

Table 7 • Ordering Information

Part Number	Ambient Temperature	Type	Package	Packaging Type	Part Marking
PD70224ILQ	–40 °C to 85 °C	RoHS compliant, Pb-free, MSL3	MLP-Quad (40 lead)	Bulk/Tube	Microsemi Logo PD70224 ZZ e3[1] YYWWNNN[2]
PD70224ILQ-TR				Tape and reel	

1. ZZ e3: ZZ = Random character with no meaning, e3 = Second level interconnect.
2. 2. YY = Year, WW = Week, NNN = Trace code.

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