Description

The configurator in-system programming cable (ISP cable) is a PC-only based cable that attaches to the parallel port of a computer. This cable can be used to download and verify configuration data cascading up to 8 devices. This cable allows designers to quickly and economically program Atmel's family of AT17 configuration memories. It also provides support for new devices in the AT17 family prior to third-party programmer support being available. Therefore, it is a truly portable solution that allows engineers to work from their lab bench or office.

Supported Devices

The AT17 series configurators can interface with many SRAM-based FPGA families. This document is limited to example implementations for the following families:

- Atmel – AT94K(FPSLIC), AT40K, AT6K
- Xilinx – XC4000, XC5200, Spartan®, Spartan2, Virtex®, VirtexE
- Altera – EPF6K, EPF8K, EPF10K
- Cypress – Delta39K15, 39K30, 39K50, 39K100, 39K165, 39K200

Software Support

Make sure to use the latest CPS software (http://www.atmel.com/atmel/products/prod185.htm). CPS is used to program configurators and supports both the ATDH2200E programming board and this ISP cable. CPS also includes a conversion utility which supports Cypress, Xilinx and Altera file formats. The software, in conjunction with Atmel ISP cable, can be used to download an Atmel, Cypress, Xilinx or Altera programming file directly to Atmel's configurator(s).

- CPS – Configurator Programming System
- GUI Bbased Interface
- Supports Windows® 95/98/2000 and Windows NT®
- Supports up to 8 devices
- Supports programming reset polarity
- Verification routines to validate programming
- Accepts HEX, MCS, POF, RBF, HXU and BST file formats
- Online help
- Ability to enable or disable internal oscillator

For specific information on using the CPS software, refer to the *ATDH2200E Programming Kit User Guide*.
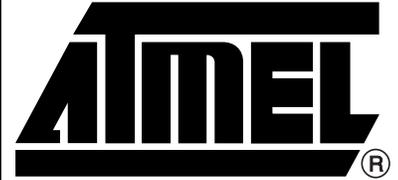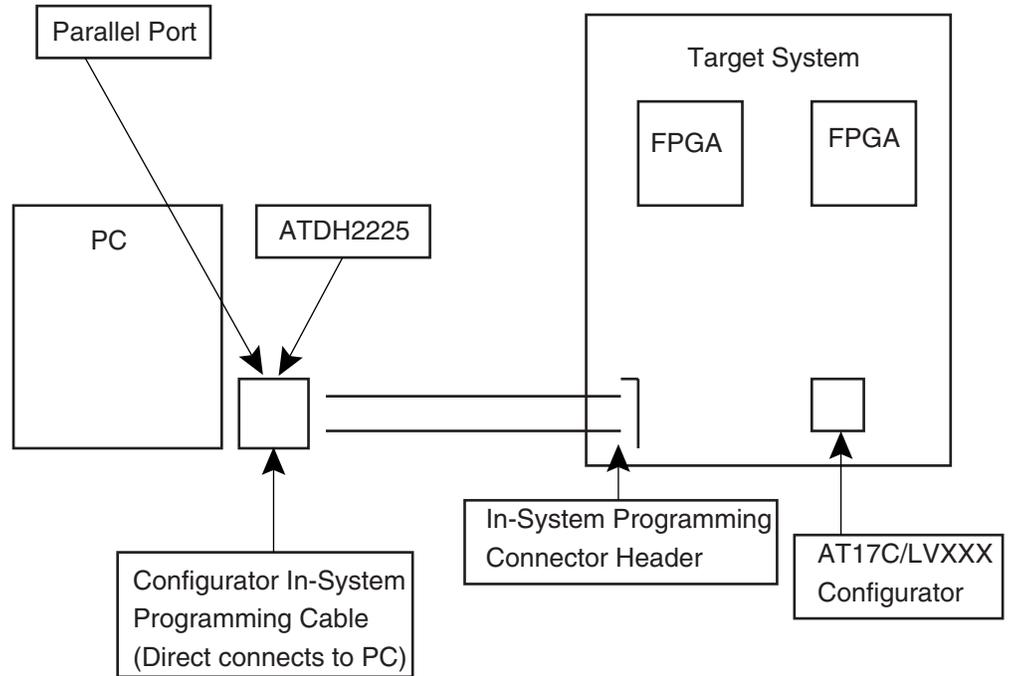
In-System Programming Cable

**ATDH2225 FPGA Configuration EEPROM Memory**

Connecting Cable to Target System

The cable draws its power from the target system through VCC and GND. Therefore, power to the cable, as well as to the target FPGA, must be stable. Do not connect any signals before connecting VCC and GND. Connect the programming dongle to your printer parallel port. Connect the other end with 10-pin header to your target system (Figure 1). Your target system should have the 10-pin header pin layout as follow in order to match the download cable (Figure 2). The pin 9 of the 10-pin header on the target system is a key pin; therefore, it is cut off. The control signals generated by the software are fed to the header. The programming algorithms written by Atmel can be used to program an AT17 device in-system.

Figure 1. In-System Programming Application

**Figure 2.** In-System Programming Header
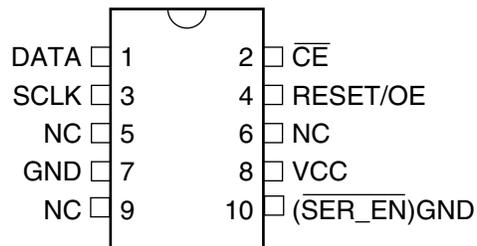
Table 1. 10-pin Header Pin Location on Target Board

1(DATA)	2($\overline{CE}$)
3(SCLK)	4(RESET/OE)
5(SW1)	6(SW2)
7(GND)	8(VCC)
9(NC)	10($\overline{SER\_EN}$/GND)

Notes: 1. Pin 10 activates "SER_EN" on target board.
2. Pin 9 is the polarizing pin (cut off).
3. The 10-pin header is 0.1' spacing

Pin 5 and Pin 6 of the 10-pin header are the two signals which able to decode for cascading up to 8 devices. The latest CPS software has the ability to control the 2 signals SW1, SW2 and by using the A2 pin of the device, you can select up to 8 devices. Therefore, you could use a 2-to-4 decoder to cascade 8 devices using our existing ISP circuit (see Figure 3).

Figure 3. ISP of Cascaded AT17C/LV002s in AT40K FPGA Applications
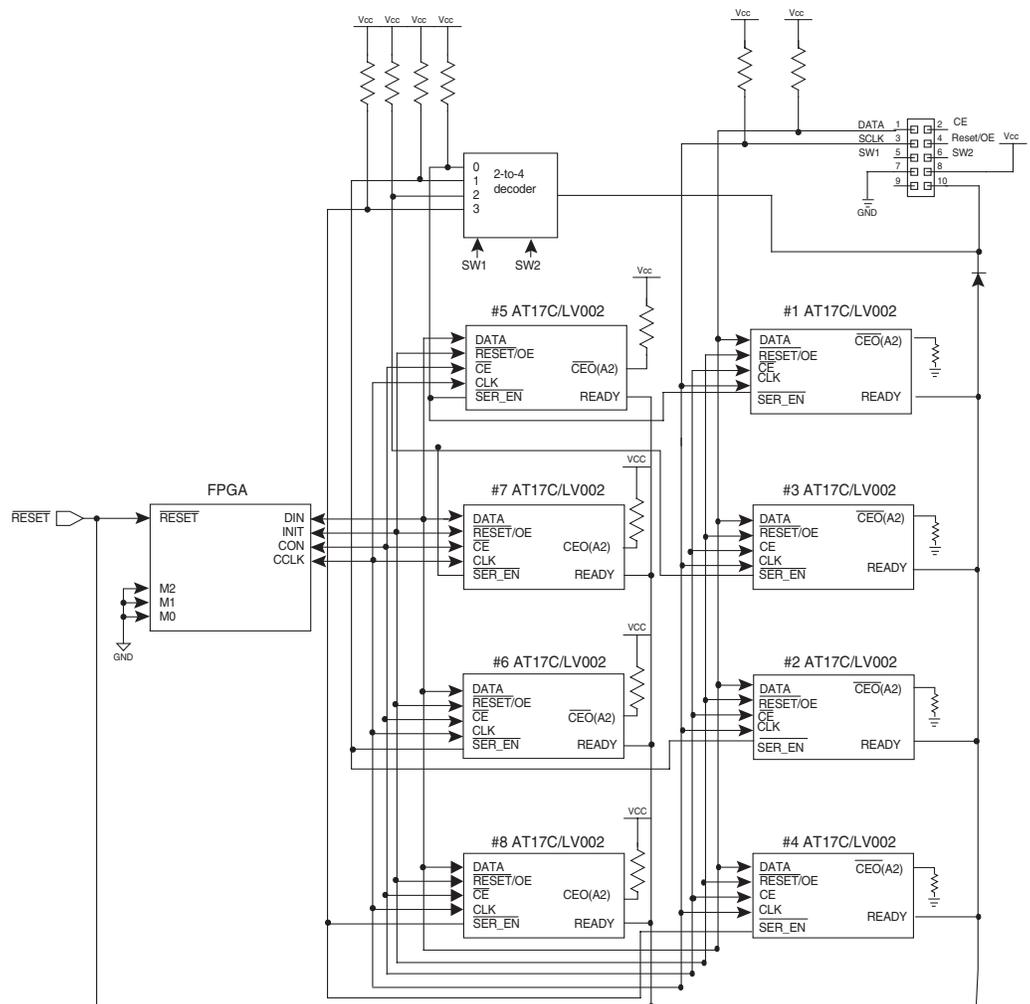
Table 2. 2 Devices

Device	A2
Device #1	pull down
Device #2	pull up

Note: No additional logic required, SW1 and SW2 not used.

Table 3. 4 Devices

Device	SW1	A2
Device #1	0	pull down
Device #2	1	pull down
Device #3	0	pull up
Device #4	1	pull up

Note: SW1 and some additional logic required for selecting up to 4 devices.

Table 4. 8 Devices

Device	SW1	SW2	A2
Device #1	0	0	pull down
Device #2	0	1	pull down
Device #3	1	0	pull down
Device #4	1	1	pull down
Device #5	0	0	pull up
Device #6	0	1	pull up
Device #7	1	0	pull up
Device #8	1	1	pull up

Note: SW1, SW2 and some additional logic required for selecting up to 8 devices.

Table 5. For 020 Max. is 4 Devices

Device	SW2	SW1
Device #1	0	0
Device #2	0	1
Device #3	1	0
Device #4	1	1

Note: 2 to 4 devices and some additional logic required for selecting up to 4 devices.

The AT17C/LV020 device is implemented using two 1-Mb Configurator EEPROMs in a multi-chip module. The A2 pin of the first internal 1Mb is set to Low by the internal pull-down circuitry. An external 4.7 kΩ pull-up must be connected to the A2 pin of the second internal 1Mb in order to program the second device. To work with the AT17C/LV020 devices, A2 should always have a pull up on the target system. The CPS software will implement the correct A2 value to program both internal devices. In fact, to program an AT17C/LV020 is just like programming two 1-Mb Configurator EEPROMs in casacade configuration.

ATDH2225 FPGA

Due to the fact that the AT17C/LV002 device is a single-die solution, an external pull-up or pull-down resistor can be connected to the A2 pin in order to program the data to the device. As long as the software A2 setting is matched with the hardware A2 pin setting, the data can be programmed to the device.

The tables on page 4 allow you to select any device out of the 8 devices, which can work with the ISP download cable. The circuit is limited to example implementation for the Atmel vendor only. It is the same idea for Xilinx and Altera applications. In addition, user can still use the existing ISP circuit, which from the 2-megabit cascade document with the same ISP download cable.

Related Documents

ATDH2200E Programming Kit User Guide

AT17C/LV device datasheet

Programming Specification for Atmel's FPGA Serial Configuration Memories

Technical Support

Use the ATDH2200E Programming Kit User Guide

Review the Configurator FAQ at www.atmel.com

Contact your local Atmel representative or distributor who provided the ISP download cable for technical support

Contact your local Atmel FAE (available at most sales offices)

Contact the Atmel configurator technical support hotline:

  (408) 436-4119 (9:00 AM - 6:00 PM PST)

E-mail Atmel configurator technical support: configurator@atmel.com
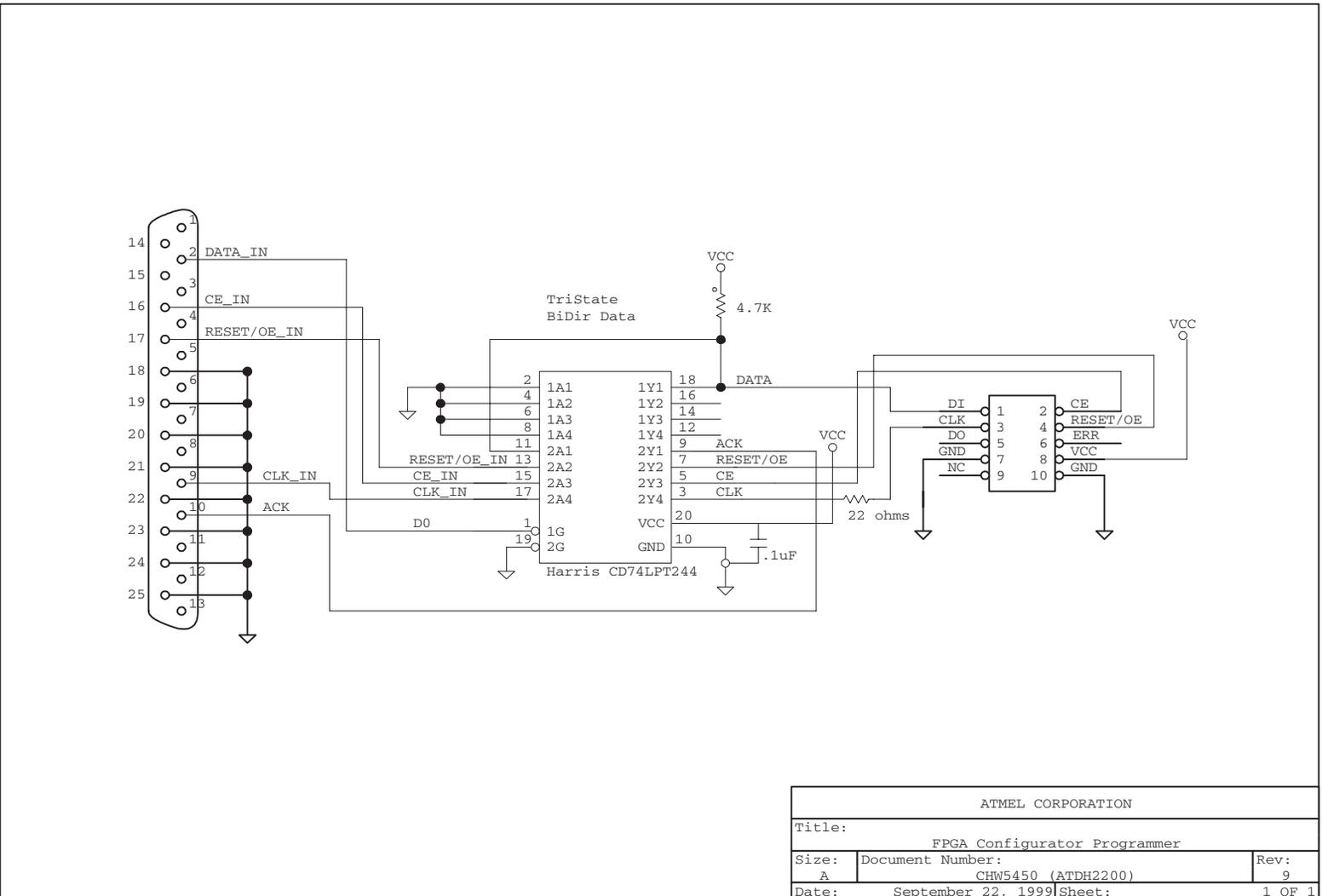
Fax your inquires to "Configurator Tech Support" at:

  (408) 487-2637

ATDH2225 FPGA

Schematic

This cable would perform ISP without the use of the ATDH2200 board. The software used would be CPS.

DATA_IN

CE_IN

RESET/OE_IN

CLK_IN

ACK

14 15 16 17 18 19 20 21 22 23 24 25

1 2 3 4 5 6 7 8 9 10 11 12 13

VCC

4.7K

TriState
BiDir Data

2 1A1   1Y1 18   DATA
4 1A2   1Y2 16
6 1A3   1Y3 14
8 1A4   1Y4 12
11
2A1   2Y1   9   ACK
RESET/OE_IN 13 2A2   2Y2   7   RESET/OE
CE_IN   15 2A3   2Y3   5   CE
CLK_IN   17 2A4   2Y4   3   CLK
D0   1 1G   VCC 20
             19 2G   GND 10

VCC

.1uF

22 ohms

Harris CD74LPT244

DI   1   2   CE
CLK   3   4   RESET/OE
DO   5   6   ERR
GND   7   8   VCC
NC   9   10 GND

VCC

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