Click here for production status of specific part numbers.

MAX98360A/B/C/D

Tiny, Cost-Effective, Plug-and-Play Digital Class-D Amplifier

General Description

The MAX98360A/B/C/D is an easy-to-use, low-cost, digital pulse-code modulation (PCM) input Class-D amplifier that provides industry-leading, Class-AB audio performance with Class-D efficiency. The digital audio interface automatically recognizes different PCM and TDM clocking schemes which eliminates the need for I²C programming. Simply supply power, LRCLK, BCLK, and digital audio to generate audio. Furthermore, a novel pinout allows customers to use the cost-effective WLP package with no need for expensive vias.

The digital audio interface is highly flexible. The devices support I²S, left-justified, and 8-channel time division multiplexed (TDM) data formats. The digital audio interface accepts 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz sample rates. Data words can be 16-bit, 24-bit, or 32-bit in I²S and left-justified modes and 16-bit or 32-bit in TDM mode.

Digital audio interface input thresholds are ideal for interfacing to 1.2V and 1.8V logic. The devices can tolerate logic input voltages up to 5.5V.

The MAX98360A and MAX98360B have fast 1ms turn-on times while the MAX98360C and MAX98360D ramp the volume over 13ms during turn-on and turn-off.

The devices eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count. The devices also feature a very high wideband jitter tolerance (12ns, typ) on BCLK and LRCLK to provide robust operation.

Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class-D devices and reduces the component count of the solution.

The devices are specified over the -40°C to +85°C temperature range.

Applications

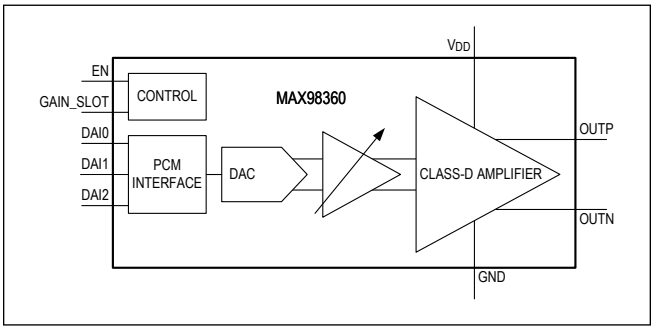
- Single Li-ion Cell/5V Devices
- Smart Speakers
- Notebook Computers
- IoT Devices
- Gaming Devices (Audio and Haptics)
- Smartphones
- Tablets
- Cameras

Benefits and Features

- Simple Plug-and-Play Design
- Single-Supply Operation (2.5V to 5.5V)
- 3.2W Output Power into 4Ω at 5V
- 2.2mA Quiescent Current
- 1ms Turn-On Time (for MAX98360A and MAX98360B)
- 92% Efficiency (R_L = 8Ω, THD+N = 10%)
- 10μV_{RMS} Output Noise
- 110dB Dynamic Range
- Low 0.009% THD+N at 1kHz
- No MCLK Required
- Sample Rates of 8kHz to 96kHz
- Supports Left, Right, or (Left/2 + Right/2) Output in I²S and Left-Justified Modes
- Sophisticated Edge Rate Control Enables Filterless Class-D Outputs
- 81dB PSRR at 217Hz
- 1.5μA Standby Current Allows Elimination of GPIO for EN Pin
- Low RF Susceptibility Rejects TDMA Noise from GSM Radios
- Class-D Switching Frequency Trimmed to 5% for Better EMI Planning
- Extensive Click-and-Pop Reduction Circuitry
- Robust Short-Circuit and Thermal Protection
- Available in Space-Saving Package: 9-Pin WLP (0.4mm Pitch) or 10-Pin FC2QFN (0.5mm Pitch)
- 3.69mm² Solution Size for WLP With A Single Bypass Capacitor

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



maxim integrated™

Absolute Maximum Ratings

V_{DD}, DAI0, DAI1, and DAI2 to GND..... -0.3V to +6V
All other pins to GND..... -0.3V to V_{DD} + 0.3V
Duration of OUTP or OUTN short circuit to GND or V_{DD}..... Continuous
Duration of OUTP short to OUTN..... Continuous

Continuous power dissipation (T_A = +70°C) WLP (derate 13.7mW/°C above +70°C) 1096mW
Junction temperature .....+150°C
Operating temperature range.....-40°C to +85°C
Storage temperature range.....-65°C to +150°C
Soldering temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	N91E1+1
Outline Number	21-100371
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	73°C/W
Junction to Case (θ_{JC})	N/A

FC2QFN

Package Code	F102A2F+1
Outline Number	21-100376
Land Pattern Number	90-100123
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	73°C/W
Junction to Case (θ_{JC})	41°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 5V, V_{GND} = 0V, gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM						
Supply Voltage Range	V_{DD}	Guaranteed by PSRR test	2.5		5.5	V
Undervoltage Lockout	V_{UVLO}		1.5	1.8	2.3	V
Quiescent Current	I_{VDD}	T_A = +25°C		2.4	3.35	mA
		T_A = +25°C, V_{DD} = 3.7V		2.2	2.85	
Shutdown Current	I_{SHDN}	EN = 0V, T_A = +25°C		0.014	0.5	µA
Standby Current	I_{STNDBY}	EN = 1.8V, T_A = +25°C, all DAIn pins at 0V		1.5	3	µA
		EN = 1.8V, T_A = +25°C, no toggling on DAIn pins			49	
Turn-On Time	t_{ON}	Time from shutdown or standby to full gain audio out, MAX98360A and MAX98360B		1	1.2	ms
		Time from shutdown or standby to full gain audio out, MAX98360A and MAX98360B, f_S = 8kHz		1.8		
		Time from shutdown or standby to full gain audio out, MAX98360C and MAX98360D			13	
Thermal Shutdown Temperature				150		°C
Thermal Shutdown Recovery Hysteresis				18		°C
CLASS-D AMPLIFIER						
Output Offset Voltage	V_{OS}	T_A = +25°C	-2.5	±0.3	+2.5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, into Standby or Shutdown		-72		dBV
		Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, out of Standby or Shutdown		-66		

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞, DC, V_{DD} = 2.5V to 5.5V	66	81		dB
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 217Hz, 200mV_{PP} ripple		81		
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 1kHz, 200mV_{PP} ripple		81		
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 10kHz, 200mV_{PP} ripple		73		
Output Power	P_{OUT}	THD+N ≤ 10%, Z_{SPK} = 4Ω + 33µH		3.2		W
		THD+N ≤ 10%, Z_{SPK} = 8Ω + 33µH		1.8		
		THD+N ≤ 10%, Z_{SPK} = 8Ω + 33µH, V_{DD} = 3.7V		0.93		
		THD+N ≤ 1%, Z_{SPK} = 4Ω + 33µH		2.5		
		THD+N ≤ 1%, Z_{SPK} = 8Ω + 33µH		1.4		
		THD+N ≤ 1%, Z_{SPK} = 8Ω + 33µH, V_{DD} = 3.7V		0.77		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 1W, T_A = +25°C , Z_{SPK} = 4Ω + 33µH		0.01		%
		f = 1kHz, P_{OUT} = 0.7W, T_A = +25°C , Z_{SPK} = 8Ω + 33µH (Note 3)		0.009	0.02	
Dynamic Range	DR	A-weighted, Z_{SPK} = 8Ω + 33µH, -60dB 1kHz output signal, normalized to full scale (THD+N = 1%), 24- or 32-bit data		110		dB
Output Noise	e_{Nd}	A-weighted, 24-bit or 32-bit data		10		μV_{RMS}
Gain (Relative to a 2.3dBV Reference Level)	A_V	I^2S or left-justified mode with GAIN_SLOT = GND, or TDM mode	11.4	12	12.6	dB
		I^2S or left-justified mode, GAIN_SLOT = unconnected	8.4	9	9.6	
		I^2S or left-justified mode, GAIN_SLOT = V_{DD}	5.4	6	6.6	
		I^2S or left-justified mode, GAIN_SLOT = V_{DD} through 100kΩ	2.4	3	3.6	
		I^2S or left-justified mode, GAIN_SLOT = GND through 100kΩ	-3.6	-3	-2.4	
Output Current Limit	I_{LIM}			2.6		A
Output Current Limit Autorestart Time				100		µs
Efficiency	η	Z_{SPK} = 8Ω + 33µH, THD+N = 10%, f = 1kHz		92		%

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response			-0.2		+0.3	dB
Class-D Switching Frequency	f_{SW}	V_{DD} = 3.0V to 5.5V	285	300	315	kHz
Spread-Spectrum Bandwidth	f_{SSM}	V_{DD} = 2.5V to 5.5V		±14		kHz
Output Stage On-Resistance	R_{ON}	PMOS + NMOS (Full H-Bridge), T_A = +25°C		285		mΩ
Maximum Device to Device Phase Error		Output phase shift between multiple devices from 20Hz to 20kHz across all sample rates and DAI operating modes		1		deg
DAC DIGITAL FILTERS/VOICE MODE IIR LOWPASS FILTER (LRCLK < 30kHz)						
Passband	f_{PLP}	Ripple < δ_P	0.443 x f_S			Hz
		Droop < 3dB	0.446 x f_S			
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband	f_{SLP}	Attenuation > δ_S			0.464 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}	75			dB
DAC DIGITAL FILTERS/AUDIO MODE FIR LOWPASS FILTER (30kHz < LRCLK < 50kHz)						
Passband	f_{PLP}	Ripple < δ_P	0.43 x f_S			Hz
		Droop < 3dB	0.47 x f_S			
		Droop < 6.02dB	0.5 x f_S			
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband	f_{SLP}	Attenuation > δ_S			0.58 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}	60			dB
DAC DIGITAL FILTERS/AUDIO MODE FIR LOWPASS FILTER (LRCLK > 50kHz)						
Passband	f_{PLP}	Ripple < δ_P	0.24 x f_S			Hz
		Droop < 3dB	0.31 x f_S			
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband	f_{SLP}	Attenuation > δ_S			0.477 x f_S	Hz
Stopband Attenuation	δ_S	f < f_{SLP}	60			dB
DAC DIGITAL FILTERS/DIGITAL DC BLOCKING FILTER						
DC Blocking Filter -3dB Cutoff Frequency	f_C	f_S = 96kHz		3.75		Hz
		f_S = 48kHz		3.75		
		f_S = 44.1kHz		3.47		
		f_S = 8kHz		0.65		

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL I/O							
Minimum LRCLK Frequency	f_{LRMIN}	Minimum LRCLK frequency for DAI Configuration and unmuting (Note 2)		6.44	6.8	7.12	kHz
Maximum LRCLK Frequency	f_{LRMAX}	Maximum LRCLK frequency for DAI Configuration and unmuting (Note 2)		110	116	125	kHz
LRCLK Range 1	f_{S1}	(Note 2)		7.6	8	8.4	kHz
LRCLK Range 2	f_{S2}	(Note 2)		15.2	16	16.8	kHz
LRCLK Range 3	f_{S3}	(Note 2)		30.4	48	50.4	kHz
LRCLK Range 4	f_{S4}	(Note 2)		83.8	96	100.8	kHz
BCLK Periods per LRCLK Period Range 1	BL_{CLK1}	(Note 2)		29	32	36	none
BCLK Periods per LRCLK Period Range 2	BL_{CLK2}	(Note 2)		41	48	56	none
BCLK Periods per LRCLK Period Range 3	BL_{CLK3}	(Note 2)		57	64	72	none
BCLK Periods per LRCLK Period Range 4	BL_{CLK4}	(Note 2)		113	128	144	none
BCLK Periods per LRCLK Period Range 5	BL_{CLK5}	(Note 2)		225	256	288	none
Resolution		I^2S/left-justified mode			16/24/32		Bits
		TDM mode			16/32		
BCLK Frequency Range	f_{BCLK}	BCLK frequency required for DAI Configuration and unmuting (Note 2)		0.2432		25.804	MHz
BCLK High Time	t_{BCLKH}			15			ns
BCLK Low Time	t_{BCLKL}			15			ns
Maximum Low Frequency BCLK and LRCLK Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter ≤ 40kHz			0.5		ns
Maximum High Frequency BCLK and LRCLK Jitter		Maximum allowable jitter before the dynamic range has a 1dB reduction, RMS jitter > 40kHz			12		ns
Input High Voltage	V_{IH}	DAI0, DAI1, DAI2		0.84			V
		EN		1.0			
Input Low Voltage	V_{IL}	DAI0, DAI1, DAI2				0.54	V
		EN				0.24	
Input Hysteresis	V_{HYS}	DAI0, DAI1, DAI2 (Note 3)		75			mV
		EN			25		
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V, V_{DD} = 5.5V, T_A = +25°C	DAI0, DAI1, DAI2	-1		+4	µA
			EN	-1		+1	
Input Capacitance	C_{IN}				3		pF

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN to BCLK Setup Time	t_{SETUP}		10			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$		10			ns
DIN to BCLK Hold Time	t_{HOLD}		10			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$		10			ns
GAIN_SLOT COMPARATOR TRIP POINTS						
GAIN_SLOT Comparator Trip Points	V_{GAIN_SLOT4}	A_V = 6dB gain in I^2S and left-justified modes, channel 1, 3, or 7 in TDM mode	0.9 x V_{DD}		V_{DD}	V
	V_{GAIN_SLOT3}	A_V = 3dB gain in I^2S and left-justified modes	0.65 x V_{DD}		0.85 x V_{DD}	
	V_{GAIN_SLOT2}	A_V = 9dB gain in I^2S and left-justified modes, channel 2 or 6 in TDM mode	0.4 x V_{DD}		0.6 x V_{DD}	
	V_{GAIN_SLOT1}	A_V = -3dB gain in I^2S and left-justified modes	0.15 x V_{DD}		0.35 x V_{DD}	
	V_{GAIN_SLOT0}	A_V = 12dB gain in I^2S and left-justified modes, channel 0, 4, or 5 in TDM mode	0		0.1 x V_{DD}	

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

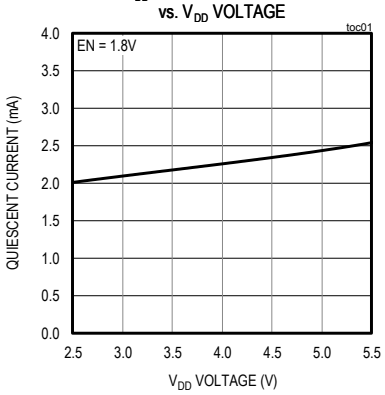
Note 2: See the *Digital Audio Interface Configuration* and *Valid Clock Frequencies* sections for more information.

Note 3: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

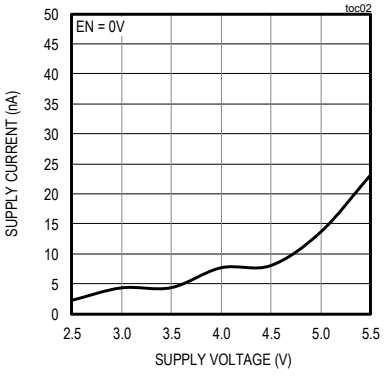
Typical Operating Characteristics

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

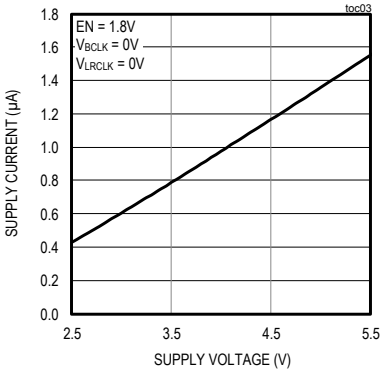
V_{DD} QUIESCENT CURRENT vs. V_{DD} VOLTAGE



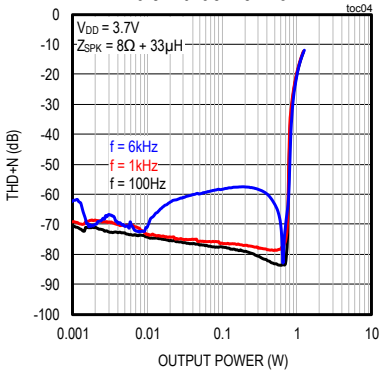
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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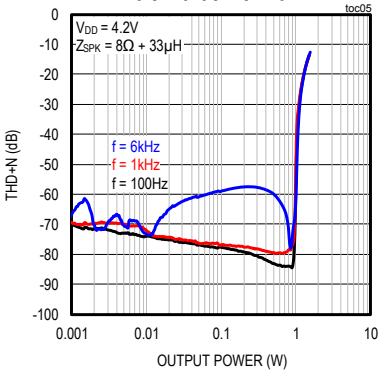

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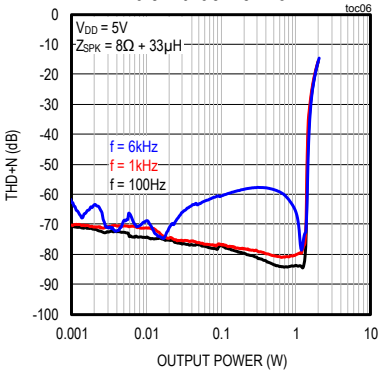

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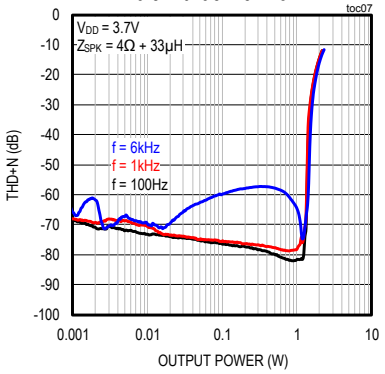

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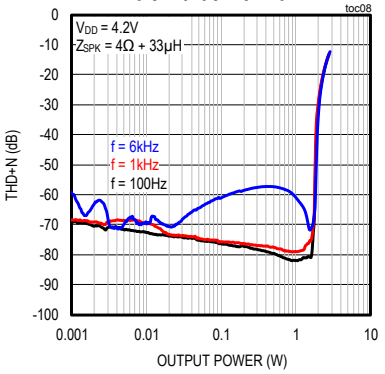

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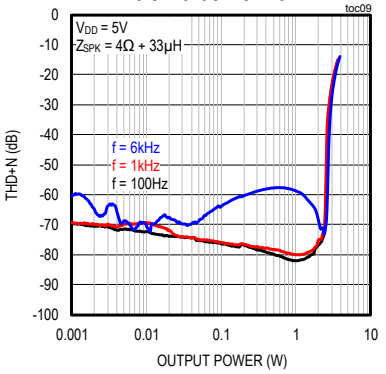
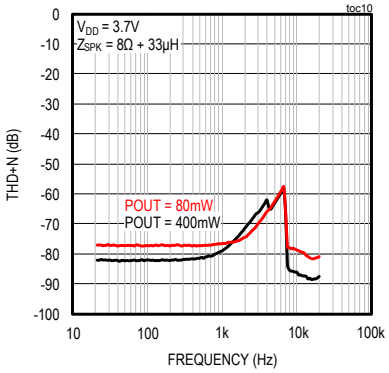


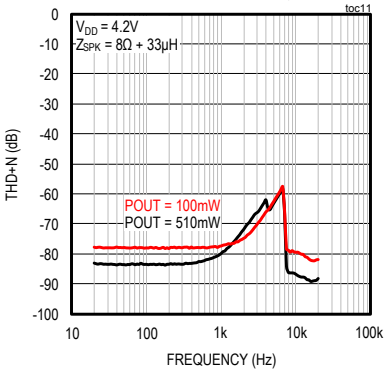
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

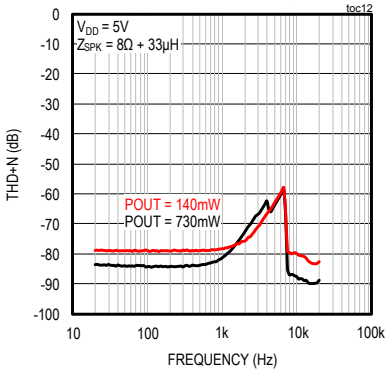
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



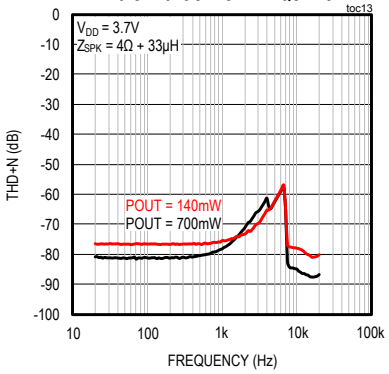
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



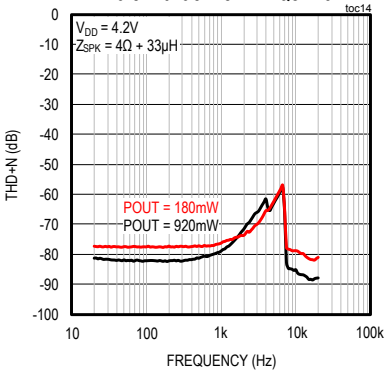
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



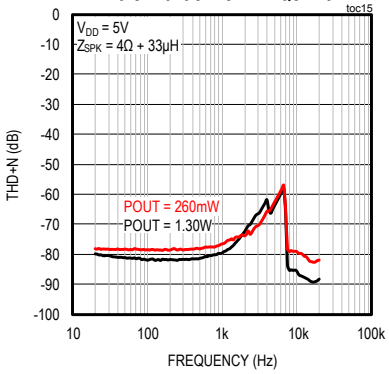
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



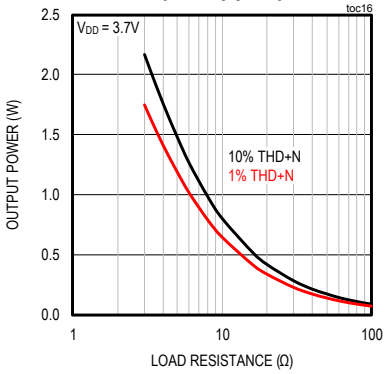
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



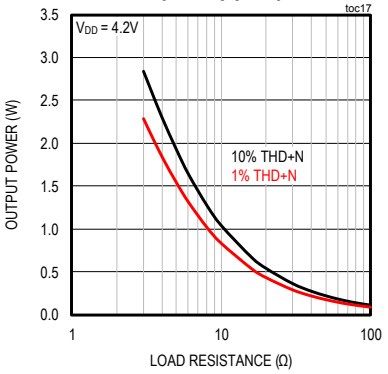
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



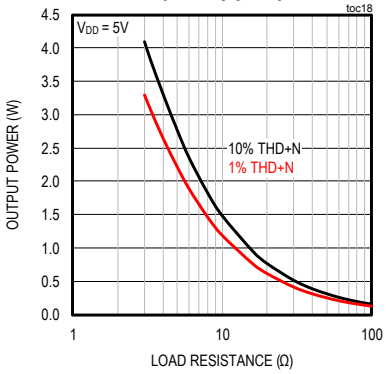
OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. LOAD RESISTANCE



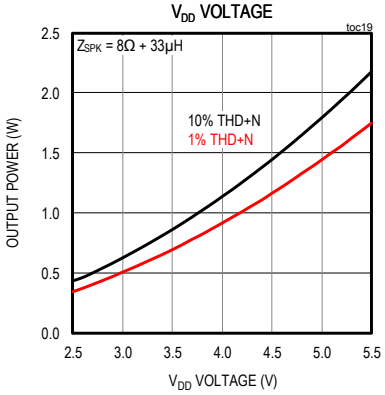
OUTPUT POWER vs. LOAD RESISTANCE



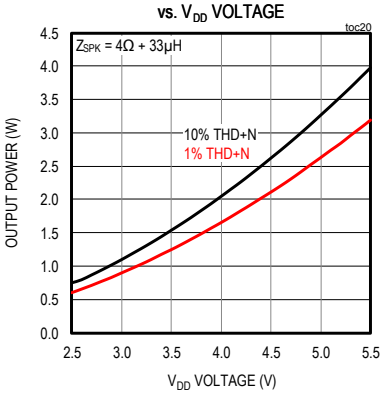
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

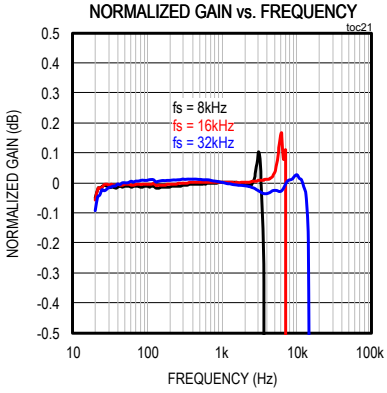
OUTPUT POWER vs. V_{DD} VOLTAGE



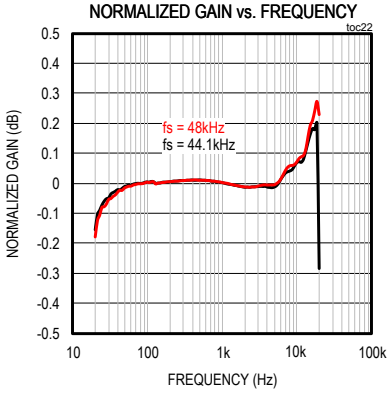
OUTPUT POWER vs. V_{DD} VOLTAGE



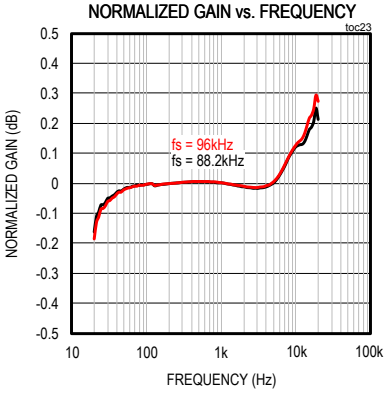
NORMALIZED GAIN vs. FREQUENCY



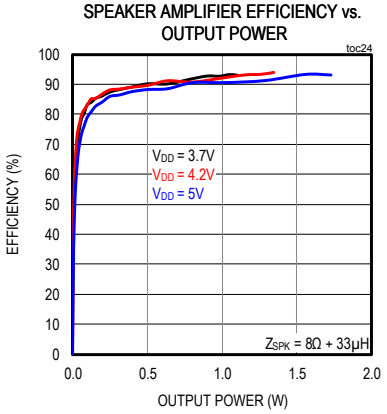
NORMALIZED GAIN vs. FREQUENCY



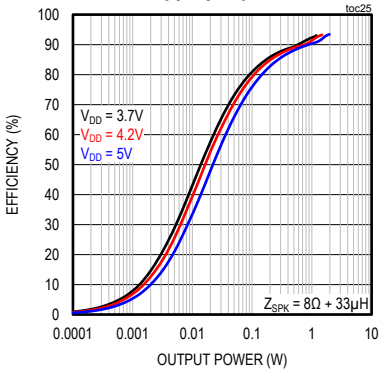
NORMALIZED GAIN vs. FREQUENCY



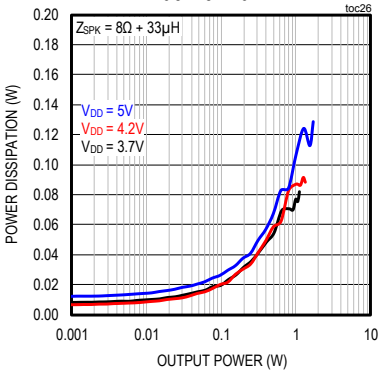
SPEAKER AMPLIFIER EFFICIENCY vs. OUTPUT POWER



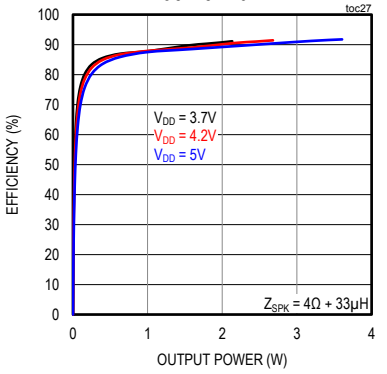
SPEAKER AMPLIFIER EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



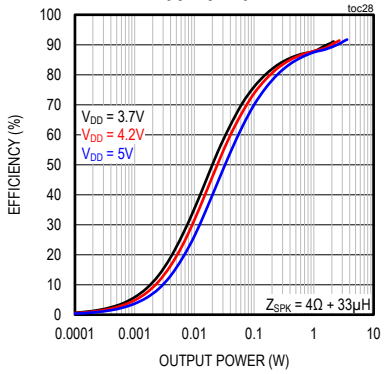
SPEAKER AMPLIFIER EFFICIENCY vs. OUTPUT POWER



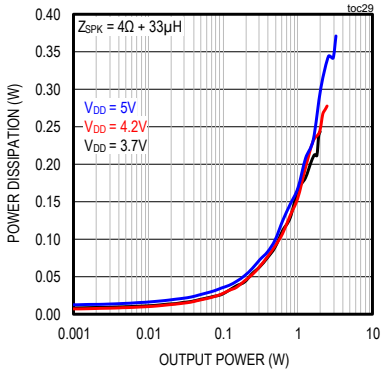
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

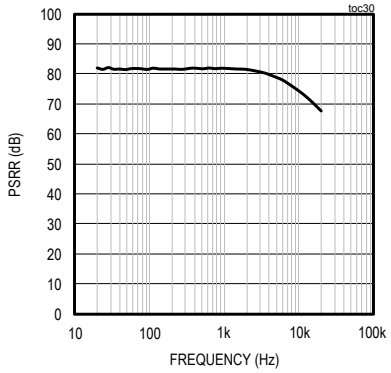
SPEAKER AMPLIFIER EFFICIENCY vs. OUTPUT POWER



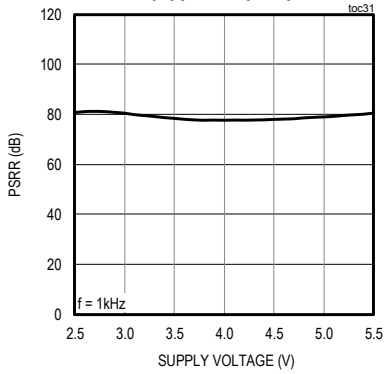
POWER DISSIPATION vs. OUTPUT POWER



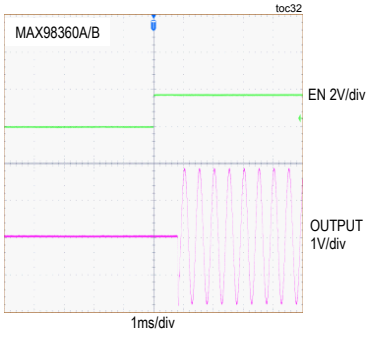
POWER-SUPPLY REJECTION RATIO vs. FREQEUNCY



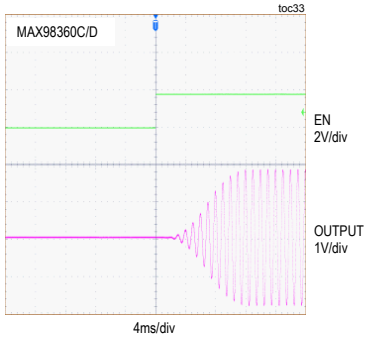
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



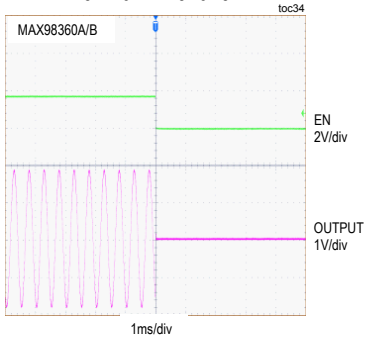
TURN-ON RESPONSE



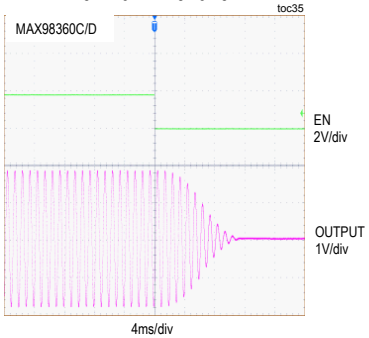
TURN-ON RESPONSE



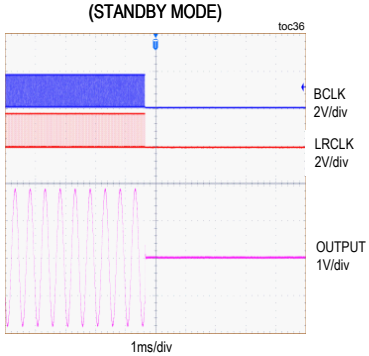
TURN-OFF RESPONSE



TURN-OFF RESPONSE



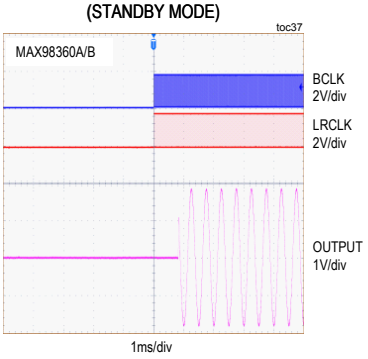
TURN-OFF RESPONSE (STANDBY MODE)



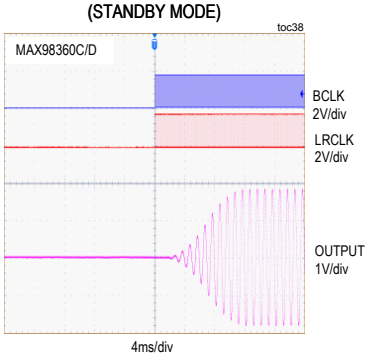
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

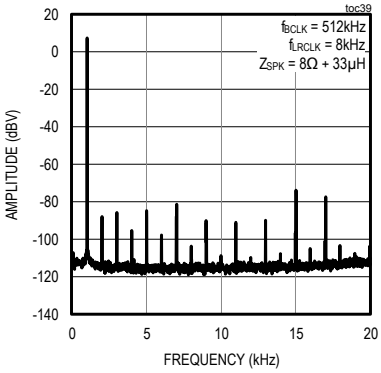
TURN-ON RESPONSE
(STANDBY MODE)



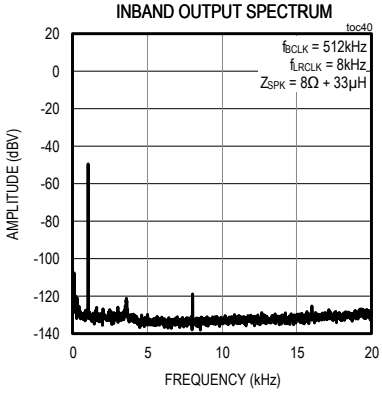
TURN-ON RESPONSE
(STANDBY MODE)



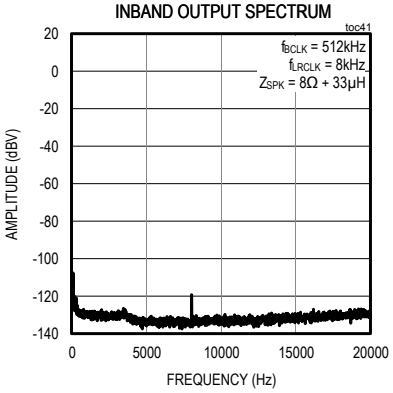
INBAND OUTPUT SPECTRUM



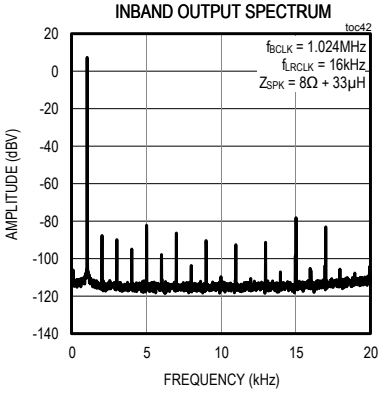
INBAND OUTPUT SPECTRUM



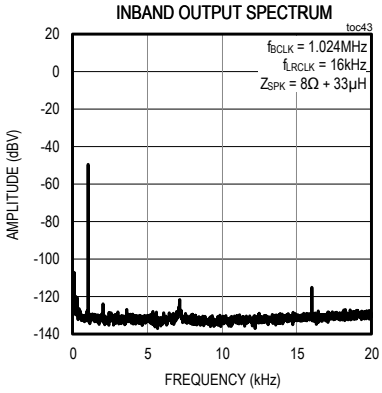
INBAND OUTPUT SPECTRUM



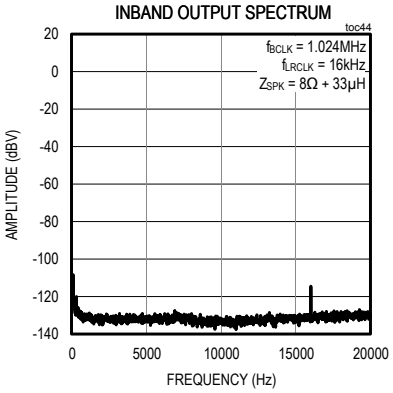
INBAND OUTPUT SPECTRUM



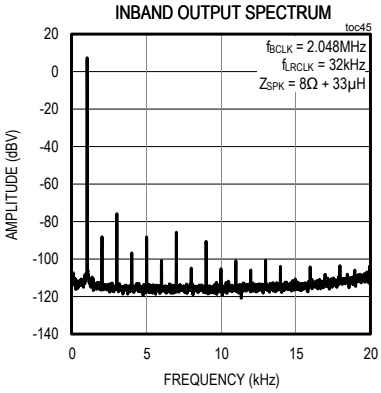
INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM



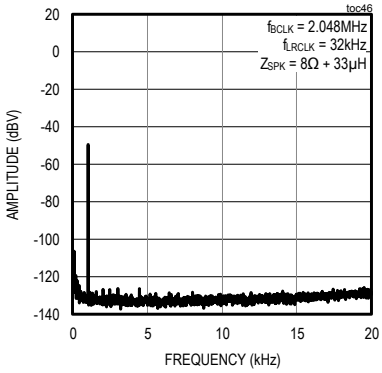
INBAND OUTPUT SPECTRUM



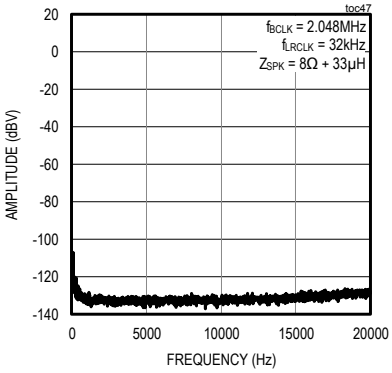
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

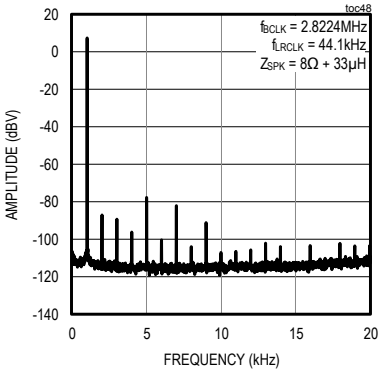
INBAND OUTPUT SPECTRUM



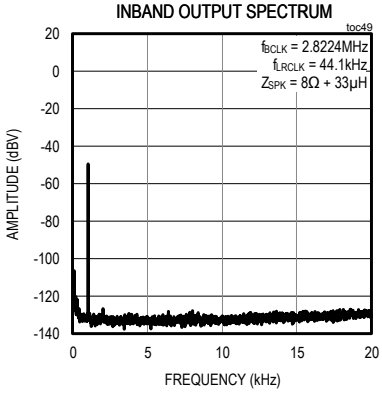
INBAND OUTPUT SPECTRUM



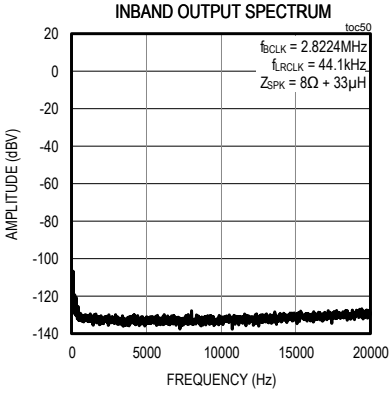
INBAND OUTPUT SPECTRUM



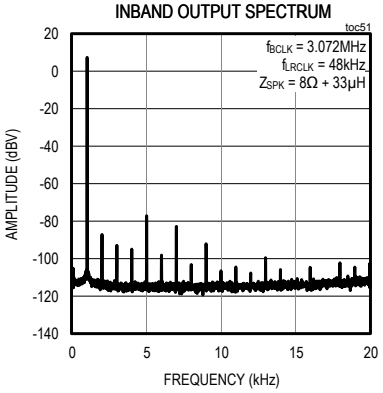
INBAND OUTPUT SPECTRUM



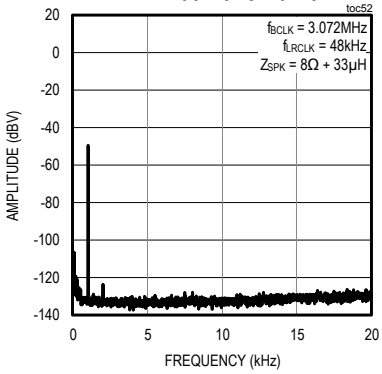
INBAND OUTPUT SPECTRUM



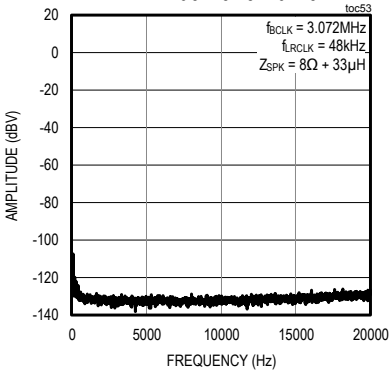
INBAND OUTPUT SPECTRUM



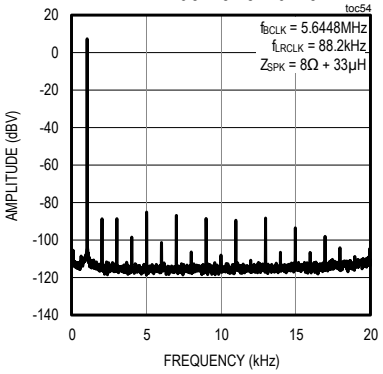
INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM



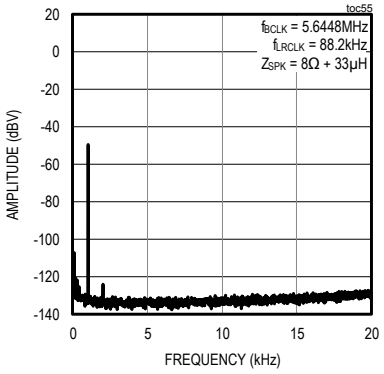
INBAND OUTPUT SPECTRUM



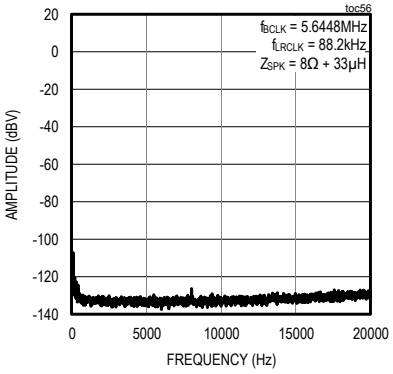
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, Gain = 12dB, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = +25°C.)

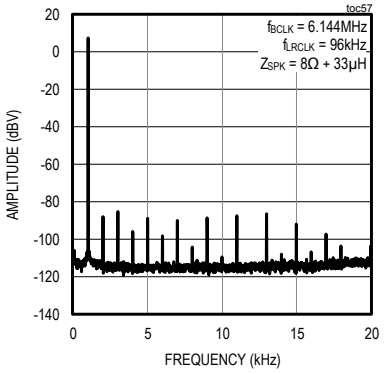
INBAND OUTPUT SPECTRUM



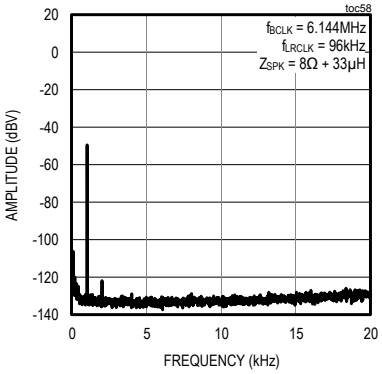
INBAND OUTPUT SPECTRUM



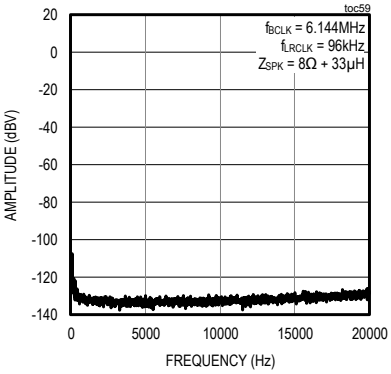
INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM

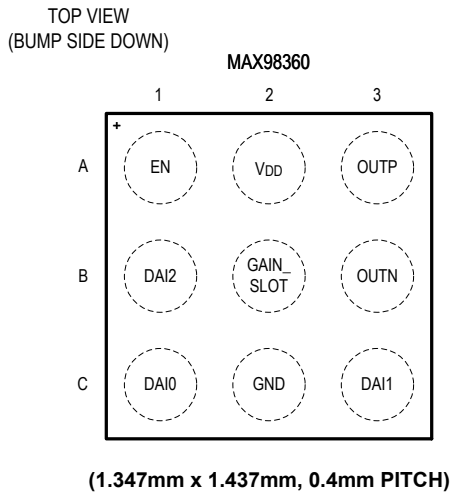


INBAND OUTPUT SPECTRUM



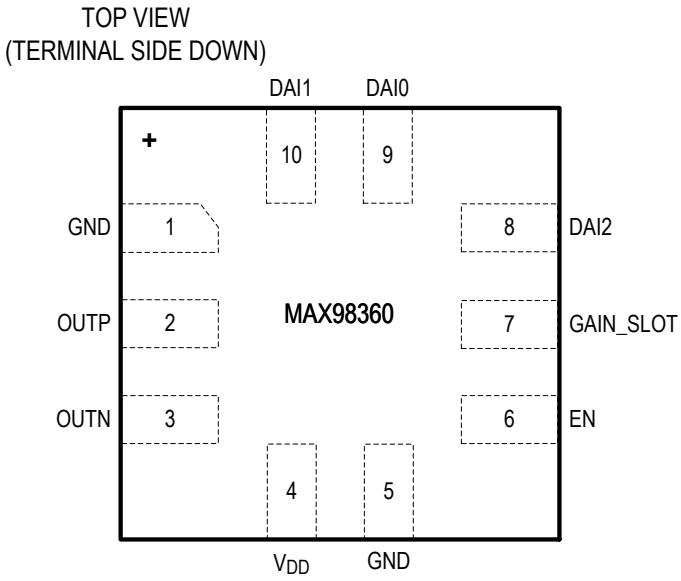
Pin Configurations

9 WLP



(1.347mm x 1.437mm, 0.4mm PITCH)

10 FC2QFN

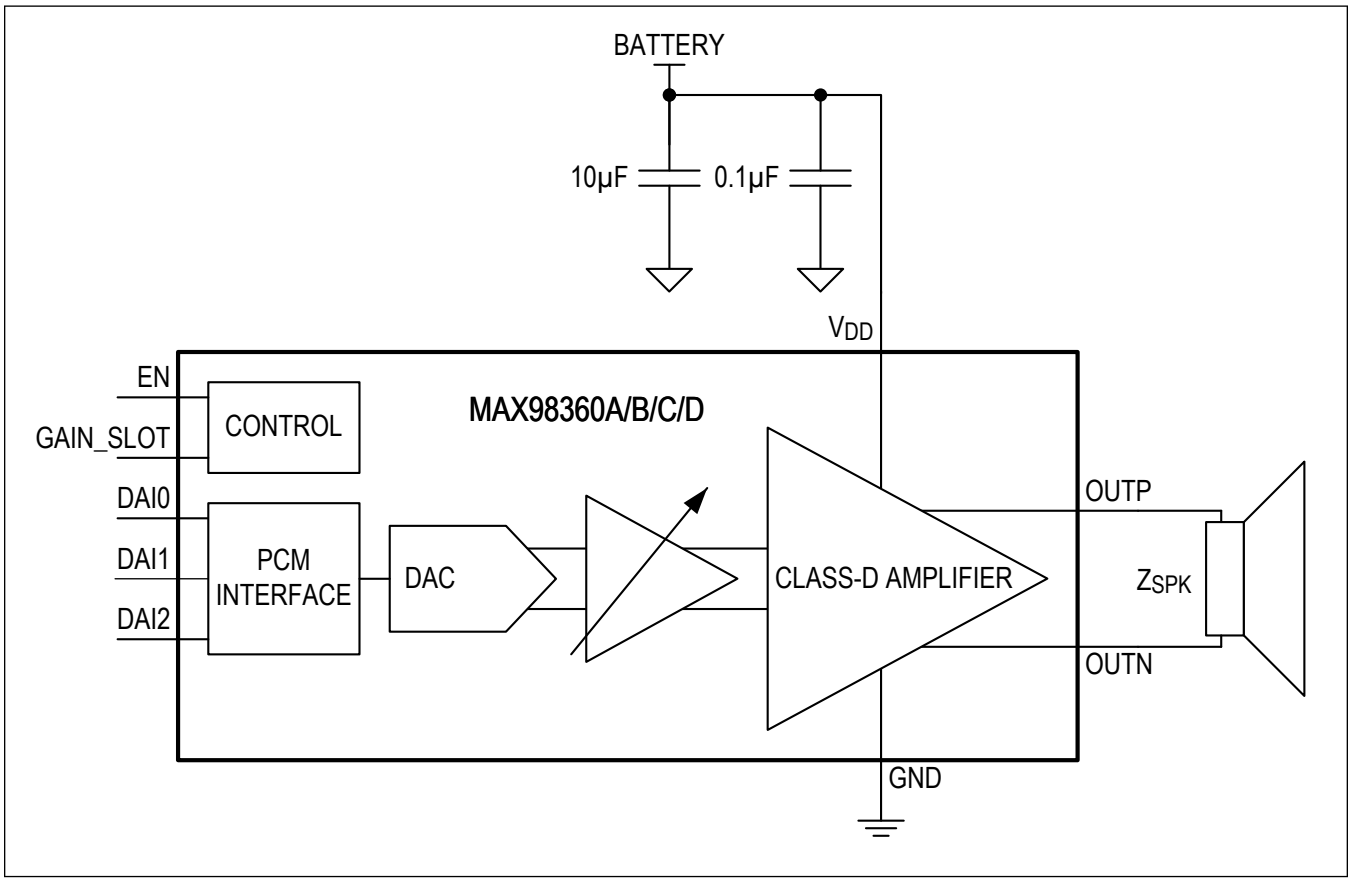


(2.0mm x 2.0mm, 0.5mm PITCH)

Pin Description

PIN		NAME	FUNCTION	REF SUPPLY	TYPE
9 WLP	10 FC2QFN				
A1	6	EN	When EN is low, the device is in Shutdown mode.	V_{DD}	Digital Input
A2	4	V_{DD}	Power Supply Input	—	Supply
A3	2	OUTP	Positive Class-D Amplifier Output	V_{DD}	Analog Output
B1	8	DAI2	Digital Audio Interface Pin 2. Internally pulled down to GND through a 3MΩ resistor.	—	Digital Input
B2	7	GAIN_SLOT	Gain and Channel Selection. Determines amplifier gain in I^2S and left-justified modes (Table 9). Used for channel selection along with DAI Configuration in TDM mode (Table 8). In TDM mode, gain is fixed at 12dB.	V_{DD}	Digital Input
B3	3	OUTN	Negative Class-D Amplifier Output	V_{DD}	Analog Output
C1	9	DAI0	Digital Audio Interface Pin 0. Internally pulled down to GND through a 3MΩ resistor.	—	Digital Input
C2	1, 5	GND	Ground	—	Supply
C3	10	DAI1	Digital Audio Interface Pin 1. Internally pulled down to GND through a 3MΩ resistor.	—	Digital Input

Functional Diagram



Detailed Description

The MAX98360A/B/C/D are digital PCM input Class-D power amplifiers. When LRCLK duty cycle is 50%, the MAX98360A and MAX98360C accept standard I^2S data, while the MAX98360B and MAX98360D accept left-justified data. When LRCLK is a frame sync pulse (LRCLK is high for 4 BCLK periods or less), the device accepts 16-bit or 32-bit TDM data with eight channels. The digital audio interface eliminates the need for an external MCLK signal that is typically required for I^2S data transmission.

The MAX98360A and MAX98360B have a fast 1ms turn-on time. The MAX98360C and MAX98360D ramp the audio volume over 13ms upon EN going high or low.

Table 1. MAX98360 Versions

	TURN-ON AND TURN-OFF RAMP	TURN-ON TIME (ms)	DATA FORMAT WHEN LRCLK DUTY CYCLE IS 50%	DATA FORMAT WHEN LRCLK IS A SYNC PULSE
MAX98360A	Ramp Disabled	1	I^2S data valid on BCLK rising edge	TDM data valid on BCLK rising edge
MAX98360B	Ramp Disabled	1	Left-justified data valid on BCLK rising edge	TDM data valid on BCLK falling edge
MAX98360C	Ramp Enabled	13	I^2S data valid on BCLK rising edge	TDM data valid on BCLK rising edge
MAX98360D	Ramp Enabled	13	Left-justified data valid on BCLK rising edge	TDM data valid on BCLK falling edge

Gain and channel selection are configured by a combination of GAIN_SLOT pin settings and connecting digital audio source signals to different DAIn pins.

The MAX98360A/B/C/D features low quiescent current, comprehensive click-and-pop suppression, and excellent RF immunity. The amplifier offers Class-AB audio performance with Class-D efficiency in a minimal board-space solution. The Class-D amplifier features spread-spectrum modulation with edge-rate and overshoot control circuitry that offers significant improvements in switch-mode amplifier radiated emissions. The amplifier features click-and-pop suppression that reduces audible transients during turn-on and turn-off. The amplifier includes thermal-overload and short-circuit protection.

EN and Shutdown Mode

The device features a low-power shutdown mode, drawing I_{SHDN} current. During shutdown, all internal blocks are turned off, including setting the output stage to a Hi-Z state. Drive EN low to put the device into shutdown.

Take care to avoid violating the Absolute Maximum Ratings limits for the EN pin. Ensuring that V_{DD} is always greater than EN is one way to prevent EN from violating the Absolute Maximum Ratings limits. If this is not possible in the application (e.g., if V_{DD} < 3.0V and EN = 3.3V), then it is necessary to add a small resistance (~2kΩ) in series with EN to limit the current into the EN pin.

Standby Mode

When the EN pin is high and there is no toggling on the DAIn pins, the device automatically enters Standby mode. In Standby mode, the Class-D amplifier is off and the outputs are in a Hi-Z state. Standby mode has reduced current consumption from normal operation (I_{STNDBY}), but not as low as full shutdown when the EN pin is low (I_{SHDN}). Standby mode can be used to reduce power consumption when no host GPIO is available to control the EN pin.

Note that volume is not ramped down when entering standby. For optimal click-and-pop performance on MAX98360A and MAX98360B, ramp down the digital audio amplitude on data presented to DIN before removing clocks. For optimal click-and-pop performance on MAX98360C and MAX98360D, either ramp down the digital audio amplitude on data presented to DIN before removing clocks or keep clocks valid for at least 13ms after pulling EN low to allow time for turn-off volume ramping.

While in standby, any toggling of the DAIn pins causes the part to exit Standby mode and enter DAI Configuration.

GAIN_SLOT Pin

The voltage on the GAIN_SLOT pin selects the gain setting while in I²S and left-justified modes and selects (in conjunction with DAI Configuration) which channel is sent to the amplifier while in TDM mode.

When the EN pin is high and the device emerges from Standby mode because of toggling on the DAIn pins, 200kΩ pullup and pulldown resistors are internally connected to GAIN_SLOT. The voltage on GAIN_SLOT can be selected by connecting the pin to GND, connecting the pin to V_{DD}, connecting the pin to GND through a 100kΩ 5% resistor, connecting the pin to V_{DD} through a 100kΩ 5% resistor, or leaving the pin unconnected.

See the *Gain Selection* section for more information on setting the gain in I²S and left-justified modes or see the *TDM Mode* section for more information on selecting the channel in TDM mode.

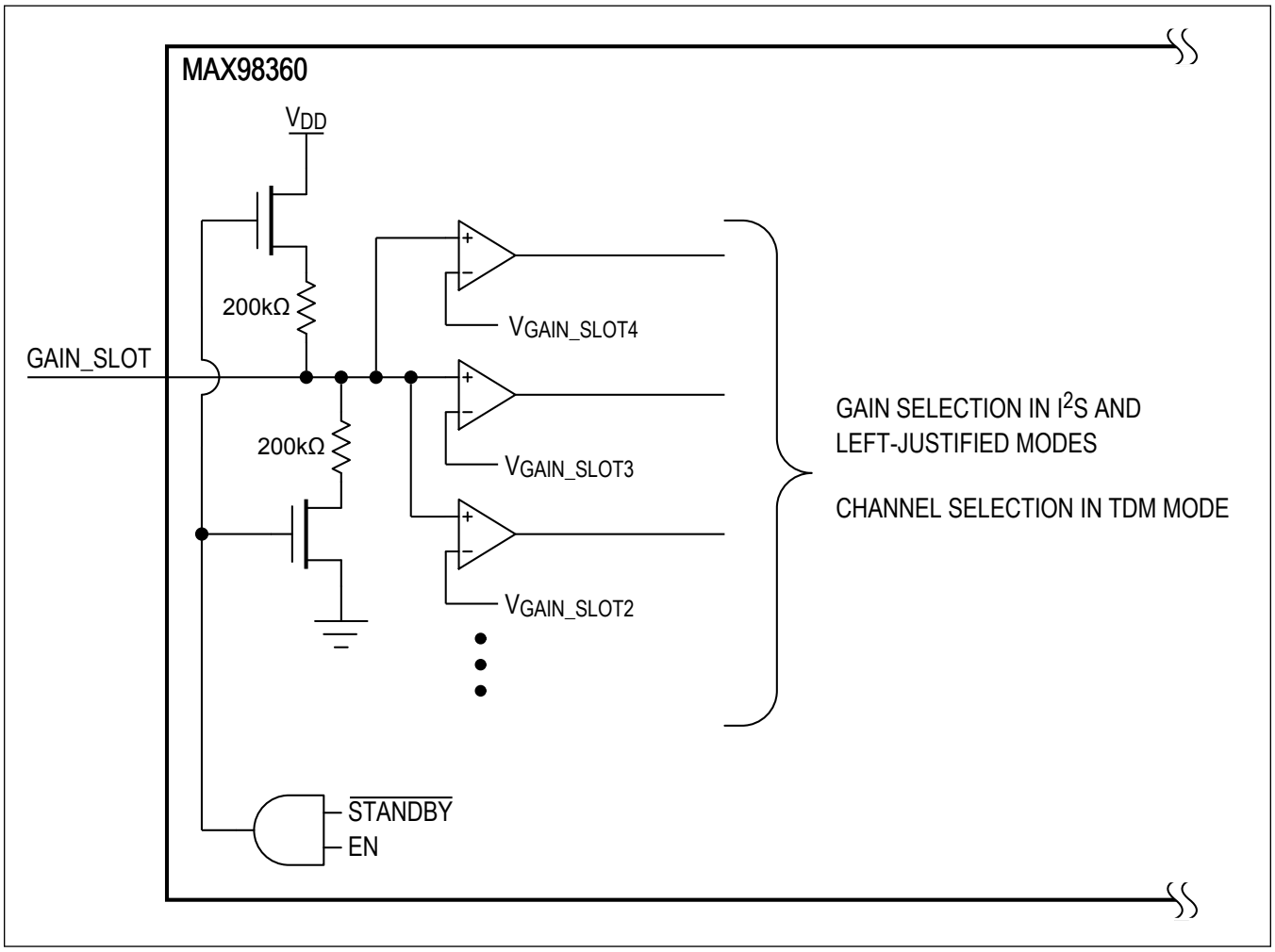


Figure 1. GAIN_SLOT Internal Resistors

Digital Audio Interface (DAI) Configuration (Patent Pending)

Different operating modes can be selected by connecting the digital audio bit clock (BCLK), the digital audio frame clock (LRCLK), and the digital audio data (DIN) to different DAIn pins.

The DAI detects BCLK by monitoring the switching frequencies at the DAIn pins. Detection starts when EN is toggled from low to high, when V_{DD} rises from UVLO to operating range while EN is held high, and when exiting Standby mode by applying clocks. The DAIn pin with the highest frequency is selected as the BCLK input. Once the BCLK input pin is identified, the LRCLK and DIN pin locations are assumed, as shown in Table 2.

If the clocks are valid for four consecutive LRCLK periods, the DAI Configuration is latched and the amplifier is allowed to turn on. Otherwise, if there is still toggling on the DAIn pins, the detection routine is restarted; if there is no toggling on the DAIn pins, the device enters Standby mode.

Once a DAI Configuration has been latched, it does not change unless EN is toggled, V_{DD} falls below V_{UVLO}, DAI Configuration restarts due to invalid clocks, or the DAIn pins stop toggling and the part goes into Standby mode. Shutdowns due to thermal protection or Class-D Current Limit do not trigger a new round of BCLK detection.

While the amplifier is on, clock validity is continually checked. If clocks become invalid, the Class-D amplifier is immediately turned off (no volume ramping) and the outputs go into a Hi-Z state. If there is still toggling on the DAIn pins, the detection routine is restarted; if there is no toggling on the DAIn pins, the device enters Standby mode.

DAI Configurations other than those shown in Table 2 are not valid.

Table 2. DAI Configurations

BCLK LOCATION	LRCLK LOCATION	DIN LOCATION	DAI CONFIGURATION
DAI0	DAI1	DAI2	A
DAI1	DAI2	DAI0	B
DAI2	DAI0	DAI1	C

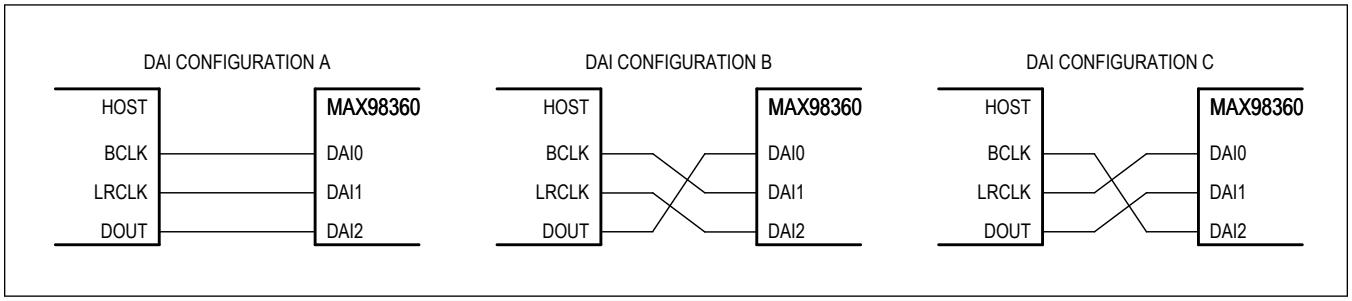


Figure 2. DAI Connections

Valid Clock Frequencies

When LRCLK has a 50% duty cycle, MAX98360A and MAX98360C are automatically configured for I²S mode, while MAX98360B and MAX98360D are automatically configured for left-justified mode. When a frame sync pulse is used for LRCLK (LRCLK is high for 4 BCLK periods or less), the device is automatically configured for TDM mode.

Valid sample rates are 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz. (LRCLK clocks at 11.025kHz, 12kHz, 22.05kHz, and 24kHz are **NOT** supported.) f_{S1}, f_{S2}, f_{S3}, and f_{S4} define LRCLK frequency regions where the device is guaranteed to perform within specifications (assuming that all other inputs are in valid ranges). The output waveform is unpredictable if LRCLK frequency is not within f_{S1}, f_{S2}, f_{S3}, or f_{S4}.

In I²S/left-justified mode, valid resolutions are 16 bits per channel, 24 bits per channel, and 32 bits per channel. There are 2 channels per LRCLK period. Therefore, the valid numbers of BCLK periods per LRCLK period in I²S/left-justified mode are exactly 32 BCLK periods per LRCLK period, 48 BCLK periods per LRCLK period, and 64 BCLK periods per LRCLK period.

In TDM mode, valid resolutions are 16 bits per channel and 32 bits per channel. There are 8 channels per LRCLK period. Therefore, the valid numbers of BCLK periods per LRCLK period in TDM mode are exactly 128 BCLK periods per LRCLK period and exactly 256 BCLK periods per LRCLK period.

An invalid number of BCLKs per LRCLK results in an unpredictable output waveform.

Table 3. Valid Resolutions and Frame Widths

SAMPLE RESOLUTION (BITS)	BCLK PERIODS PER LRCLK IN I²S/LEFT-JUSTIFIED MODE	BCLK PERIODS PER LRCLK IN TDM MODE
16	32	128
24	48	NOT VALID
32	64	256

Table 4. Valid BCLK Frequencies (kHz)

	I²S/LEFT-JUSTIFIED MODE			TDM MODE	
	32 BCLKs PER LRCLK	48 BCLKs PER LRCLK	64 BCLKs PER LRCLK	128 BCLKs PER LRCLK	256 BCLKs PER LRCLK
LRCLK = 8kHz	256	384	512	1024	2048
LRCLK = 16kHz	512	768	1024	2048	4096
LRCLK = 32kHz	1024	1536	2048	4096	8192
LRCLK = 44.1kHz	1411.2	2116.8	2822.4	5644.8	11289.6
LRCLK = 48kHz	1536	2304	3072	6144	12288
LRCLK = 88.2kHz	2822.4	4233.6	5644.8	11289.6	22579.2
LRCLK = 96kHz	3072	4608	6144	12288	24576

MCLK Elimination

The MAX98360 eliminates the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin-count.

BCLK Jitter Tolerance

The MAX98360 features a high BCLK jitter tolerance while maintaining a high dynamic range (see the *Electrical Characteristics* table).

BCLK Polarity

In I²S and left-justified mode, incoming serial data is always clocked-in on the rising-edge of BCLK. In TDM mode, the MAX98360A and MAX98360C clock-in serial data on the rising-edge of BCLK, while the MAX98360B and MAX98360D clock in serial data on the falling-edge of BCLK (Table 5).

Table 5. BCLK Polarity

MODE	PART NUMBERS	BCLK POLARITY
I²S	MAX98360A/C	Rising edge
Left-justified	MAX98360B/D	Rising edge
TDM	MAX98360A/C	Rising edge
TDM	MAX98360B/D	Falling edge

LRCLK Polarity in I²S/Left-Justified Mode

In I²S and left-justified mode, LRCLK specifies whether left-channel data or right-channel data is currently being read by the digital audio interface. The MAX98360A and MAX98360C indicate the left channel word when LRCLK is low, and the MAX98360B and MAX98360D indicate the left channel word when LRCLK is high (Table 6).

Table 6. LRCLK Polarity in I²S/Left-Justified Mode

PART NUMBER	LRCLK POLARITY (LEFT CHANNEL)
MAX98360A/C	Low
MAX98360B/D	High

I²S and Left-Justified Mode

When LRCLK duty cycle is 50%, the MAX98360A and MAX98360C follow standard I²S timing by allowing a delay of one BCLK cycle after the LRCLK transition before the beginning of a new data word (Figure 3 and Figure 4). The MAX98360B and MAX98360D follow the left-justified timing specification by aligning the LRCLK transitions with the beginning of a new data word (Figure 5 and Figure 6).

In I²S and left-justified modes, the audio channel that is sent to the amplifier output is chosen by the DAI Configuration (see Table 2). Use DAI Configuration A to select the left word of the stereo input data. Use DAI Configuration B to select the right word of the stereo input data. Use DAI Configuration C to select both the left and right words of the stereo input data (left/2 + right/2).

Table 7. Channel Selection in I²S and Left-Justified Modes

DAI CONFIGURATION	CHANNEL
A	Left
B	Right
C	Left/2 + Right/2

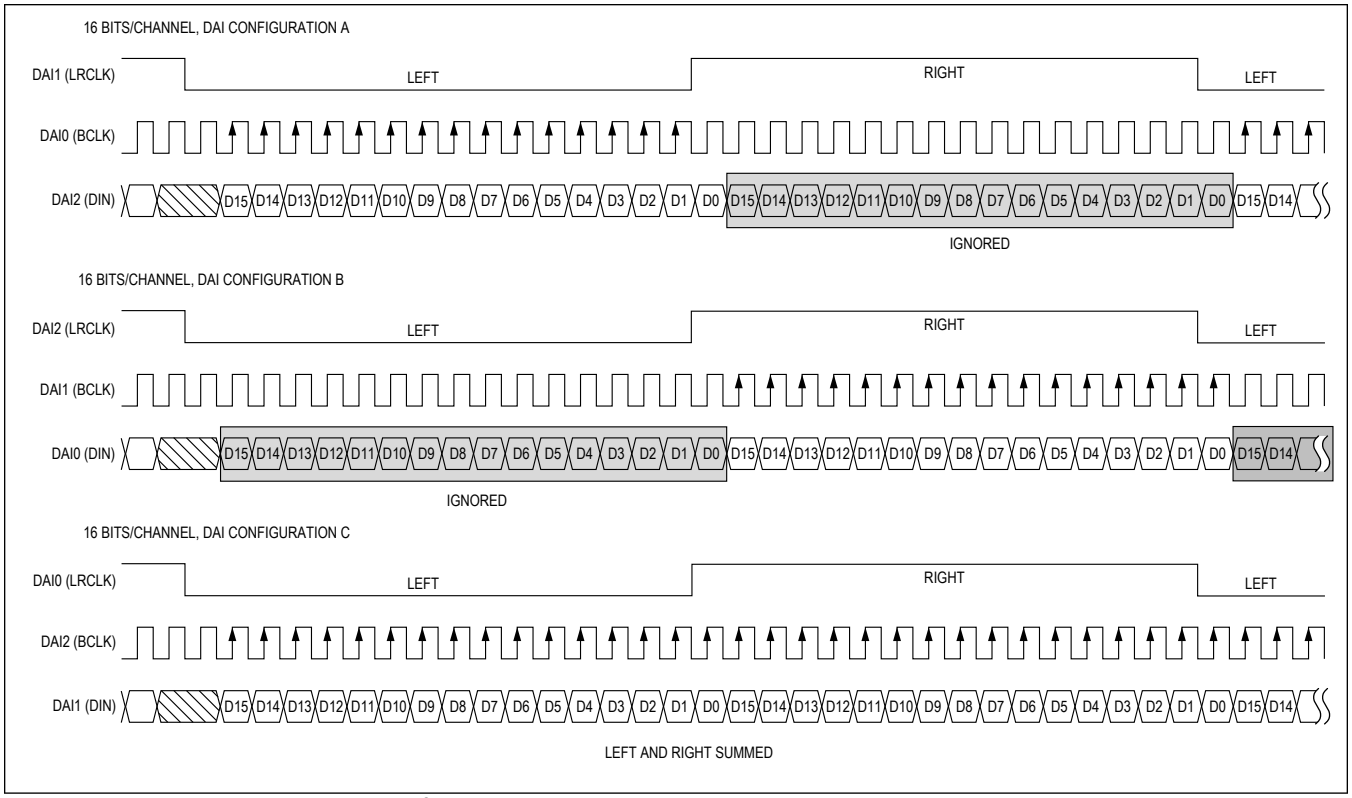


Figure 3. MAX98360A and MAX98360C I²S Protocol, 16-Bit Resolution

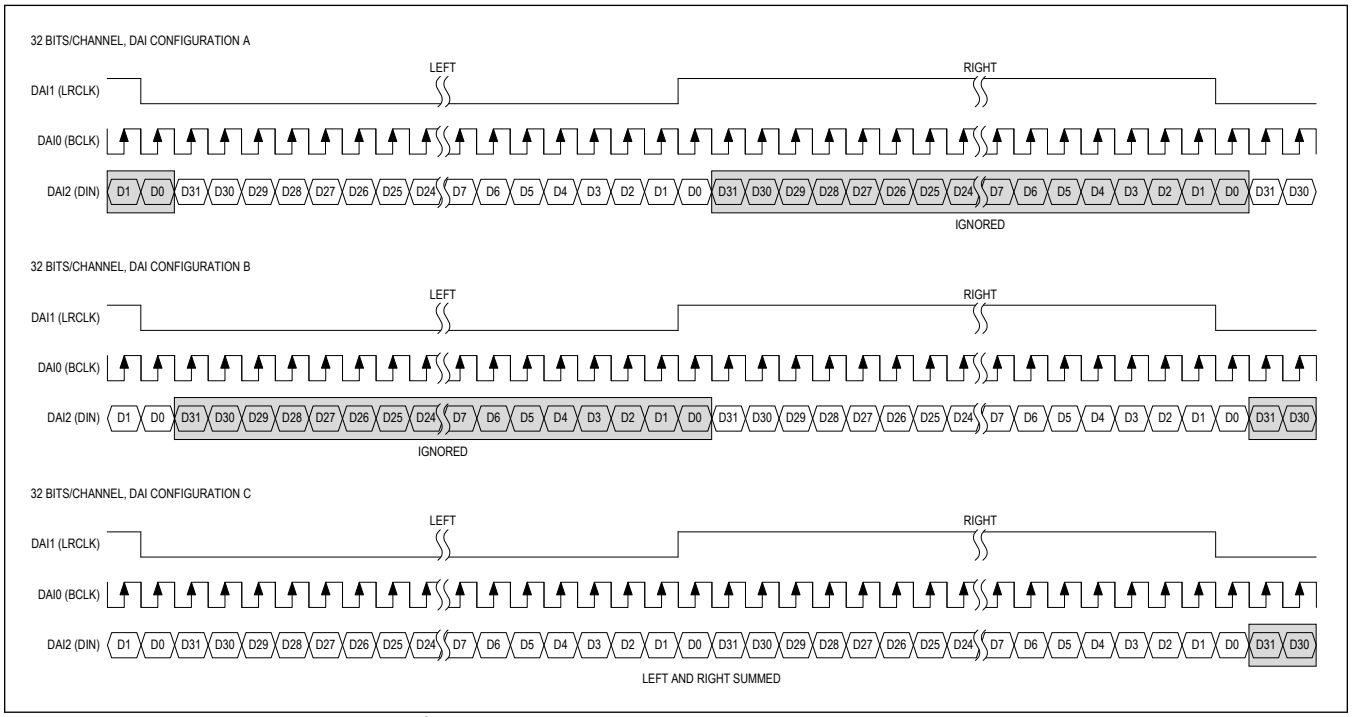


Figure 4. MAX98360A and MAX98360C I²S Protocol, 32-Bit Resolution

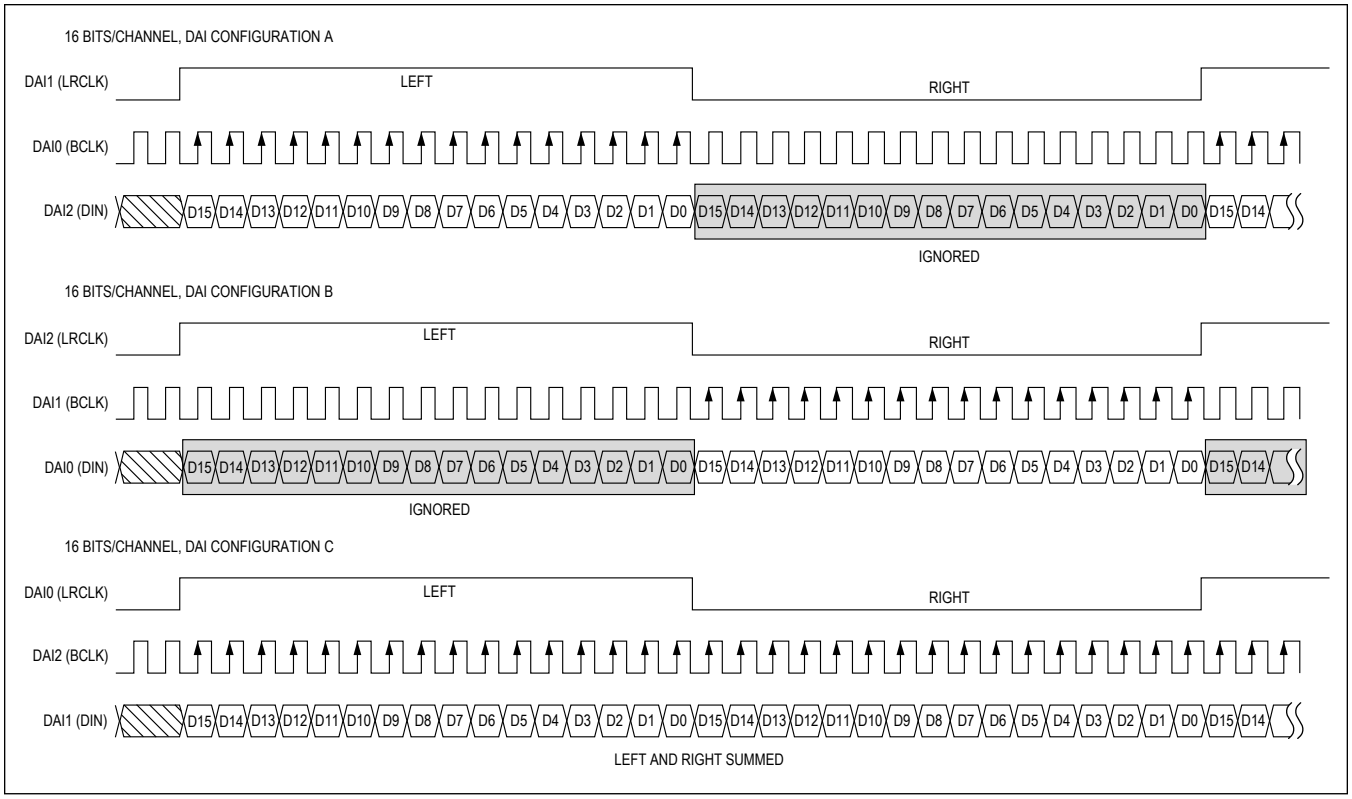


Figure 5. MAX98360B and MAX98360D Left-Justified Protocol, 16-Bit Resolution

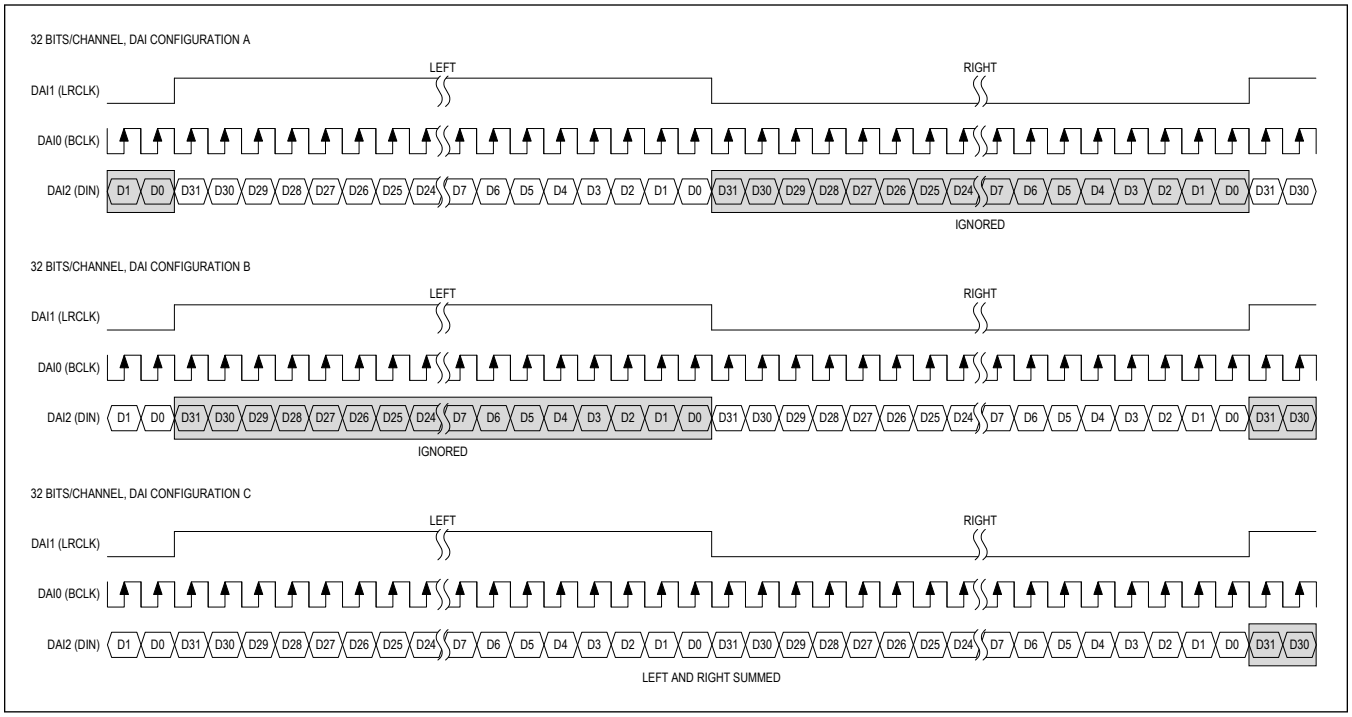


Figure 6. MAX98360B and MAX98360D Left-Justified Protocol, 32-Bit Resolution

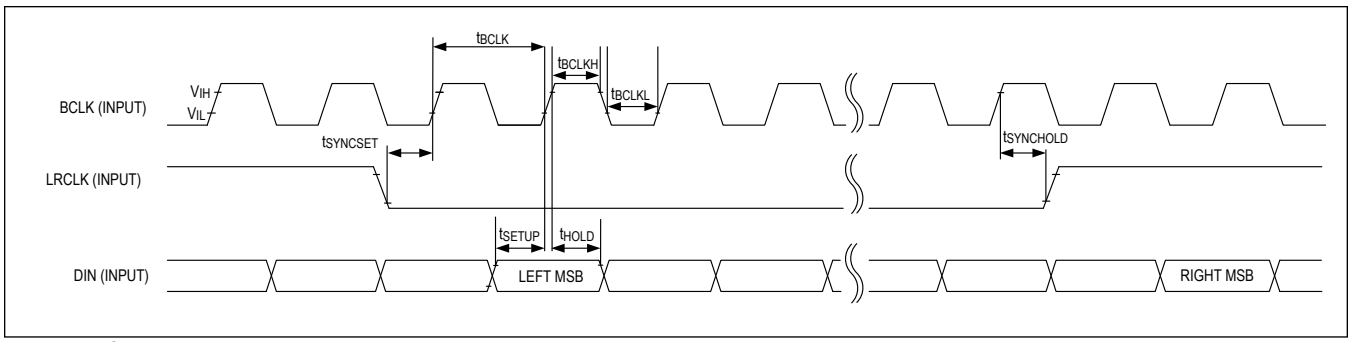


Figure 7. I²S Timing Diagram (MAX98360A and MAX98360C)

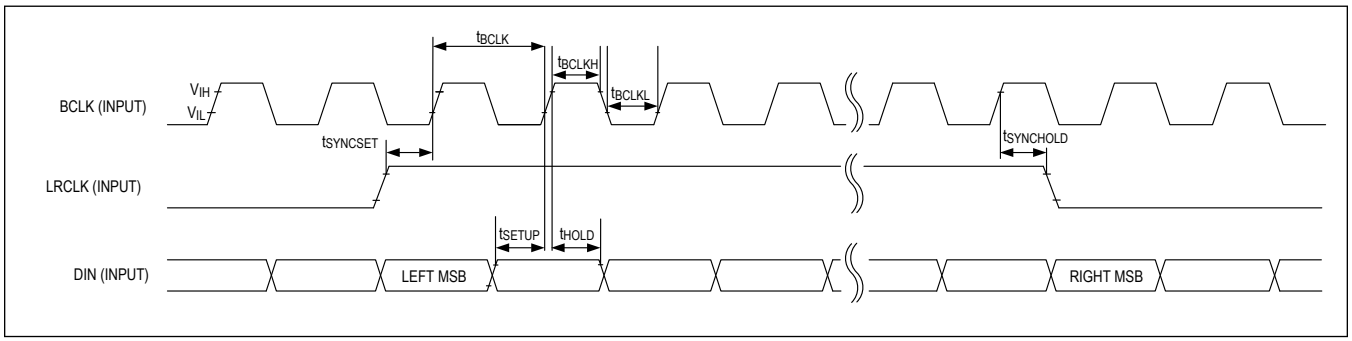


Figure 8. Left-Justified Timing Diagram (MAX98360B and MAX98360D)

TDM Mode

When a frame sync pulse is used for LRCLK (LRCLK is high for 4 BCLK periods or less), the device is automatically configured for TDM mode.

In TDM mode, the device only accepts 8 channels of 16-bit or 32-bit formatted data. Therefore, there must be 128 (16-bit mode) or 256 (32-bit mode) BCLK cycles per frame.

DAI Configuration and GAIN_SLOT are used to select which channel is sent to the amplifier (see Table 8).

On the MAX98360A and MAX98360C, data is valid on the BCLK rising edge (see Figure 9 and Figure 10). On the MAX98360B and MAX98360D, data is valid on the BCLK falling edge (see Figure 11 and Figure 12).

Table 8. TDM Mode Channel Selection

DAI CONFIGURATION	GAIN_SLOT	CHANNEL
A	GND	0
A	V_{DD}	1
A	Unconnected	2
B	V_{DD}	3
B	GND	4
C	GND	5
C	Unconnected	6
C	V_{DD}	7

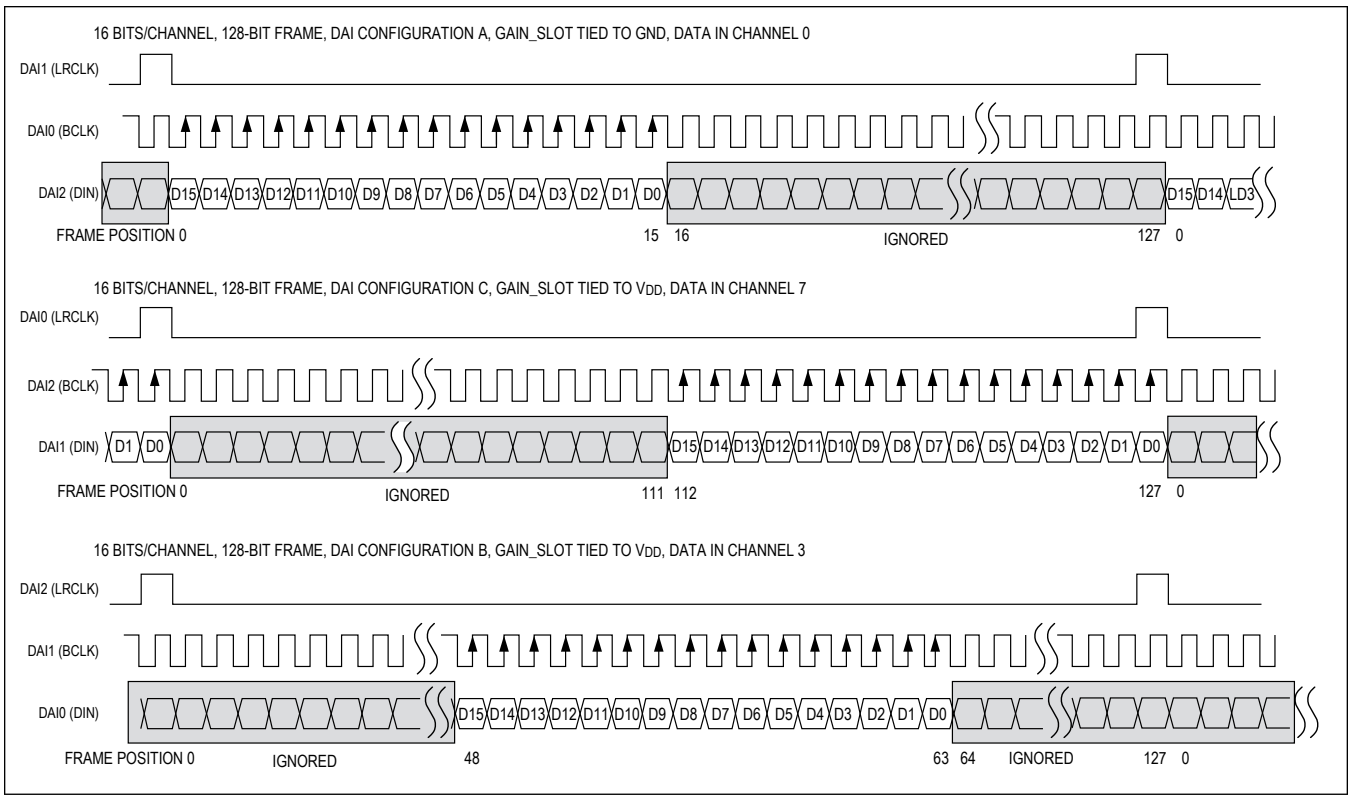


Figure 9. MAX98360A and MAX98360C TDM Protocol, 16-Bit Resolution

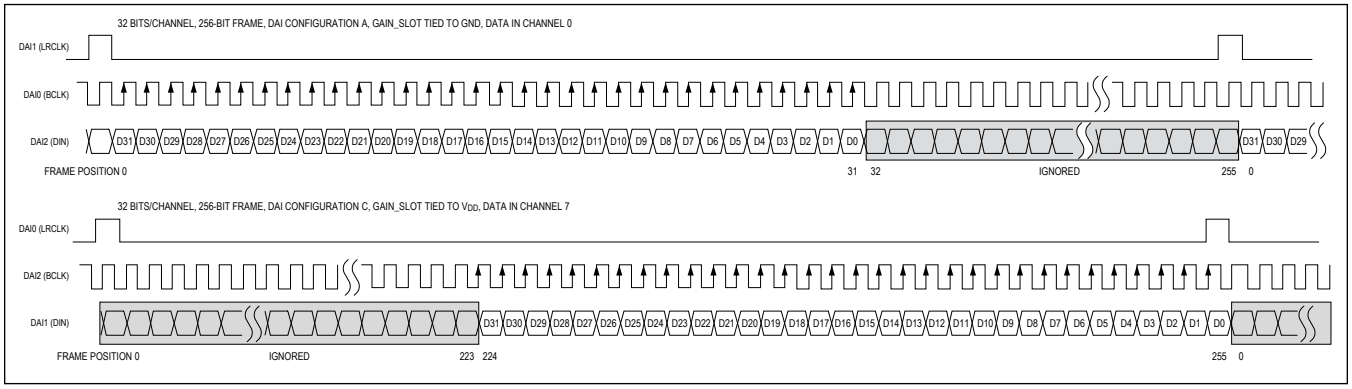


Figure 10. MAX98360A and MAX98360C TDM Protocol, 32-Bit Resolution

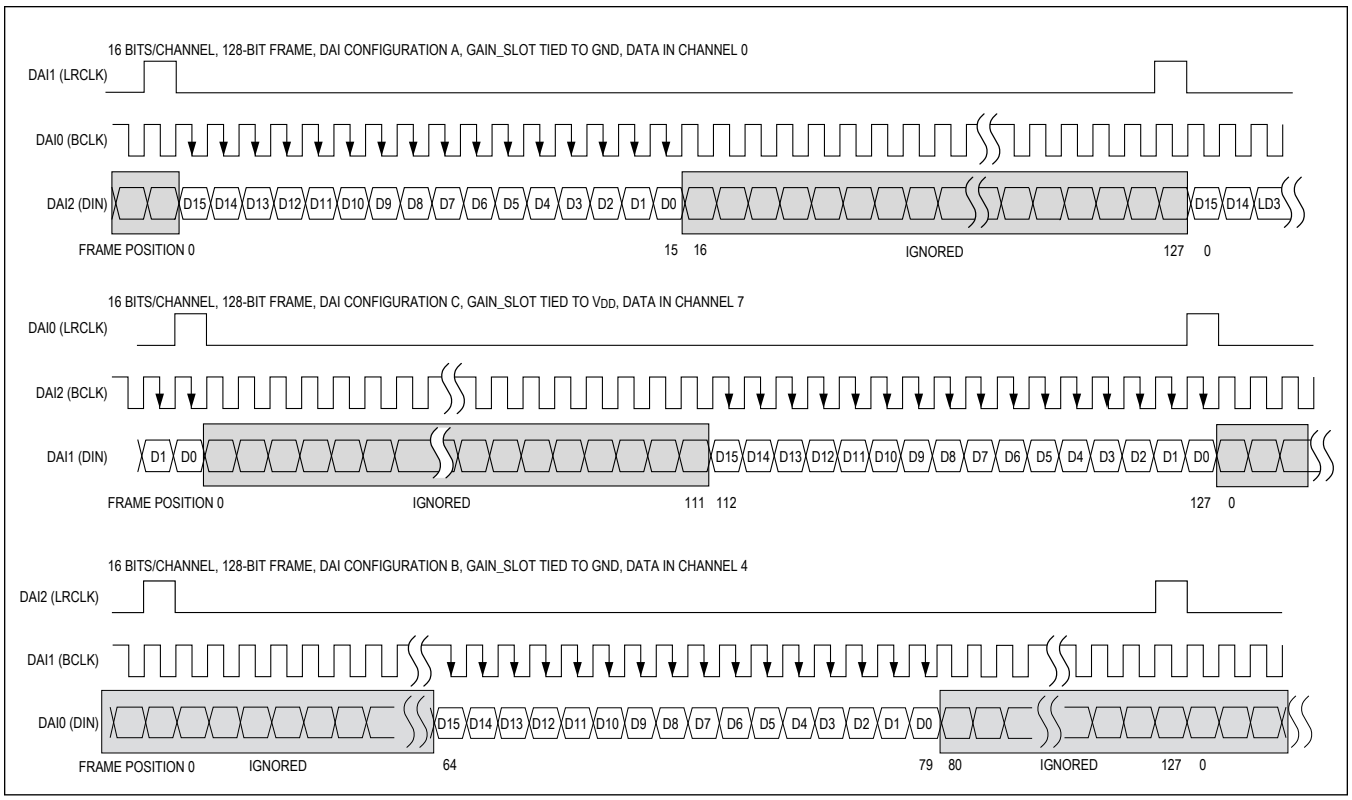


Figure 11. MAX98360B and MAX98360D TDM Protocol, 16-Bit Resolution

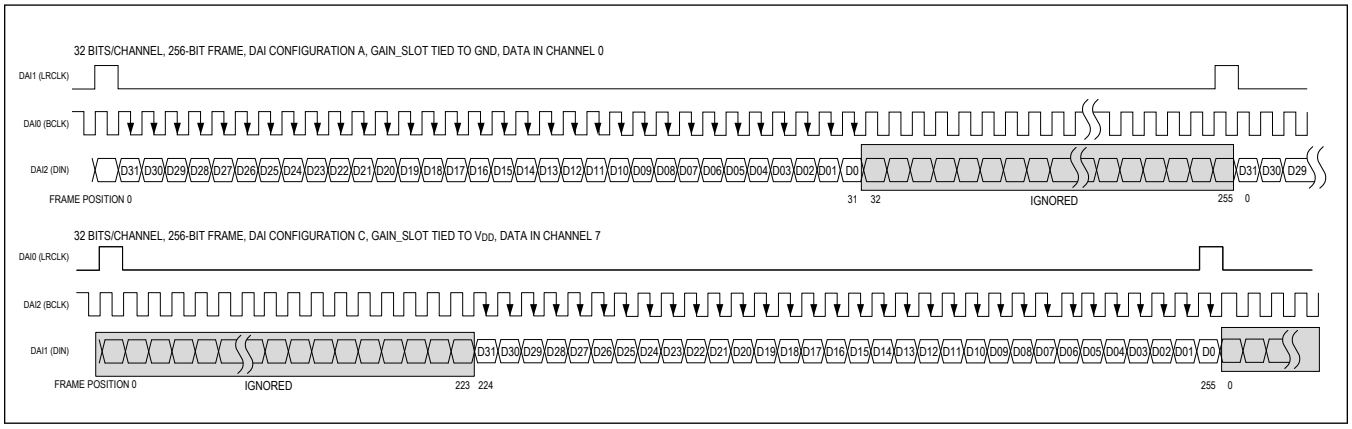


Figure 12. MAX98360B and MAX98360D TDM Protocol, 32-Bit Resolution

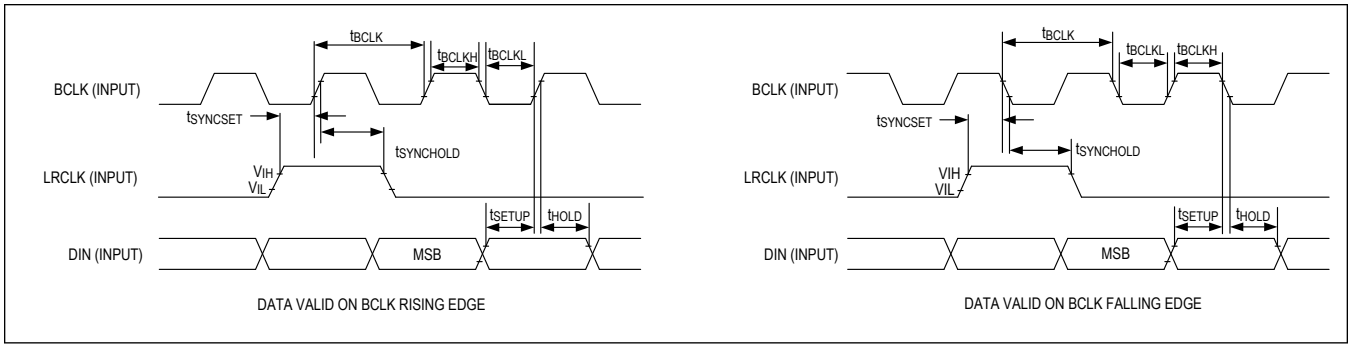


Figure 13. TDM Timing Diagrams—BCLK Rising Edge (MAX98360A/C) and BCLK Falling Edge (MAX98360B/D)

Gain Selection

In I^2S and left-justified modes, one of five gain settings is selected through the GAIN_SLOT pin (Table 9). In TDM mode, the gain is automatically set at a fixed 12dB.

Gain is referenced to the full-scale output of the DAC, which is 2.3dBV. Assuming that the desired output swing is not limited by the supply voltage rail, the output level can be calculated based on the digital input signal level and selected amplifier gain according to the following equation:

Output signal level (dBV) = input signal level (dBFS) + 2.3dB + amplifier gain (dB)

Table 9. Gain Selection

GAIN_SLOT	I^2S/LEFT-JUSTIFIED GAIN (dB)
Connect to GND	12
Unconnected	9
Connect to V_{DD}	6
Connect to V_{DD} through 100kΩ ±5% resistor	3
Connect to GND through 100kΩ ±5% resistor	-3

DC Blocking Filter

The digital audio interface includes a DC blocking filter with a -3dB cutoff at f_C (see the *Electrical Characteristics* table).

DAC Digital Filters

The DAC features a digital lowpass filter that is automatically configured for voice playback or music playback based on the sample rate that is used. This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. See the *DAC Digital Filters* section of the *Electrical Characteristics* table.

Class-D Amplifier

The filterless Class-D amplifier offers much higher efficiency than Class-AB amplifiers. The high efficiency of a Class-D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class-D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Class-D Output Short-Circuit Protection

If the output current limit of the Class-D amplifier (I_{LIM}) is exceeded (see the *Electrical Characteristics* table), the outputs are disabled for approximately 100µs. At the end of the 100µs, the outputs are re-enabled. If the fault condition still exists, the outputs continue to disable and re-enable until the fault condition is removed.

Turn-On and Turn-Off Volume Ramping

The MAX98360A and MAX98360B have a fast 1ms turn-on time. For optimal click-and-pop performance, ramp down the digital audio amplitude on data presented to DIN before shutting down, removing clocks, or removing power.

The MAX98360C and MAX98360D ramp the audio signal from mute to full scale over 13ms after DAI Configuration. When turned off by pulling EN low, gain is ramped down to mute over 13ms. Turn-off ramping only occurs if BCLK and LRCLK remain valid and V_{DD} remains within its operating range for at least 13ms after EN goes low. If either clock becomes invalid, or if V_{DD} falls below V_{UVLO}, audio stops immediately without ramping.

Click-and-Pop Suppression

The speaker amplifier features Maxim's comprehensive click-and-pop suppression. During turn-on, the click-and-pop suppression circuitry reduces audible transient sources internal to the device. When entering shutdown or standby, the differential speaker outputs simultaneously go to Hi-Z.

The comprehensive click-and-pop suppression of the MAX98360 is unaffected by power-up or power-down sequencing. Applying or removing the clocks before or after the transition of EN yields the same click-and-pop performance. However, note that for MAX98360C and MAX98360D, clocks and V_{DD} must remain valid for 13ms after EN goes low to allow for volume ramping to complete for best click-and-pop performance.

Ultra-Low EMI Filterless Output Stage

Traditional Class-D amplifiers require the use of external LC filters or shielding to meet EN55022B electromagnetic interference (EMI) regulation standards. Maxim's active emissions-limiting, edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions while maintaining high efficiency.

Maxim's spread-spectrum modulation mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The device's spread-spectrum modulator randomly varies the switching frequency by f_{SSM} around the center frequency (f_{SW}). Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Applications Information

Filterless Class-D Operation

Traditional Class-D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, size, and decreases efficiency and THD+N performance. The amplifier's filterless modulation scheme does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output.

Because the switching frequency of the amplifier is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Power Supply Input

The device is powered from a single 2.5V to 5.5V supply (V_{DD}). Bypass V_{DD} with a 0.1µF and 10µF capacitor to GND. Some applications might require only the 10µF bypass capacitor, making it possible to operate with a single external component. Apply additional bulk capacitance at the V_{DD} pin if long PCB traces between V_{DD} and the power source are used.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

For best EMI and audio performance, it is essential that the V_{DD} decoupling capacitor be placed as close as possible to the MAX98360 to minimize the supply loop inductance.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increases. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through 100mΩ of total speaker trace, 1.904W is being delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.951W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

Parasitic capacitance on the output traces cause higher quiescent current by $V_{DD} \times f_{SW} \times C_{PARASITIC}$. For example, at V_{DD} = 5V and a total parasitic capacitance of 100pF (50pF on each output trace), the increase in quiescent current is 5V x 300kHz x 100pF = 150µA.

The device is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

In many applications, the only passive component required is a single capacitor, which results in a tiny solution size of 3.69mm^2.

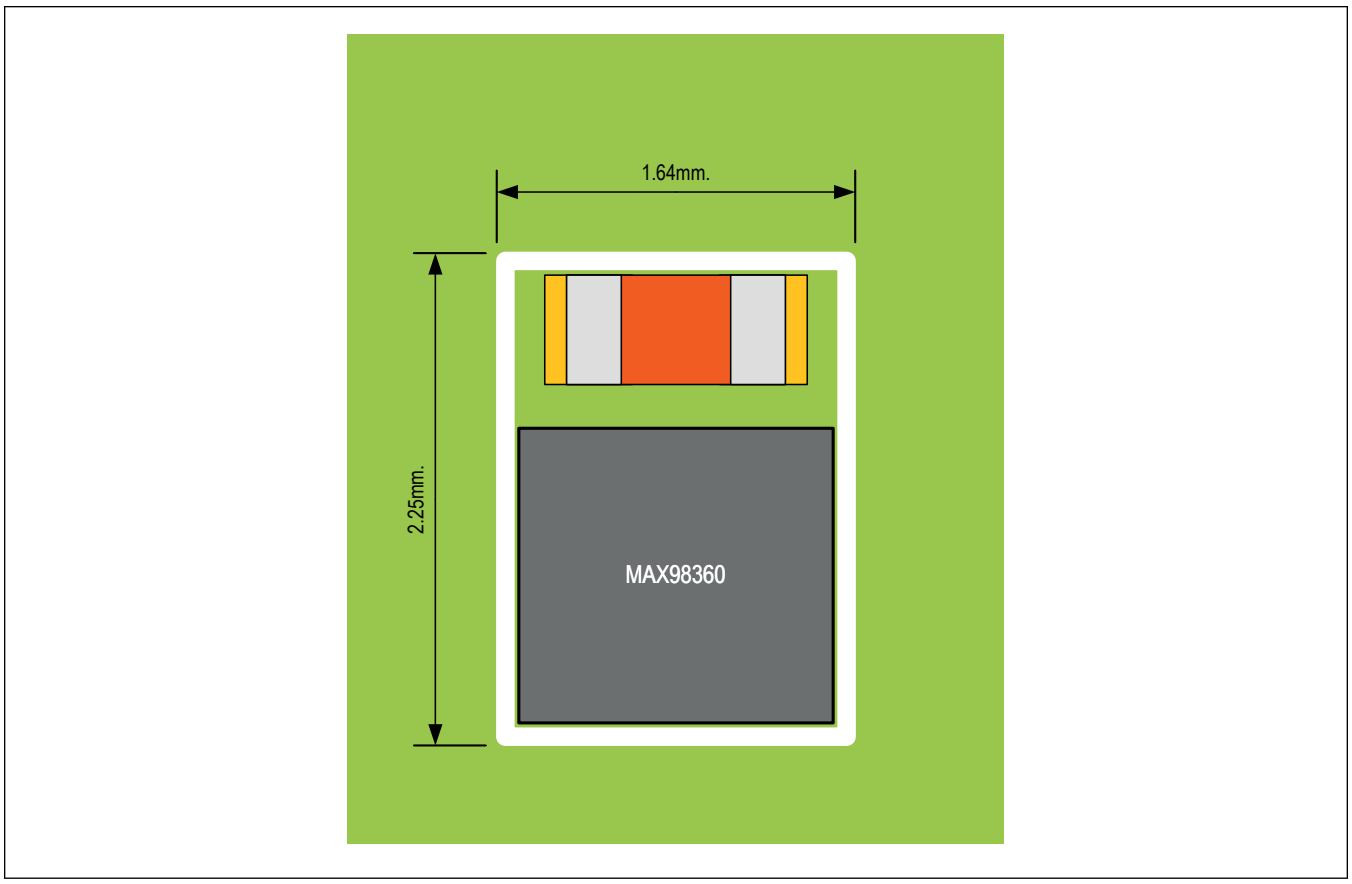


Figure 14. Solution Size

WLP GAIN_SLOT Routing

The intended use for the GAIN_SLOT pin is to either fix the desired gain in I²S and left-justified modes or to select the TDM channel. GAIN_SLOT should not be changed during audio playback as it could result in audible clicks or pops.

Most modes are selectable without using a via or routing out the center bump of the WLP. This simplifies the layout and allows for inexpensive PCB fabrication.

In I²S and left-justified modes, 6dB, 9dB, and 12dB gain settings do not require GAIN_SLOT to be routed out (see Table 9). In TDM mode, all channels can be selected without routing out GAIN_SLOT (see Table 8). This is possible because of the GAIN_SLOT pin's placement in relation to the V_{DD} and GND pins.

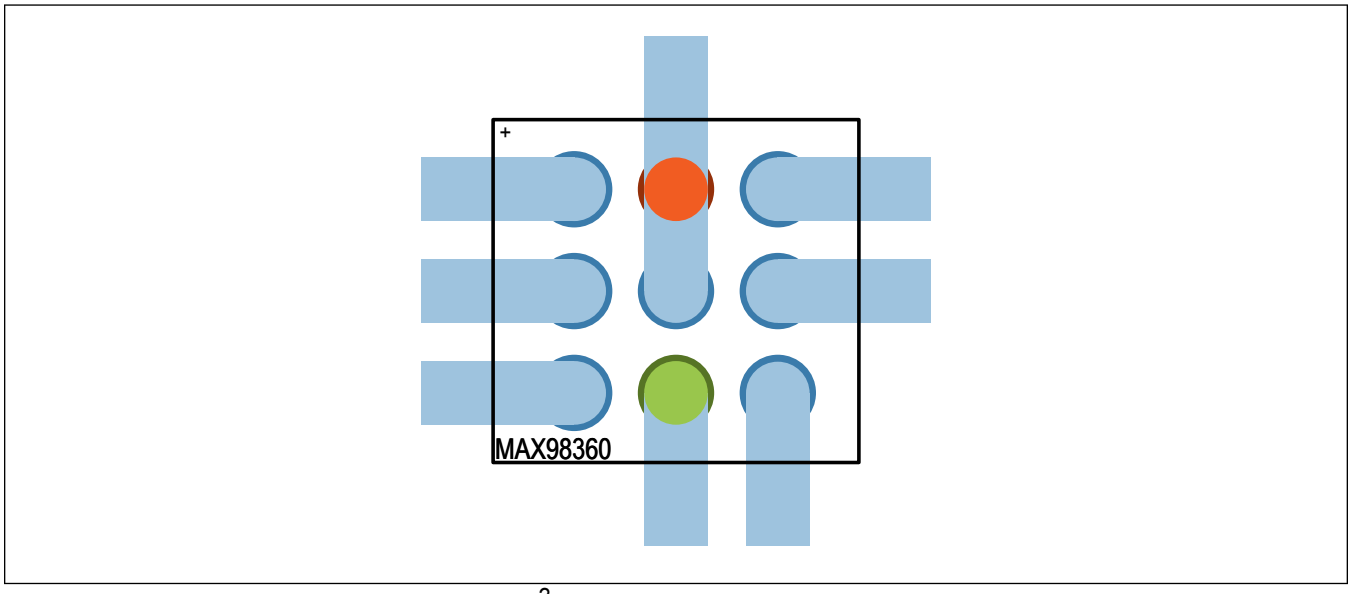


Figure 15. GAIN_SLOT Tied to V_{DD} (Gain is 6dB in I²S and Left-Justified Modes)

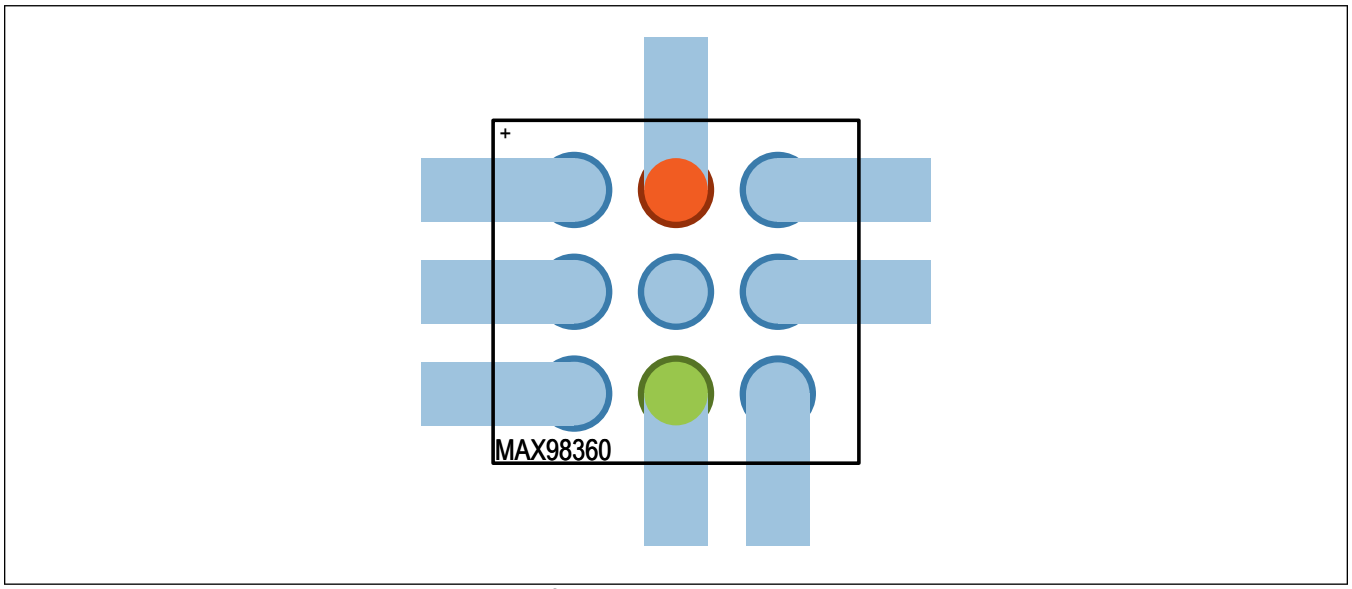


Figure 16. GAIN_SLOT Unconnected (Gain is 9dB in I²S and Left-Justified Modes)

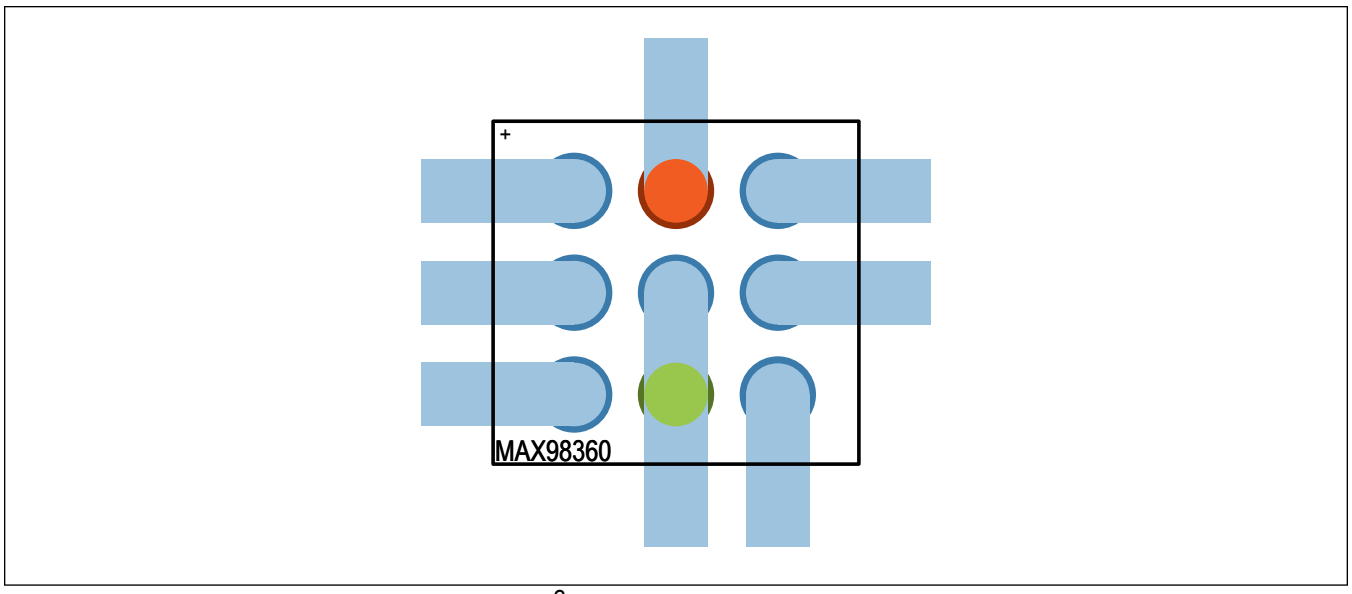


Figure 17. GAIN_SLOT Tied to GND (Gain is 12dB in I^2S and Left-Justified Modes)

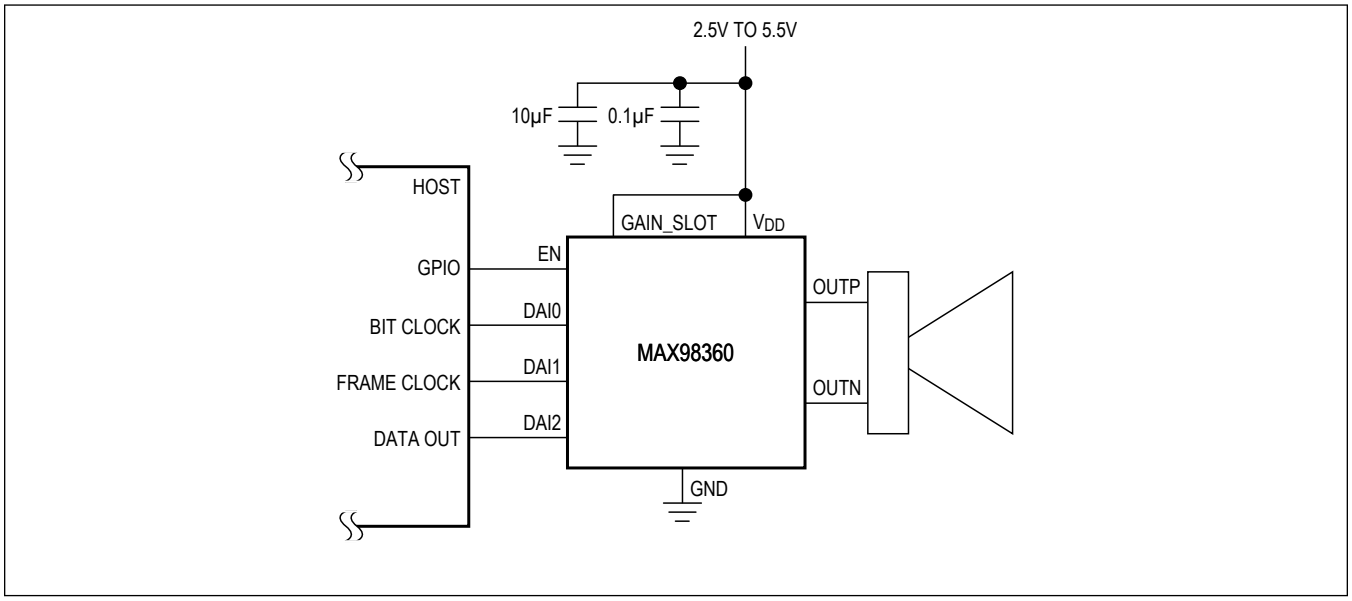
If using I^2S or left-justified modes and a -3dB or 3dB gain setting is required, the GAIN_SLOT pin must be routed to a 100kΩ resistor that is connected to either V_{DD} or GND. Some routing options are:

- Mechanically drilled via: cheaper if PCB volumes are low
- Laser-drilled alternative: cheaper if PCB volumes are high
- Blind and buried vias with dog-boning
- Trace on the top layer: this must be a minimal pitch trace

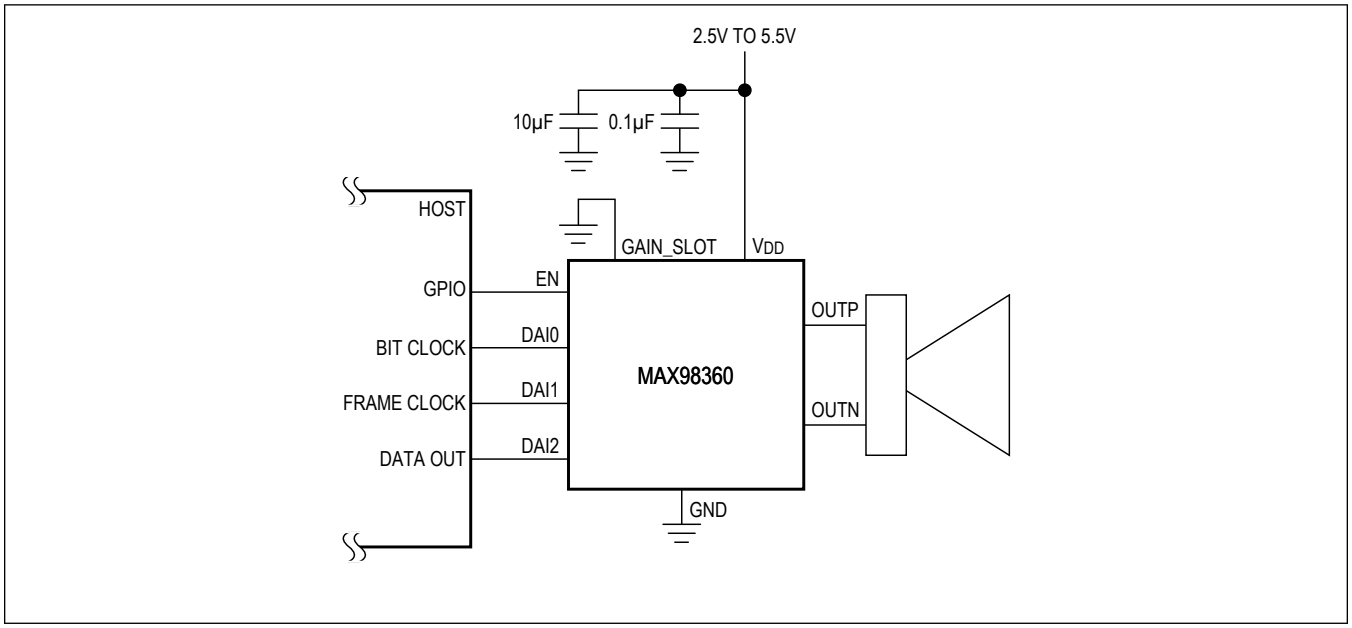
PCB fabrication technology is constantly evolving, so check with your PCB manufacturer to see what option may work best for your design.

Typical Application Circuits

I²S/Left-Justified Left-Channel Operation with 6dB Gain

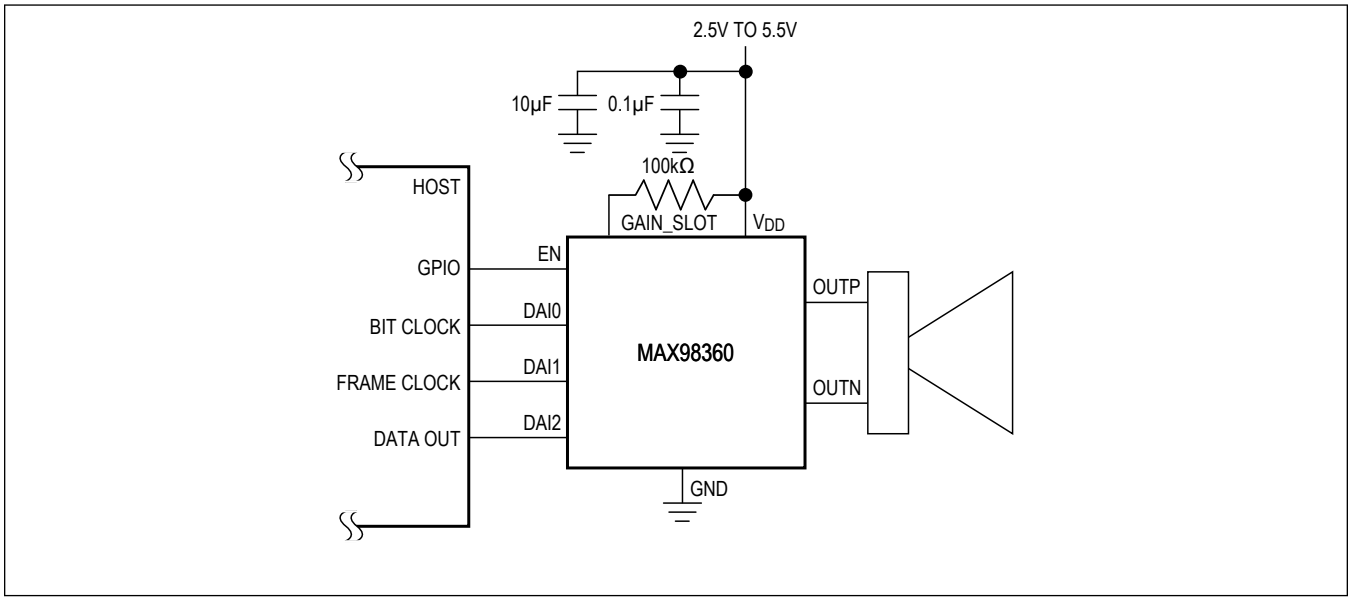


I²S/Left-Justified Left-Channel Operation with 12dB Gain

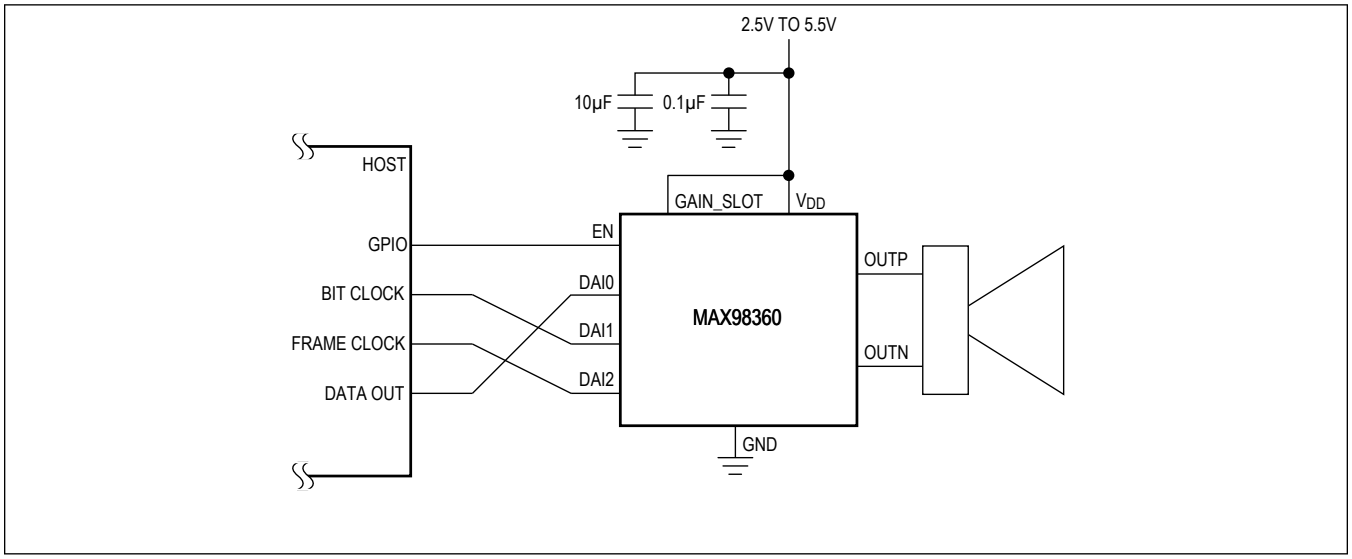


Typical Application Circuits (continued)

I²S/Left-Justified Left-Channel Operation with 3dB Gain

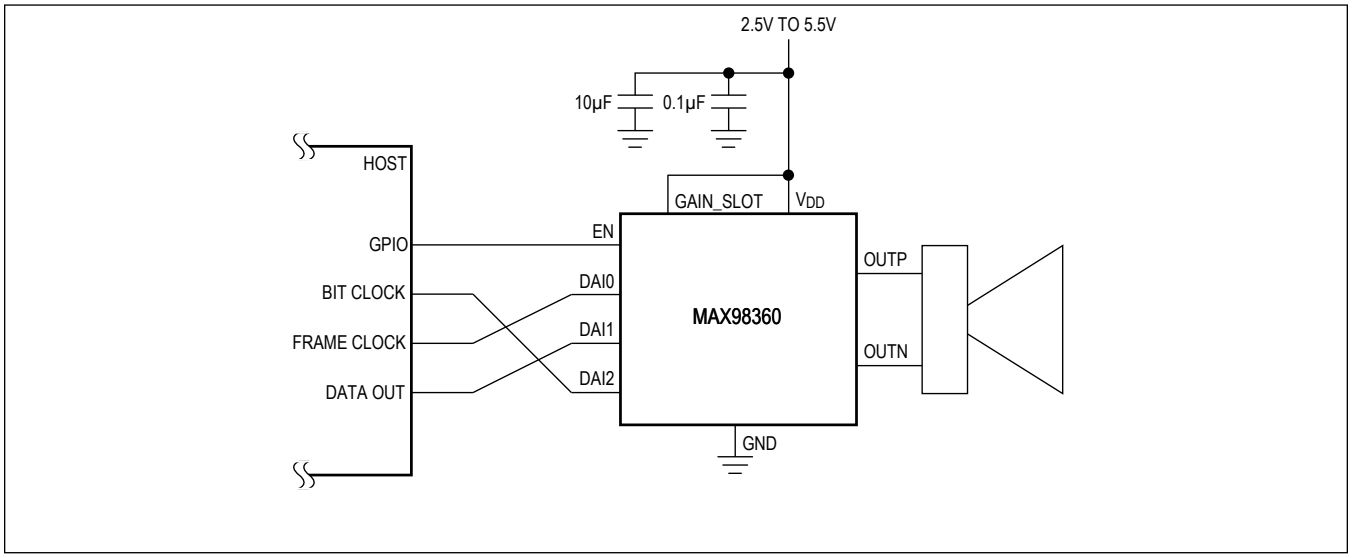


I²S/Left-Justified Right-Channel Operation with 6dB Gain



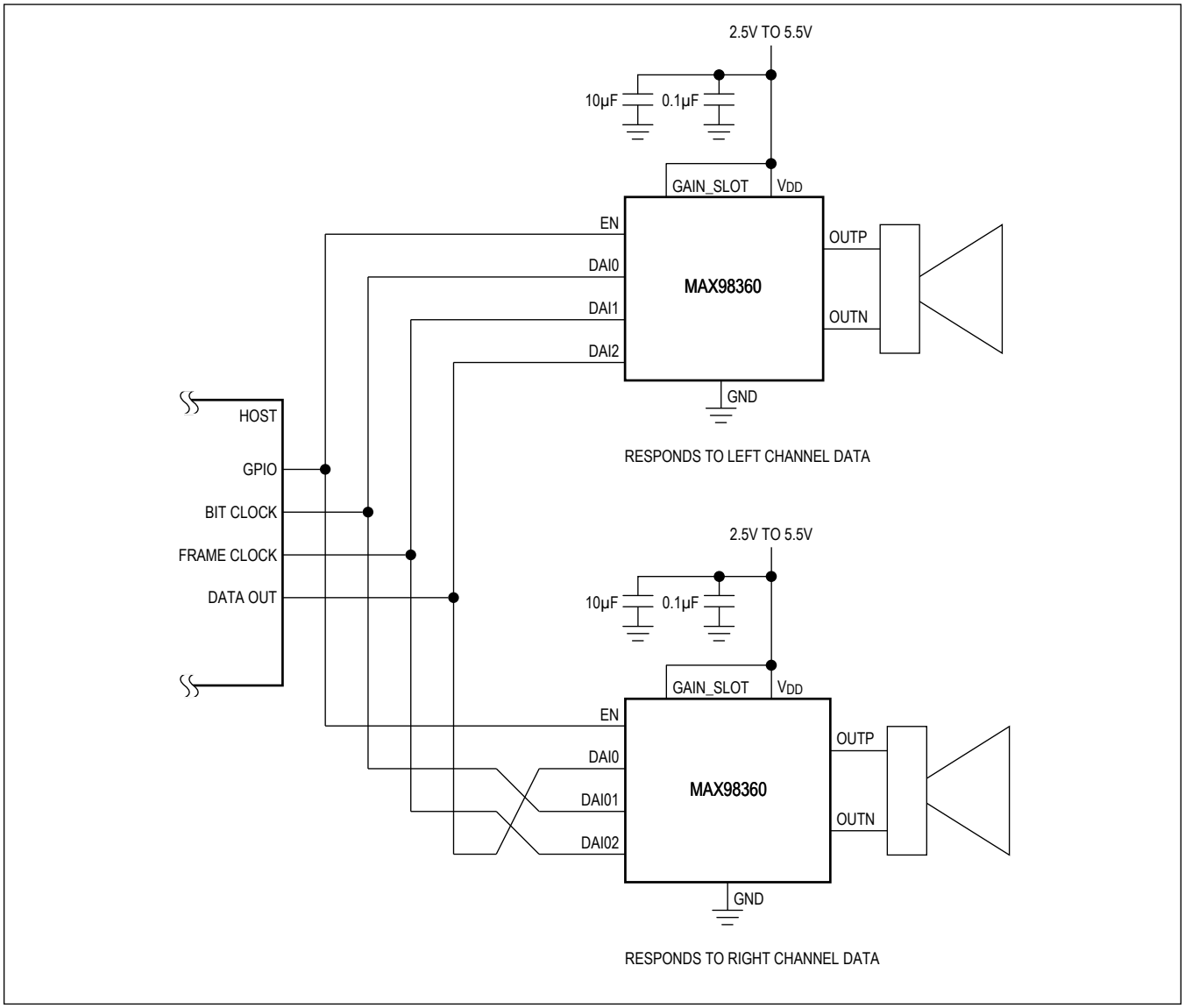
Typical Application Circuits (continued)

I²S/Left-Justified Left/2 + Right/2 Operation with 6dB Gain



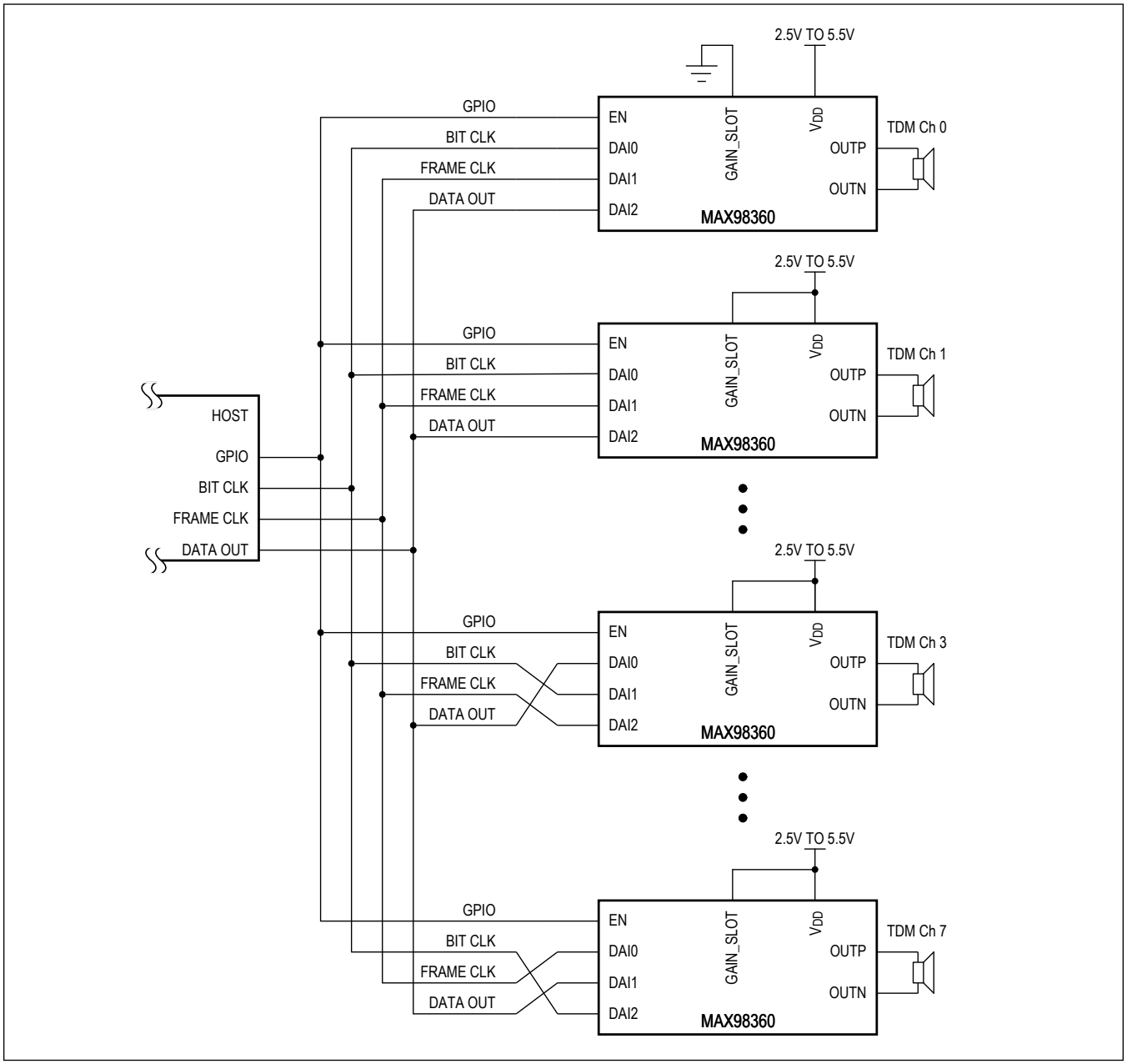
Typical Application Circuits (continued)

I²S/Left-Justified Stereo Operation with 6dB Gain



Typical Application Circuits (continued)

TDM Operation (Gain Fixed at 12dB)



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX98360AENL+	-40°C to +85°C	9 WLP	AAL
MAX98360AENL+T	-40°C to +85°C	9 WLP	AAL
MAX98360BENL+	-40°C to +85°C	9 WLP	AAO
MAX98360BENL+T	-40°C to +85°C	9 WLP	AAO
MAX98360CENL+	-40°C to +85°C	9 WLP	AAN
MAX98360CENL+T	-40°C to +85°C	9 WLP	AAN
MAX98360DENL+	-40°C to +85°C	9 WLP	AAM
MAX98360DENL+T	-40°C to +85°C	9 WLP	AAM
MAX98360AEFB+	-40°C to +85°C	10 FC2QFN	AAAA
MAX98360AEFB+T	-40°C to +85°C	10 FC2QFN	AAAA
MAX98360BEFB+	-40°C to +85°C	10 FC2QFN	AAAB
MAX98360BEFB+T	-40°C to +85°C	10 FC2QFN	AAAB
MAX98360CEFB+	-40°C to +85°C	10 FC2QFN	AAAC
MAX98360CEFB+T	-40°C to +85°C	10 FC2QFN	AAAC
MAX98360DEFB+	-40°C to +85°C	10 FC2QFN	AAAD
MAX98360DEFB+T	-40°C to +85°C	10 FC2QFN	AAAD

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/19	Initial release	—
1	12/19	Updated *Benefits and Features* section, changed Spread-Spectrum Bandwidth from ±20kHz typ to ±14kHz typ in the *Electrical Characteristics* table, added FC2QFN package to *Package Information*, *Pin Configurations*, *Pin Description*, and *Ordering Information* table	1, 2, 5, 15, 16, 38
2	3/20	Removed the "continuous current in or out" line items from the *Absolute Maximum Ratings* section, updated *Typical Operating Characteristics* 24 through 29, changed Class-D switching frequency conditions from "V_{DD} = 2.5V to 5.5V" to "V_{DD} = 3.0V to 5.5V", and removed GAIN_SLOT pin from Input Leakage Current conditions, and enumerated V_{GAIN_SLOT} symbols in the *Electrical Characteristics* table, added *GAIN_SLOT Pin* section	2, 5–8, 10, 11, 19–40