Click here for production status of specific part numbers.

MAX86150

Integrated Photoplethysmogram and Electrocardiogram Bio-Sensor Module For Mobile Health

General Description

The MAX86150 is an integrated electrocardiogram, pulse oximeter, heart rate monitor sensor module. It includes internal LEDs, photodetector, and low-noise electronics with ambient light rejection. The MAX86150 helps ease design-in to mobile and wearable devices.

The MAX86150 operates on a 1.8V supply voltage with a separate power supply for the internal LEDs. Communication to and from the module is entirely through a standard I²C-compatible interface. The module can be shut down through software with near zero standby current, allowing the power rails to remain powered at all times.

Applications

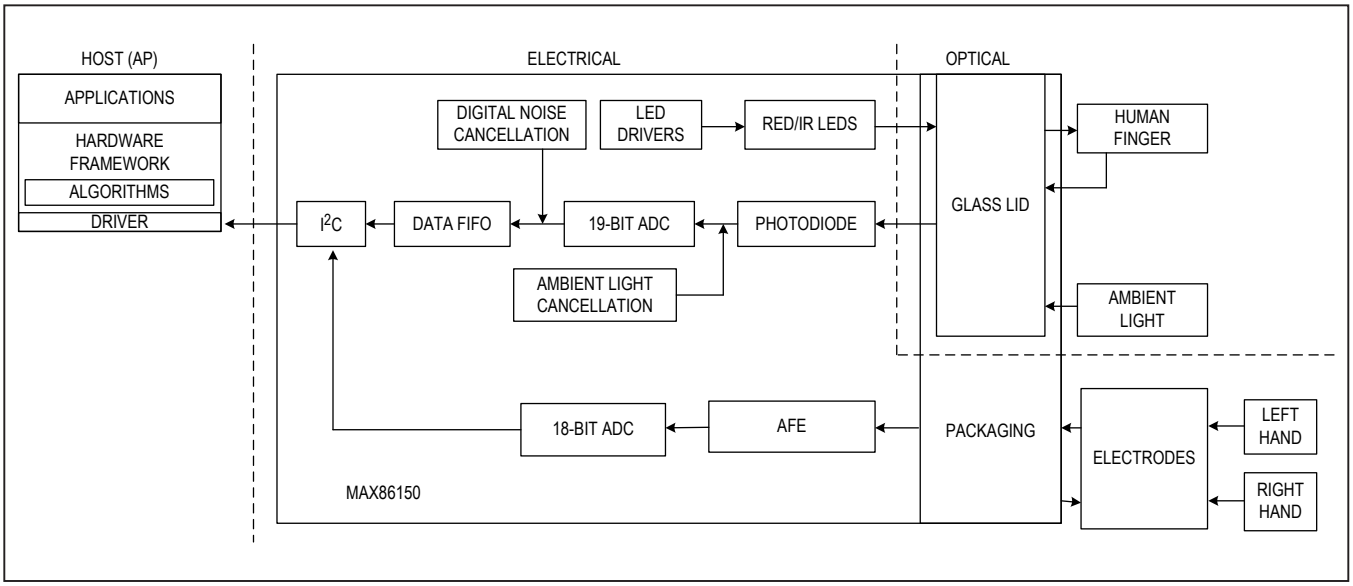
- Smartphones
- Tablets
- Wearable Devices
- Fitness Assistant Devices

Benefits and Features

- Electrocardiogram (ECG) Optimized for Dry Electrode Operation
- Reflective Heart Rate Monitor and Medical-Grade Pulse Oximeter
- Miniature 3.3mm x 5.6mm x 1.3mm 22-pin Optical Module
  - Optical-Grade Glass for Long-Term Optimal and Robust Performance
- Ultra-Low Power Operation for Mobile Devices
  - Ultra-Low Shutdown Current (0.7µA Typical)
- High SNR and Robust Ambient Light Cancellation
- -40°C to +85°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



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Absolute Maximum Ratings

V_{DD_ANA} to GND_ANA.....-0.3V to +2.2V
V_{DD_DIG} to GND DIG .....-0.3V to +2.2V
V_{DD_ANA} to V_{DD_DIG}..... V_{DD_DIG} - 0.3V to V_{DD_DIG} + 0.3V
GND_ANA to GND_DIG..... GND_DIG - 0.3V to GND_DIG + 0.3V
PGND to GND_ANA.....-0.3V to +0.3V
V_{LED} to PGND .....-0.3V to +6.0V
ECG_P, ECG_N, ECG_C to GND_ANA .....-0.3V to +2.2V
C1_P, C1_N to GND_ANA .....-0.3V to +2.2V
IDRV_P, IDRV_N to GND_ANA .....-0.3V to +2.2V
V_{REF} to GND_ANA .....-0.3V to +2.2V
Output Short-Circuit Duration .....Continuous
Continuous Input Current Into Any Pin.....±20mA
SDA, SCL, INTB to GND_ANA .....-0.3V to +6.0V
OESIP (derate 5.5mW/°C above +70°C) .....-40°C to 85°C
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +105°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 22 OLGA	
Package Code	F223A5+1
Outline Number	**21-100071**
Land Pattern Number	**90-100024**
THERMAL RESISTANCE, FOUR LAYER BOARD:	
Junction-to-Ambient (θ_{JA})	180°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	150°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 3.3V, V_{GND_ANA} = V_{GND_DIG} = V_{PGND} = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power Supply Voltage	V_{DD}	Guaranteed by RED and IR count tolerance	1.7	1.8	2.0	V
LED Supply Voltage	V_{LED}	Guaranteed by PSRR of LED driver	3.1	3.3	5	V
V_{DD} Supply Current	I_{DD}	Heart rate/SpO_2 mode; PPG_LED_PW = 50µs; PPG_SR = 100sps; LED driver = 0mA		400	750	µA
		Heart rate/SpO_2 mode; PPG_LED_PW = 50µs; PPG_SR = 10sps; LED driver = 0mA		400		
		ECG sample rate = 200Hz		340	750	
VLED Supply Current	I_{LED}	Heart rate mode; PPG_LED_PW = 50µs; PPG_SR = 100sps, LED driver = 0mA		0.03	1	µA
		Heart rate mode; PPG_LED_PW = 50µs; PPG_SR = 100sps, LED driver = 50mA		350		
		Heart rate mode; PPG_LED_PW = 50µs; PPG_SR = 10sps, LED driver = 50mA		50		
	ILED	SpO_2 mode; PPG_LED_PW = 50µs; PPG_SR = 100sps, LED driver = 50mA		750		
	I_{LED}	SpO_2 mode; PPG_LED_PW = 50µs; PPG_SR = 10sps; LED driver = 50mA		80		
V_{DD} Current in Shutdown	I_{SHDN}	T_A = +25°C		0.5	12	µA
V_{LED} Current in Shutdown	$I_{SHDNVLED}$	T_A = +25°C		0	1	µA
Reference Voltage (Note 2)	V_{REF}	Bypass to GND_ANA with 1µF	1.192	1.204	1.215	V
PULSE OXIMETRY/HEART RATE SENSOR CHARACTERISTICS						
ADC Resolution				19		bits
Red ADC Count (Note 3)	RED_C	Proprietary ATE setup, LED2_PA = 0x16, PPG_LED_PW = 50µS, PPG_SR = 100sps, T_A = +25°C	120,072	140,072	160,072	Counts
IR ADC Count (Note 3)	IR_C	Proprietary ATE setup, LED1_PA = 0x16, PPG_LED_PW = 50µS, PPG_SR = 100sps, T_A = +25°C	136,072	156,072	176,072	Counts
Dark Current Counts	DC_C	ALC = ON, LED2_PA = LED1_PA = 0x00, PPG_LED_PW = 50µS, PPG_SR = 100sps, PPG_ADC_RGE[1:0] = 8µA, T_A = +25°C		0.0004	0.01	% of FS
RED/IR ADC Count - PSRR (VDD)	PSRR_VDD	Propriety ATE setup, 1.7V < V_{DD} < 2.0V, LED1_PA = 0x16, LED2_PA = 0x16, PPG_LED_PW = 50µS, PPG_SR = 100sps, T_A = +25°C		0.05	0.5	% of FS
RED/IR ADC Count—PSRR (LED Driver Outputs)	PSRR_LED	Propriety ATE setup, 3.1V < V_{LED} < 5V, LED1_PA = 0x16, LED2_PA = 0x16, PPG_LED_PW = 50µS, PPG_SR = 100sps, T_A = +25ºC		0.05	0.5	% of FS
ADC Clock Frequency	CLK		9.633	9.8304	10.027	MHz

Electrical Characteristics (continued)

(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 3.3V, V_{GND_ANA} = V_{GND_DIG} = V_{PGND} = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IR LED (LED1) CHARACTERISTICS (Note 4)						
LED Peak Wavelength	λ_P	I_{LED} = 20mA, T_A = +25°C	870	880	900	nm
RED LED (LED2) CHARACTERISTICS (Note 4)						
LED Peak Wavelength	λ_P	I_{LED} = 20mA, T_A = +25°C	650	660	670	nm
LED DRIVERS						
LED Current Resolution				8		bits
LED Drive Current	I_{LED}	LEDx_RGE = 0x0		50		mA
		LEDx_RGE = 0x1		100		
ECG (Note 5)						
ADC Resolution				18		bits
Gain	G	V_{IN} = ±10mVDC, T_A = +25°C, V_{DIFF} = 0mV (Note 6)	72	76	80	V/V
Gain Error		V_{IN} = 20m$V_{P-P,AC}$ ±400mVDC, I_{A_GAIN} = 9.5, PGA_GAIN = 8, f = 84Hz, T_A = +25°C			2.2	%
DC Differential Input Range		V_{IN} = 20m$V_{P-P,AC}$, f = 84Hz, gain error < 2.2%, T_A = +25°C	-400		+400	mV
CMRR		Balanced Inputs, 60Hz with ±300mV differential DC offset, per AAMI/IEC standard, lead biasing enabled		136		dB
		51kΩ // 47nF imbalance, 60Hz with ±300mV differential DC offset, per AAMI/IEC standard, lead biasing enabled		78		dB
DC CMRR		Gain = 76V/V, input pins tied together (no electrodes), 0.2V < V_{IN} < 1.0V	80	120		dB
DC PSRR		Gain = 76V/V, input pins tied together (no electrodes), 1.7V < V_{DD} < 2.0V	70	100		
AC PSRR		ECG_P/N tied together, AC signal at 60Hz, 10mV_{P-P} to V_{DD}, lead bias disabled		95		dB
Input Impedance		ECG_P or ECG_N to GND_ANA, DC, lead biasing enabled		100		MΩ
Input Referred Noise		Gain = 76V/V, inputs tied together on chip, ECG sample rate = 400sps (Register 0x3C = 0x02), 0.5Hz to 100Hz		0.76		μV_{RMS}

Electrical Characteristics (continued)

(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 3.3V, V_{GND_ANA} = V_{GND_DIG} = V_{PGND} = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL CHARACTERISTICS (SDA, SCL, INTB)						
Output Low Voltage SDA, INTB	V_{OL}	I_{SINK} = 6mA			0.4	V
I²C Input Voltage Low	V_{IL_I2C}	SDA, SCL			0.4	V
I²C Input Voltage High	V_{IH_I2C}	SDA, SCL	1.4			V
Input Hysteresis (Note 3)	V_{HYS}	SDA, SCL		200		mV
Input Capacitance (Note 3)	C_{IN}	SDA, SCL		10		pF
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C (SDA, SCL)		0.01	1	µA
		V_{IN} = V_{DD}, T_A = +25°C (SDA, SCL)		0.01	1	
I²C TIMING CHARACTERISTICS (SDA, SCL) (Note 4, Figure 1)						
I²C Write Address				BC		Hex
I²C Read Address				BD		Hex
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	C_B				400	pF
SDA and SCL Receiving Rise Time	t_R		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F		20 + 0.1C_B		300	ns

Electrical Characteristics (continued)

(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 3.3V, V_{GND_ANA} = V_{GND_DIG} = V_{PGND} = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.
Note 2: Internal reference only.
Note 3: Specifications are guaranteed by Maxim Integrated's bench characterization and by 100% production test using proprietary ATE setup and conditions.
Note 4: For design guidance only. Not production tested.
Note 5: Test conditions: ECG sample rate = 1600Hz, ECG_ADC_OSR[1:0] = 00 (OSR = 16), ECG_ADC_CLK = 0 (25.6kHZ), IA_GAIN[1:0] = 01 (IA_GAIN = 9.5), and PGA_ECG_GAIN[1:0] = 11 (PGA_GAIN = 8), V_{CM} = 600mV, unless otherwise noted.
Note 6: For measurements with DC difference as input, the highpass filter function is disabled.

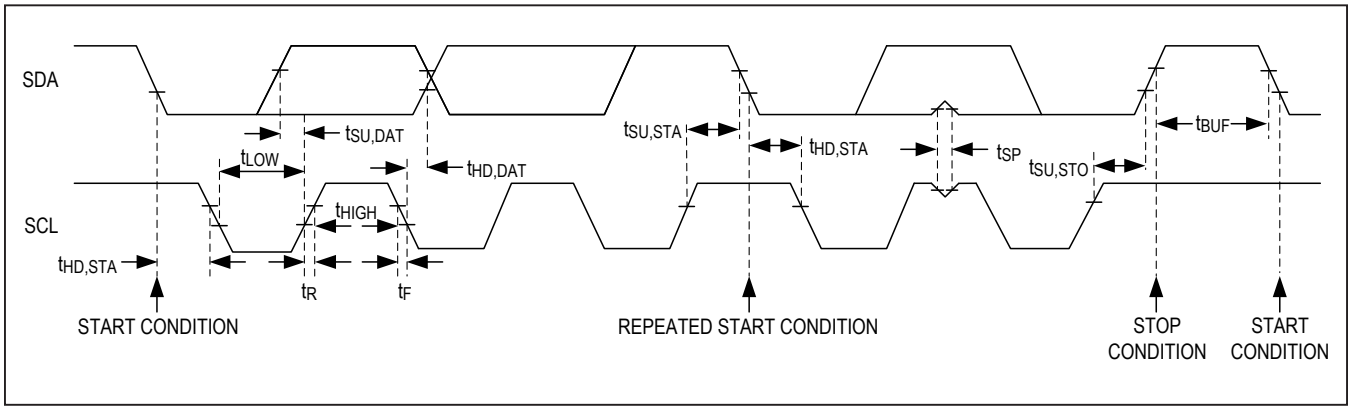


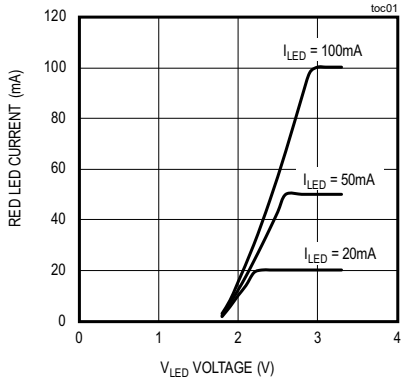
Figure 1. I²C-Compatible Interface Timing Diagram

Typical Operating Characteristics

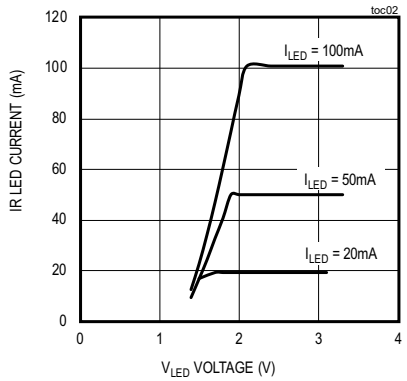
(T_A = +25°C, unless otherwise noted.)

Photoplethysmogram (PPG)

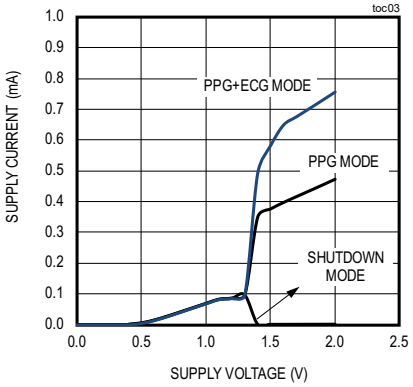
RED LED SUPPLY HEADROOM



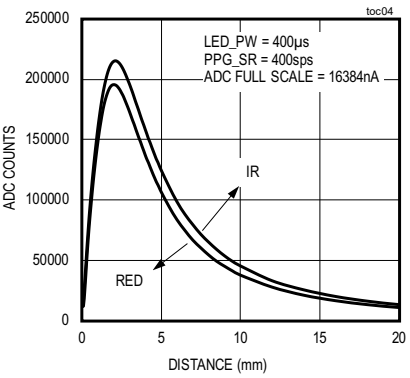
IR LED SUPPLY HEADROOM



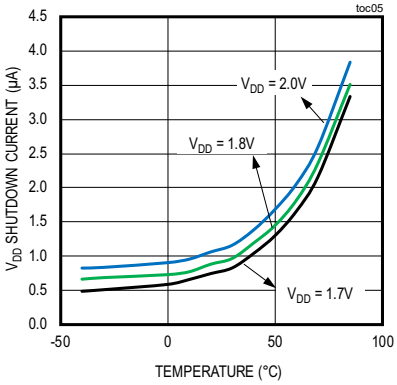
V_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE



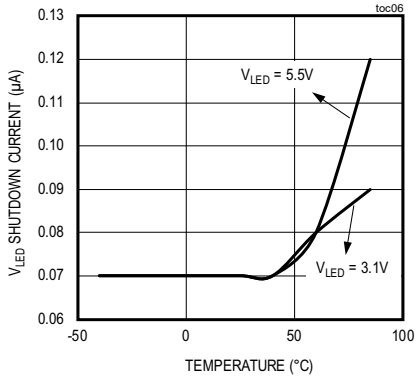
DC COUNTS vs. DISTANCE FROM WHITE HIGH IMPACT STYRENE CARD



V_{DD} SHUTDOWN CURRENT vs. TEMPERATURE



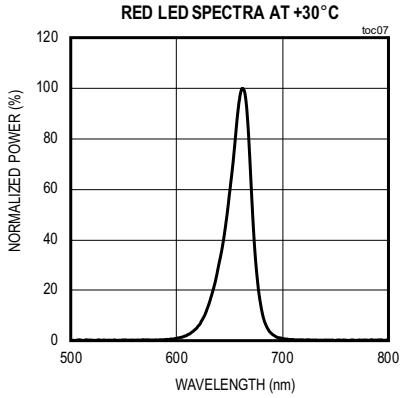
V_{LED} SHUTDOWN CURRENT vs. TEMPERATURE

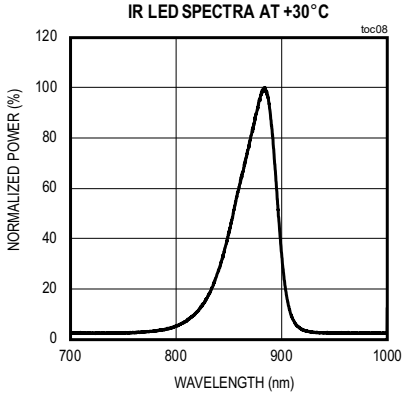


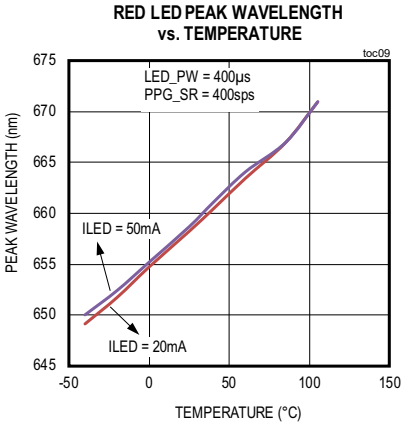
Typical Operating Characteristics (continued)

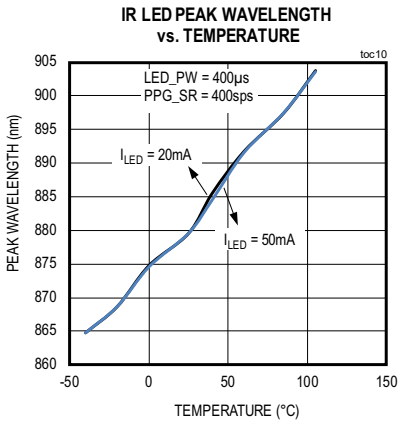
(T_A = +25°C, unless otherwise noted.)

Photoplethysmogram (PPG)







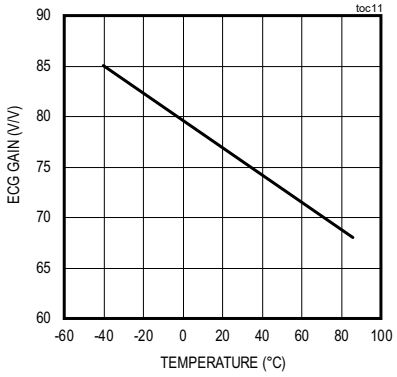


Typical Operating Characteristics (continued)

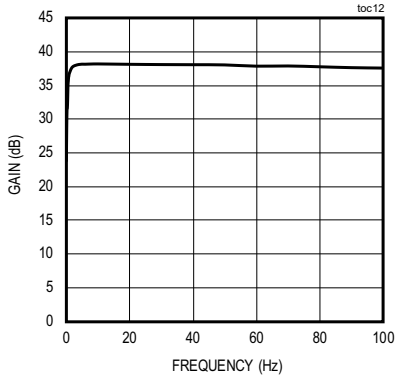
(T_A = +25°C, unless otherwise noted.)

Electrocardiogram (ECG)

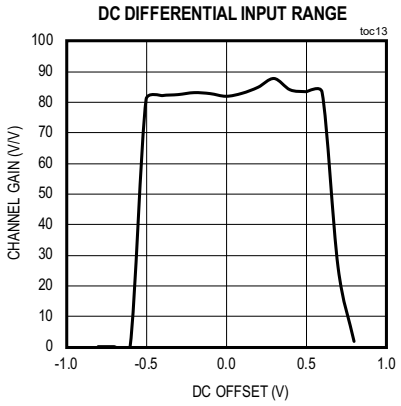
ECG CHANNEL GAIN vs. TEMPERATURE



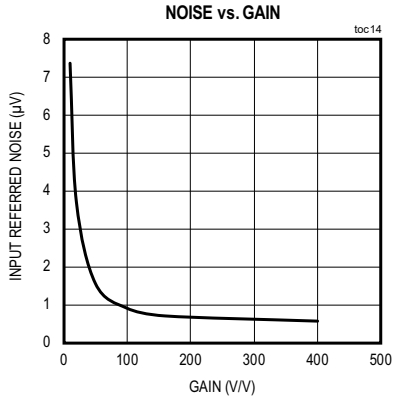
ECG CHANNEL GAIN vs. FREQUENCY



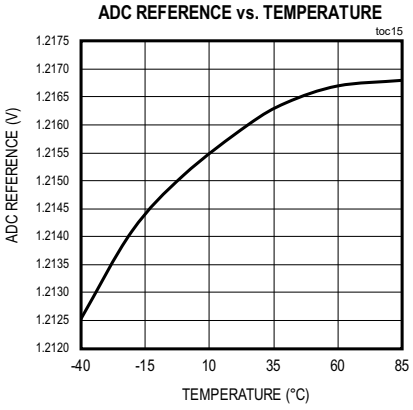
DC DIFFERENTIAL INPUT RANGE



NOISE vs. GAIN

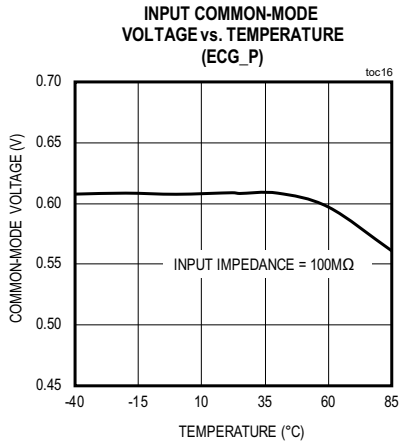


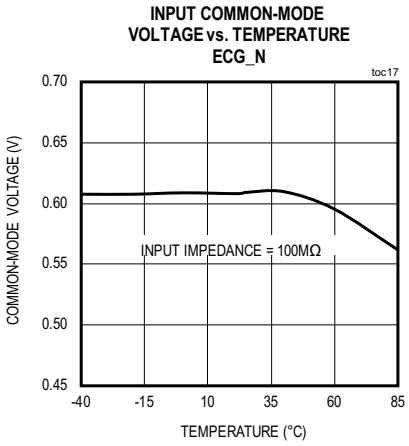
ADC REFERENCE vs. TEMPERATURE



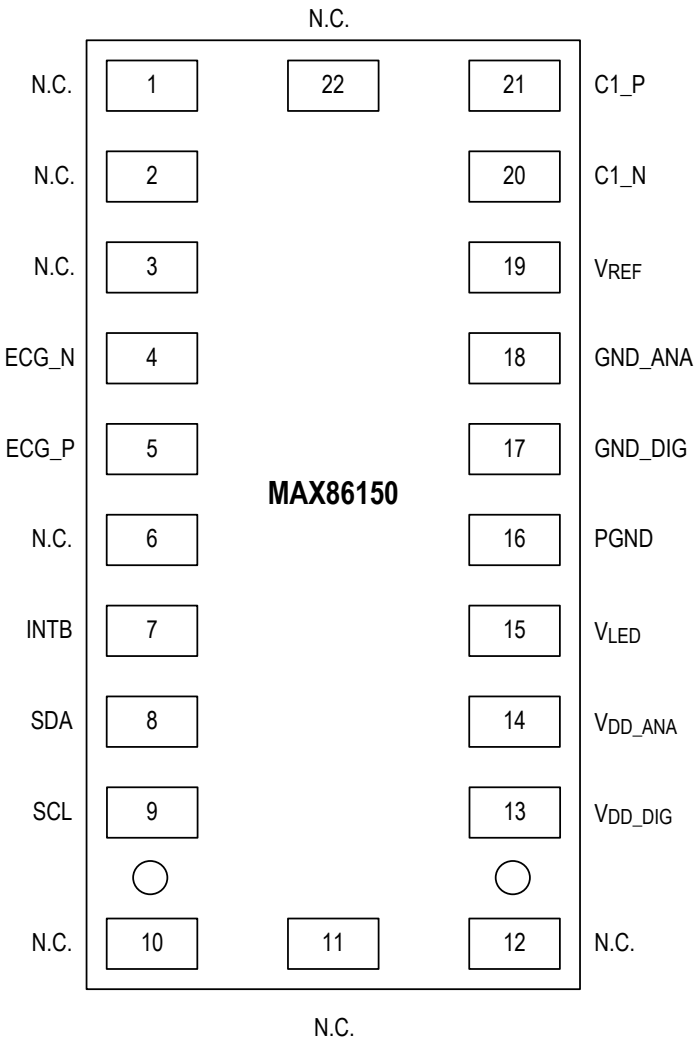
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





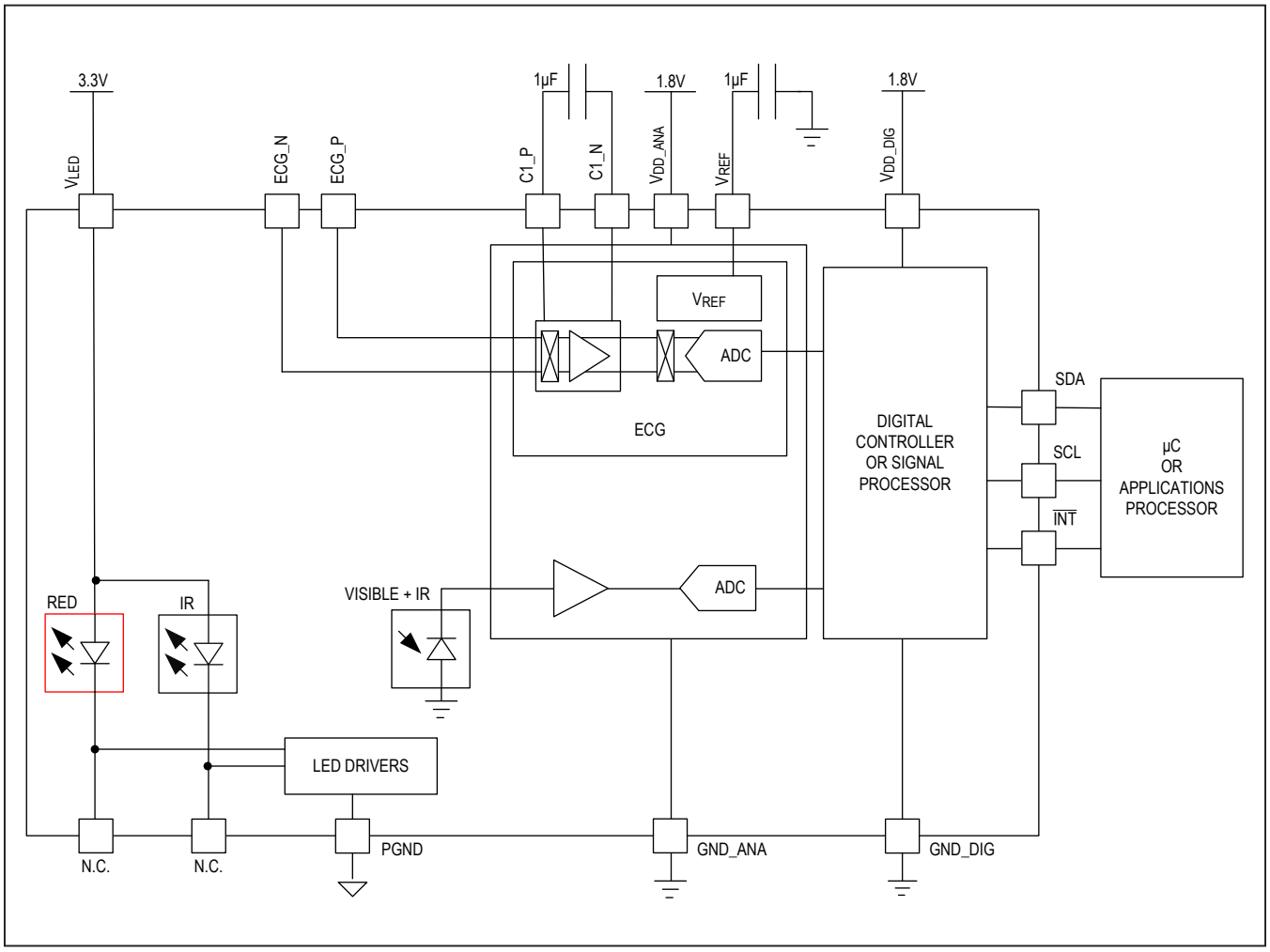
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
N.C.		
1–3, 6, 10–12, 22	N.C.	No Connection. Connect to an unconnected PCB pad for mechanical stability. N.C. pin should not be connected to any signal, power, or ground pins.
ECG		
5	ECG_P	Positive ECG Electrode
4	ECG_N	Negative ECG Electrode
21	C1_P	Capacitor for ECG HPF. Connect to C1_N through a 1µF capacitor.
20	C1_N	Capacitor for ECG HPF. Connect to C1_P through a 1µF capacitor.
CONTROL INTERFACE		
8	SDA	I^2C Data
9	SCL	I^2C Clock
7	INTB	Open-Drain Interrupt
POWER		
13	V_{DD_DIG}	Digital Logic Supply. Connect to externally regulated supply. Bypass to GND_DIG.
17	GND_DIG	Digital Logic and Digital Pad Return. Connect to Ground.
14	V_{DD_ANA}	Analog Supply. Connect to externally regulated supply. Bypass to GND_ANA.
18	GND_ANA	Analog Power Return. Connect to Ground.
15	V_{LED}	LED Power Supply Input. Connect to external battery supply. Bypass to PGND.
16	PGND	LED Power Return. Connect to Ground.
REFERENCE		
19	V_{REF}	Internal Reference Decoupling Point. Bypass to GND_ANA.

Functional Diagrams



Detailed Description

The MAX86150 is a complete electrocardiogram, pulse oximetry, and heart rate sensor system solution module designed for the demanding requirements of mobile devices. The MAX86150 maintains a very small total solution size without sacrificing performance. Minimal external hardware components are necessary for integration into a mobile device. The MAX86150 is fully adjustable through software registers, and the digital output data is stored in a 32-deep FIFO within the device. The FIFO allows the MAX86150 to be connected to a microcontroller or processor on a shared bus, where the data is not being read continuously from the MAX86150's registers.

SpO_2 Subsystem

The SpO_2 subsystem in the MAX86150 is composed of ambient light cancellation (ALC), a continuous-time sigma-delta ADC, and proprietary discrete time filter. The ALC has an internal DAC to cancel ambient light and increase the effective dynamic range. The internal ADC is a continuous time oversampling sigma delta converter with 19-bit resolution. The ADC output data rate can be programmed from 10sps (samples per second) to 3200sps. The MAX86150 includes a proprietary discrete time filter to reject 50Hz/60Hz interference and slow moving residual ambient noise.

LED Driver

The MAX86150 integrates red and infrared LED drivers to modulate LED pulses for SpO_2 and HR measurements. The LED current can be programmed from 0mA to 100mA with proper V_{LED} supply voltage. The LED pulse width can be programmed from 50µs to 400µs to optimize accuracy of results and power consumption based on use cases.

Proximity Function

The MAX86150 includes a proximity function to save power and reduce visible light emission when the user's finger is not on the sensor. Proximity function is enabled by setting PROX_INT_EN to 1. When the SpO_2 or HR function is initiated, the IR LED is turned on in proximity mode with a drive current set by the PILOT_PA register. When an object is detected by exceeding the IR ADC count threshold (set in the PROX_INT_ THRESH register), PROX_INT interrupt is asserted and the part transitions automatically to the normal SpO_2/HR mode. To reenter PROX mode, a new SpO_2 or HR reading must be initiated (even if the value is the same). The proximity function can be disabled by resetting PROX_INT_EN to 0. In that case, when the SpO_2 or HR function is initiated in the FIFO Data Control registers, the SpO_2 or HR mode begins immediately.

Electrocardiogram (ECG)

The ECG subsystem in the MAX86150 is designed specifically for mobile applications. It features single-lead ECG technology that is optimized for dry electrode operation. It is comprised of Maxim proprietary analog front end (AFE), which includes an 18-bit ADC. Figure 2 shows the ECG Subsystem Block Diagram. The primary function of the AFE is to digitize heart signals. This process is complicated by the need to reject interference from strong RF sources, common-mode line frequency, signals from other muscles, and electrical noise. The electrical connections to the patient must not create a shock hazard or interfere with other equipment that might be connected to the device. The ECG subsystem also includes an on-chip highpass filter, which facilitates high SNR in real applications. The ADC output data rate can be programmed from 200sps (samples per second) to 3200sps.

The output of the ADC is an 18-bit digital representation of the input voltage. Each data sample takes three bytes in the FIFO, and the data is right-justified and in bipolar two's-complement format.

To calculate the equivalent differential input voltage of the ADC, the formula is as follows:

V_INPUT = ADC_CODE x
12.247µV/IA_GAIN/PGA_GAIN

where ADC_CODE is converted to a bipolar integer decimal format, which can be positive or negative. Note that only one gain setting, IA_GAIN = 9.5 and PGA_GAIN = 8, is trimmed to a tight tolerance at the factory, and the other gains are typical expected values only.

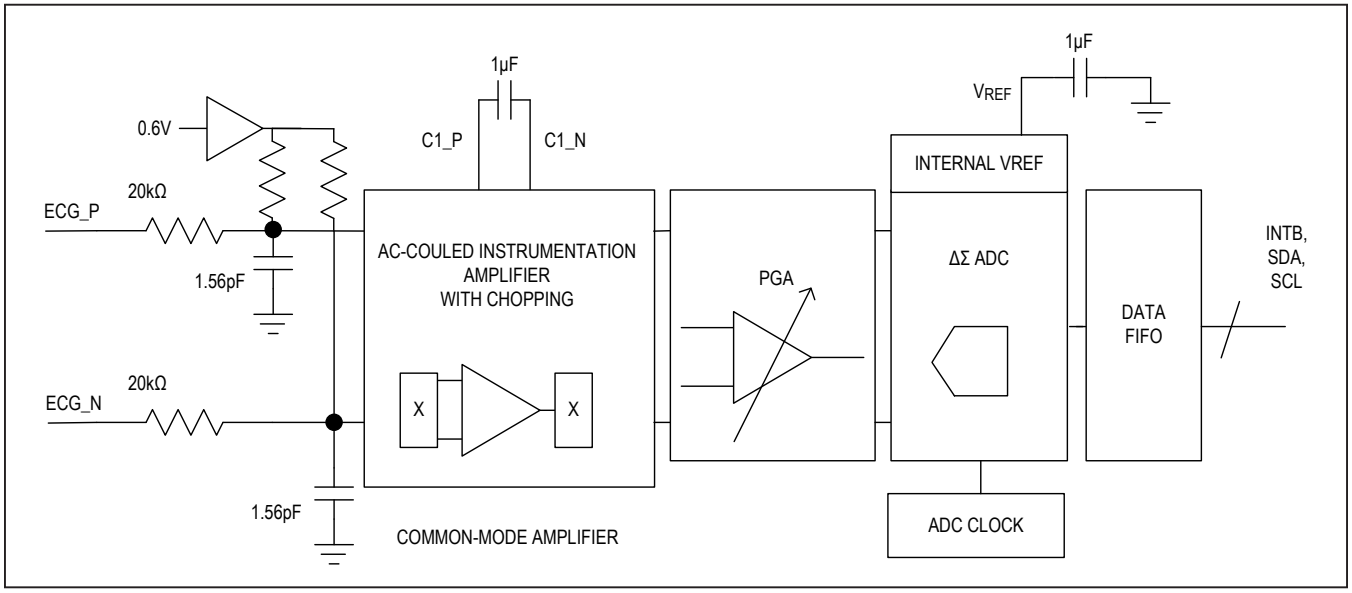


Figure 2. MAX86150 ECG Subsystem Block Diagram

ECG and PPG Synchronization

The MAX86155 allows for a simultaneous and synchronous collection of PPG and ECG signals. If the ECG sample rate is set higher than the PPG sample rate, the PPG sample rate defaults to the ECG sample rate if it can be supported. If the ECG sample rate is set above the maximum allowable PPG sample rate, then the PPG sample rate is set to the highest supported rate, and redundant data will be present in the FLEX FIFO. See Register 0x0E configuration table “Maximum Sample rates Supported for all the Pulse Widths and number of LEDs” to determine which sample rate the PPG defaults to if the ECG is set higher. For example, if the ECG sample rate is set to 400Hz, and PPG registers are set to 0x0E = 0xDB (Two LEDs, single pulse, PPG_SR = 100sps, PPG_LED_PW = 400µs) and Register 0x0F is set to 0x00 (SMP_AVE = 000, no sample averaging), then the PPG defaults to 400Hz, as this configuration is supported per the table in 0x0E Register description.

Register Map

ADDRESS	NAME	MSB							LSB
Status Registers									
0x00	**Interrupt Status 1[7:0]**	A_FULL_	PPG_ RDY_	ALC_OVF_	PROX_INT_	—	—	—	PWR_ RDY_
0x01	**Interrupt Status 2[7:0]**	VDD_ OOR_	—	—	—	—	—	—	—
0x02	**Interrupt Enable 1[7:0]**	A_FULL_ EN_	PPG_ RDY_EN_	ALC_OVF_ EN_	PROX_INT_ EN_	—	—	—	—
0x03	**Interrupt Enable 2[7:0]**	VDD_ OOR_EN_	—	—	—	—	—	—	—
FIFO Registers									
0x04	**FIFO Write Pointer[7:0]**	—	—	—	FIFO_WR_PTR_[4:0]				
0x05	**Overflow Counter[7:0]**	—	—	—	OVF_COUNTER_[4:0]				
0x06	**FIFO Read Pointer[7:0]**	—	—	—	FIFO_RD_PTR_[4:0]				
0x07	**FIFO Data Register[7:0]**	FIFO_DATA_[7:0]							
0x08	**FIFO Configuration[7:0]**	—	A_FULL_ CLR_	A_FULL_ TYPE_	FIFO_ ROLLS_ ON_FULL_	FIFO_A_FULL_[3:0]			
FIFO Data Control									
0x09	**FIFO Data Control Register 1[7:0]**	FD2_[3:0]				FD1_[3:0]			
0x0A	**FIFO Data Control Register 2[7:0]**	FD4_[3:0]				FD3_[3:0]			
System Control									
0x0D	**System Control[7:0]**	—	—	—	—	—	FIFO_EN_	SHDN_	RESET_
PPG Configuration									
0x0E	**PPG Configuration 1[7:0]**	PPG_ADC_RGE_[1:0]		PPG_SR_[3:0]				PPG_LED_PW_ [1:0]	
0x0F	**PPG Configuration 2[7:0]**	—	—	—	—	—	SMP_AVE_[2:0]		
0x10	**Prox Interrupt Threshold[7:0]**	PROX_INT_THRESH_[7:0]							

Register Map (continued)

LED Pulse Amplitude									
0x11	**LED1 PA[7:0]**	LED1_PA_[7:0]							
0x12	**LED2 PA[7:0]**	LED2_PA_[7:0]							
0x14	**LED Range[7:0]**	—	—	—	—	LED2_RGE_[7:0]		LED1_RGE_[7:0]	
0x15	**LED PILOT PA[7:0]**	PILOT_PA_[7:0]							
ECG Configuration									
0x3C	**ECG Configuration 1[7:0]**	—	—	—	—	—	ECG_ ADC_ CLK_	ECG_ADC_OSR_ [1:0]	
0x3E	**ECG Configuration 3[7:0]**	—	—	—	—	PGA_ECG_ GAIN_[1:0]		IA_GAIN_[1:0]	
Part ID									
0xFF	**Part ID[7:0]**	PART_ID_[7:0]							

Register Details

Interrupt Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	PPG_RDY	ALC_OVF	PROX_INT	—	—	—	PWR_RDY
Reset	0x0	0x0	0x0	0x0	—	—	—	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	—	—	—	Read Only

A_FULL: FIFO Almost Full Flag

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the FIFO buffer overflows the threshold set by FFIFO_A_FULL[3:0] on the next sample. This bit is cleared when the Interrupt Status 1 register is read. It is also cleared when FIFO_DATA register is read, if A_FULL_CLR = 1

PPG_RDY: New PPG FIFO Data Ready

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	In SpO_2 and HR modes, this interrupt triggers when there is a new sample in the data FIFO. The interrupt is cleared by reading the Interrupt Status 1 register (0x00), or by reading the FIFO_DATA register.

ALC_OVF: Ambient Light Cancellation Overflow

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	This interrupt triggers when the ambient light cancellation function of the SpO_2/HR photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC. The interrupt is cleared by reading the Interrupt Status 1 register (0x00).

PROX_INT: Proximity interrupt

If PROX_INT is masked then the prox mode is disabled and the select PPG begins immediately. This bit is cleared when the Interrupt Status 1 Register is read.

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the proximity threshold has been crossed when in proximity mode.

PWR_RDY: Power Ready Flag

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that VBATT went below the UVLO threshold. This bit is not triggered by a soft reset. This bit is cleared when Interrupt Status 1 Register is read.

Interrupt Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	VDD_OOR	—	—	—	—	ECG_RDY	—	—
Reset	0x0	—	—	—	—	0x0	—	—
Access Type	Read Only	—	—	—	—	Read Only	—	—

VDD_OOR: VDD Out-of-Range Flag

This flag checks if the VDD_ANA supply voltage is outside supported range.

VALUE	ENUMERATION	DECODE
0	OFF	VDD_ANA between range.
1	ON	Indicated that VDD_ANA is greater than 2.05V or less than 1.65V. This bit is automatically cleared when the Interrupt Status 2 register is read. The detection circuitry has a 10ms delay time and continues to trigger as long as the VDD_ANA is out of range.

ECG_RDY: New ECG FIFO Data Ready

This flag checks if the VDD_ANA supply voltage is outside supported range.

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the ECG ADC has finished it’s existing conversion.

Interrupt Enable 1 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	PPG_RDY_EN	ALC_OVF_EN	PROX_INT_EN	—	—	—	—
Reset	0x0	0x0	0x0	0x0	—	—	—	—
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	—	—	—	—

A_FULL_EN: FIFO Almost Full Flag Enable

VALUE	ENUMERATION	DECODE
0	OFF	A_FULL interrupt is disabled
1	ON	A_FULL interrupt is enabled

PPG_RDY_EN: New PPG FIFO Data Ready Interrupt enable

VALUE	ENUMERATION	DECODE
0	OFF	PPG_RDY interrupt is disabled
1	ON	PPG_RDY interrupt is enabled.

ALC_OVF_EN: Ambient Light Cancellation (ALC) Overflow Interrupt Enable

The ALC_OVF flag is triggered when the ambient light cancellation function has reached its maximum limit due to overflow. At this point, the ADC output is affected by the ambient light.

VALUE	ENUMERATION	DECODE
0	OFF	ALC_OVF interrupt is disabled
1	ON	ALC_OVF interrupt is enabled

PROX_INT_EN: Proximity Interrupt Enable

When the FIFO Data Control Register is configured to initiate PPG measurement, the IR LED is turned on in proximity mode with a drive current set by the PILOT_PA register. When an object is detected by exceeding the IR ADC count threshold (set in the PROX_INT_ THRESH register), PROX_INT interrupt is asserted and the part transitions to the normal SpO_2/HR mode.

VALUE	ENUMERATION	DECODE
0	OFF	PROX_INT interrupt is disabled
1	ON	PROX_INT interrupt is enabled

Interrupt Enable 2 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	VDD_OOR_ EN	—	—	—	—	ECG_ RDY_ EN	—	—
Reset	0x0	—	—	—	—	0x0	—	—
Access Type	Write, Read	—	—	—	—	Write, Read	—	—

VDD_OOR_EN: VDD Out-of-Range Indicator Enable

VALUE	ENUMERATION	DECODE
0	OFF	Disables the VDD_OVR interrupt
1	ON	Enables the VDD_OVR interrupt

ECG_RDY_EN: New ECG FIFO Data Ready Interrupt Enable

VALUE	ENUMERATION	DECODE
0	OFF	ECG_RDY interrupt is disabled
1	ON	ECG_RDY interrupt is enabled

FIFO Write Pointer (0x04)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	FIFO_WR_PTR[4:0]				
Reset	—	—	—	0x00				
Access Type	—	—	—	Write, Read				

FIFO_WR_PTR: FIFO Write Pointer

This points to the location where the next sample is written. This pointer advances for each sample pushed on to the FIFO.

Overflow Counter (0x05)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	OVF_COUNTER[4:0]				
Reset	—	—	—	0x00				
Access Type	—	—	—	Read Only				

OVF_COUNTER: FIFO Overflow Counter

When FIFO is full, any new samples result in new or old samples getting lost depending on FIFO_ROLLS_ON_FULL. OVF_COUNTER counts the number of samples lost. It saturates at 0x1F.

FIFO Read Pointer (0x06)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	FIFO_RD_PTR[4:0]				
Reset	—	—	—	0x00				
Access Type	—	—	—	Write, Read				

FIFO_RD_PTR: FIFO Read Pointer

The FIFO Read Pointer points to the location from where the processor gets the next sample from the FIFO through the I^2C interface. This advances each time a sample is popped from the FIFO. The processor can also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO.

FIFO Data Register (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0x00							
Access Type	Write, Read							

FIFO_DATA: FIFO Data Register

This is a read-only register and is used to get data from the FIFO. See *FIFO Description* for more details.

FIFO Configuration (0x08)

BIT	7	6	5	4	3	2	1	0
Field	—	A_FULL_CLR	A_FULL_TYPE	FIFO_ROLLS_ON_FULL	FIFO_A_FULL[3:0]			
Reset	—	0x0	0x0	0x0	0xF			
Access Type	—	Write, Read	Write, Read	Write, Read	Write, Read			

A_FULL_CLR: FIFO Almost Full Interrupt Options

This defines whether the A-FULL interrupt should get cleared by FIFO_DATA register read.

VALUE	ENUMERATION	DECODE
0	RD_DATA_NOCLR	A_FULL interrupt does not get cleared by FIFO_DATA register read. It gets cleared by status register read.
1	RD_DATA_CLR	A_FULL interrupt gets cleared by FIFO_DATA register read or status register read.

A_FULL_TYPE: FIFO Almost Full Flag Options

This defines the behavior of the A_FULL interrupt.

VALUE	ENUMERATION	DECODE
0	AFULL_RPT	A_FULL interrupt gets asserted when the a_full condition is detected. It is cleared by status register read, but re-asserts for every sample if the a_full condition persists.
1	AFULL_ONCE	A_FULL interrupt gets asserted only when the a_full condition is detected. The interrupt gets cleared on status register read, and does not re-assert for every sample until a new a-full condition is detected.

FIFO_ROLLS_ON_FULL: FIFO Rolls on Full Options

This bit controls the behavior of the FIFO when the FIFO becomes completely filled with data.

When the device is in PROX mode, the FIFO always rolls on full.

- Push to FIFO is enabled when FIFO is full if FIFO_ROLLS_ON_FULL = 1 and old samples are lost. Both FIFO_WR_PTR and FIFO_RD_PTR increment for each sample after the FIFO is full.
- Push to FIFO is disabled when FIFO is full if FIFO_ROLLS_ON_FULL = 0 and new samples are lost. FIFO_WR_PTR does not increment for each sample after the FIFO is full.

VALUE	ENUMERATION	DECODE
0	OFF	The FIFO stops on full.
1	ON	The FIFO automatically rolls over on full.

FIFO_A_FULL: FIFO Almost Full Value

These bits indicate how many new samples can be written to the FIFO before the interrupt is asserted. For example, if set to 0xF, the interrupt triggers when there is 17 empty space left (15 data samples), and so on.

FIFO_A_FULL<3:0>	FREE SPACE BEFORE INTERRUPT	# OF SAMPLES IN FIFO
0000	0	32
0001	1	31
0010	2	30
0011	3	29
----	----	----
1110	14	18
1111	15	17

FIFO Data Control Register 1 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	FD2[3:0]				FD1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

FD2: FIFO Data Time Slot 2

These bits set the data type for element 2 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3 and FD4 according to the following table. For restriction on data type sequences, see the *FIFO Description* section.

FD2[3:0]	DATA TYPE	FD2[3:0]	DATA TYPE	FD2[3:0]	DATA TYPE	FD2[3:0]	DATA TYPE
0000	None	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	ECG	1101	Reserved
0010	PPG_LED2	0110	Pilot LED2	1010	Reserved	1110	Reserved
0011	Reserved	Reserved	Reserved	Reserved	Reserved	1111	Reserved

FD1: FIFO Data Time Slot 1

These bits set the data type for element 1 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3 and FD4 according to the following table. For restriction on data type sequences, see the *FIFO Description* section.

FD1[3:0]	DATA TYPE	FD1[3:0]	DATA TYPE	FD1[3:0]	DATA TYPE	FD1[3:0]	DATA TYPE
0000	None	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	ECG	1101	Reserved
0010	PPG_LED2	0110	Pilot LED2	1010	Reserved	1110	Reserved
0011	Reserved	0111	Reserved	1011	Reserved	1111	Reserved

FIFO Data Control Register 2 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	FD4[3:0]				FD3[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

FD4: FIFO Data Time Slot 4

These bits set the data type for element 4 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3 and FD4 according to the following table. For restriction on data type sequences, see the *FIFO Description* section.

FD4[3:0]	DATA TYPE	FD4<3:0>	DATA TYPE	FD4<3:0>	DATA TYPE	FD4<3:0>	DATA TYPE
0000	None	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	ECG	1101	Reserved
0010	PPG_LED2	0110	Pilot LED2	1010	Reserved	1110	Reserved
0011	Reserved	0111	Reserved	1011	Reserved	1111	Reserved

FD3: FIFO Data Time Slot 3

These bits set the data type for element 3 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3 and FD4 according to the following table. For restriction on data type sequences please refer to the *FIFO Description* section.

FD3[3:0]	DATA TYPE	FD3<3:0>	DATA TYPE	FD3<3:0>	DATA TYPE	FD3<3:0>	DATA TYPE
0000	None	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	ECG	1101	Reserved
0010	PPG_LED2	0110	Pilot LED2	1010	Reserved	1110	Reserved
0011	Reserved	0111	Reserved	1011	Reserved	1111	Reserved

System Control (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	FIFO_EN	SHDN	RESET
Reset	—	—	—	—	—	0x0	0x0	0x0
Access Type	—	—	-	—	—	Write, Read	Write, Read	Write, Read

FIFO_EN: FIFO Enable

VALUE	ENUMERATION	DECODE
0	OFF	Push to FIFO is disabled, but the read and write pointers and the data in the FIFO are all held at their values before FIFO_EN is set to 0.
1	ON	The FIFO is enabled. When this bit is set the FIFO is flushed of all old data and the new samples start loading from pointer zero.

SHDN: Shutdown Control

The part can be put into a power-save mode by setting this bit to one. While in power-save mode, all registers retain their values, and write/read operations function as normal. All interrupts are cleared to zero in this mode.

VALUE	ENUMERATION	DECODE
0	OFF	The part is in normal operation. No action taken.
1	ON	The part can be put into a power-save mode by writing a ‘1’ to this bit. While in this mode all registers remain accessible and retain their data. ADC conversion data contained in the registers are previous values. Writable registers also remain accessible in shutdown. All interrupts are cleared. In this mode the oscillator is shutdown and the part draws minimum current. If this bit is asserted during a active conversion then the conversion completes before the part shuts down.

RESET: Reset Control

When this bit is set The part under-goes a forced power-on-reset sequence. All configuration, threshold and data registers including distributed registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

VALUE	ENUMERATION	DECODE
0	OFF	The part is in normal operation. No action taken.
1	ON	The part under-goes a forced power-on-reset sequence. All configuration, threshold and data registers including distributed registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

PPG Configuration 1 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	PPG_ADC_RGE[1:0]		PPG_SR[3:0]				PPG_LED_PW[1:0]	
Reset	0x0		0x0				0x0	
Access Type	Write, Read		Write, Read				Write, Read	

PPG_ADC_RGE: SpO_2 ADC Range Control

These bits set the ADC range of the SPO2 sensor as shown in the table below.

PPG_ADC_RGE<1:0>	LSB [pA]	FULL SCALE [nA]
00	7.8125	4096
01	15.625	8192
10	31.25	16384
11	62.5	32768

PPG_SR: SpO_2 Sample Rate Control

SpO_2 Sample Rate Control

These bits set the effective sampling rate of the PPG sensor as shown in the table below.

Note: If a sample rate is set that can not be supported by the selected pulse width and LED mode then the highest available sample rate will be automatically set. The user can read back this register to confirm the sample rate.

PPG_SR<3:0>	SAMPLES PER SECOND	PULSES PER SAMPLE, N
0000	10	1
0001	20	1
0010	50	1
0011	84	1
0100	100	1
0101	200	1
0110	400	1
0111	800	1
1000	1000	1
1001	1600	1
1010	3200	1
1011	10	2
1100	20	2
1101	50	2
1110	84	2
1111	100	2

Maximum sample rates supported for all the pulse widths and number of LEDs:

NUMBER OF ADC CONVERSIONS PER SAMPLE	PPG_LED_PW = 0 (50µs)	PPG_LED_PW = 1 (100µs)	PPG_LED_PW = 2 (200µs)	PPG_LED_PW = 3 (400µs)
1 LED, N=1	3200	1600	1000	1000
2 LED, N=1	1600	800	800	400
1 LED, N=2	100	100	100	100
2 LED, N=2	100	100	100	84

PPG_LED_PW: LED Pulse Width Control

These bits set the pulse width of the LED drivers and the integration time of PPG ADC as shown in the table below.

PPG_LED_PW<1:0>	PULSE WIDTH [µs]	INTEGRATION TIME [µs]	RES BITS
00	50	50	19
01	100	100	19
10	200	200	19
11	400	400	19

PPG Configuration 2 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	SMP_AVE[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

SMP_AVE: Sample Averaging Options

To reduce the amount of data throughput, adjacent samples (in each individual channel) can be averaged and decimated on the chip by setting this register.

These bits set the number of samples that are averaged on chip before being written to the FIFO.

SMP_AVE[2:0]	SAMPLE AVERAGE
000	1 (no averaging)
001	2
010	4
011	8
100	16
101	32
110	32
111	32

Prox Interrupt Threshold (0x10)

BIT	7	6	5	4	3	2	1	0
Field	PROX_INT_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

PROX_INT_THRESH: Proximity Mode Interrupt Threshold*
This register sets the IR ADC count that triggers the beginning of the PPG mode specified in the FIFO Data Control Register. The threshold is defined as the 8 MSB bits of the ADC count. For example, if PROX_INT_THRESH[7:0] = 0x01, then an ADC value of 1023 (decimal) or higher triggers the PROX interrupt. If PROX_INT_THRESH[7:0] = 0xFF, then only a saturated ADC triggers the interrupt.

LED1 PA (0x11)

BIT	7	6	5	4	3	2	1	0
Field	LED1_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED1_PA: LED 1 (IR) Current Pulse Amplitude.

These bits set the nominal current pulse amplitude of LED 1 as shown in the table below.

LED1_RGE[1:0]	00 (50mA)	01 (100mA)
LED1_PA[7:0]	LED Current [mA]	LED Current [mA]
00000000	0	0
00000001	0.2	0.4
00000010	0.4	0.8
00000011	0.6	1.2
.....		
11111100	50.4	100.8
11111101	50.6	101.2
11111110	50.8	101.6
11111111	51	102
LSB	0.2	0.4

LED2 PA (0x12)

BIT	7	6	5	4	3	2	1	0
Field	LED2_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED2_PA: LED 2 (RED) Current Pulse Amplitude

These bits set the nominal current pulse amplitude of LED 2 as shown in the table below.

LED2_RGE[1:0]	00(50mA)	01(100mA)
LED2_PA[7:0]	LED Current[mA]	LED Current[mA]
00000000	0	0
00000001	0.2	0.4
00000010	0.4	0.8
00000011	0.6	1.2
.....		
11111100	50.4	100.8
11111101	50.6	101.2
11111110	50.8	101.6
11111111	51	102
LSB	0.2	0.4

LED Range (0x14)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	LED2_RGE[1:0]		LED1_RGE[1:0]	
Reset	—	—	—	—	0x00		0x00	
Access Type	—	—	—	—	Write, Read		Write, Read	

LED2_RGE: LED 2 Current Control

Range selection of the LED current. Refer to LED2_PA[7:0] for more details.

LED2_RGE<1:0>	LED CURRENT (mA)
00	50
01	100
10	Not Applicable
11	Not Applicable

LED1_RGE: LED 1 Current Control

Range selection of the LED current. Refer to LED1_PA[7:0] for more details.

LED1_RGE<1:0>	LED CURRENT (mA)
00	50
01	100
10	Not Applicable
11	Not Applicable

LED PILOT PA (0x15)

BIT	7	6	5	4	3	2	1	0
Field	PILOT_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

PILOT_PA: Proximity Mode LED Pulse Amplitude.
The purpose of PILOT_PA[7:0] is to set the LED power during the PROX mode, as well as in Multi-LED mode. These bits set the current pulse amplitude for the pilot mode as shown in the table below.

When LED x is used, the respective LEDx_RGE<1:0> is used to control the range of the LED driver in conjunction with PILOT_PA[7:0]. For instance, if LED1 is used in the PILOT mode, then, LED1_RGE[1:0] together with PILOT_PA[7:0] will be used to set the LED1 current.

LEDx_RGE[1:0]	00 (50mA)	01 (100mA)
PILOT_PA[7:0]	LED Current[mA]	LED Current[mA]
00000000	0	0
00000001	0.2	0.4
00000010	0.4	0.8
00000011	0.6	1.2
.....		
11111100	50.4	100.8
11111101	50.6	101.2
11111110	50.8	101.6
11111111	51	102
LSB	0.2	0.4

ECG Configuration 1 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	ECG_ADC_CLK	ECG_ADC_OSR[1:0]	
Reset	—	—	—	—	—	0x0	0x0	
Access Type	—	—	—	—	—	Write, Read	Write, Read	

ECG_ADC_CLK: Please refer to ECG_ADC_OSR

ECG_ADC_OSR: ECG ADC Oversampling Ratio

These bit sets the over sampling ratio (OSR) of the ECG ADC. ECG_ADC_OSR<1:0> together with the ADC clock frequency (ECG_ADC_CLK) set the ECG sample rate. The following table shows typical values only.

{ECG_ADC_CLK, ECG_ADC_OSR[1:0]}	ECG SAMPLE RATE	FILTER BANDWIDTH (70%)	FILTER BANDWIDTH (90%)	UNITS
000	1600	420	232	Hz
001	800	210	116	Hz
010	400	105	58	Hz
011	200	52	29	Hz
100	3200	840	464	Hz
101	1600	420	232	Hz
110	800	210	116	Hz
111	400	105	58	Hz

ECG Configuration 3 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	PGA_ECG_GAIN[1:0]		IA_GAIN[1:0]	
Reset	—	—	—	—	0x0		0x2	
Access Type	—	—	—	—	Write, Read		Write, Read	

PGA_ECG_GAIN: ECG PGA Gain Options

These bit set the gain of the ECG PGA as shown below.

PGA_ECG_GAIN<1:0>	GAIN	UNITS
00	1	V/V
01	2	V/V
10	4	V/V
11	8	V/V

IA_GAIN: Instrumentation Amplifier Gain Options

These bit set the gain of the Instrumental Amplifier (IA) AFE as shown below.

IA_GAIN<1:0>	GAIN	UNITS
00	5	V/V
01	9.5	V/V
10	20	V/V
11	50	V/V

Part ID (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x1E							
Access Type	Read Only							

PART_ID: Part Identifier

This register stores the Part identifier for the chip.

Applications Information

Power Sequencing and Requirements

Power-Up Sequencing

It is recommended to power the V_{DD_ANA} supply first, followed by the V_{DD_DIG} and the LED power supplies (V_{LED}). V_{DD_ANA} and V_{DD_DIG} can be powered on at the same time. The interrupt and I²C pins can be pulled up to an external voltage even when the power supplies are not powered up.

After the power is established, an interrupt occurs to alert the system that the sensor is ready for operation. Reading the I²C interrupt register clears the interrupt, as shown in the Figure 3.

Power-Down Sequencing

The sensor is designed to be tolerant of any power-supply sequencing on power-down.

I²C Interface

The MAX86150 features an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX86150 and the master at clock rates up to 400kHz. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX86150 by transmitting the proper slave address followed by data. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX86150 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX86150 transmits the proper slave address followed by a series of nine SCL pulses.

The MAX86150 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 1000Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 1000Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX86150 from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

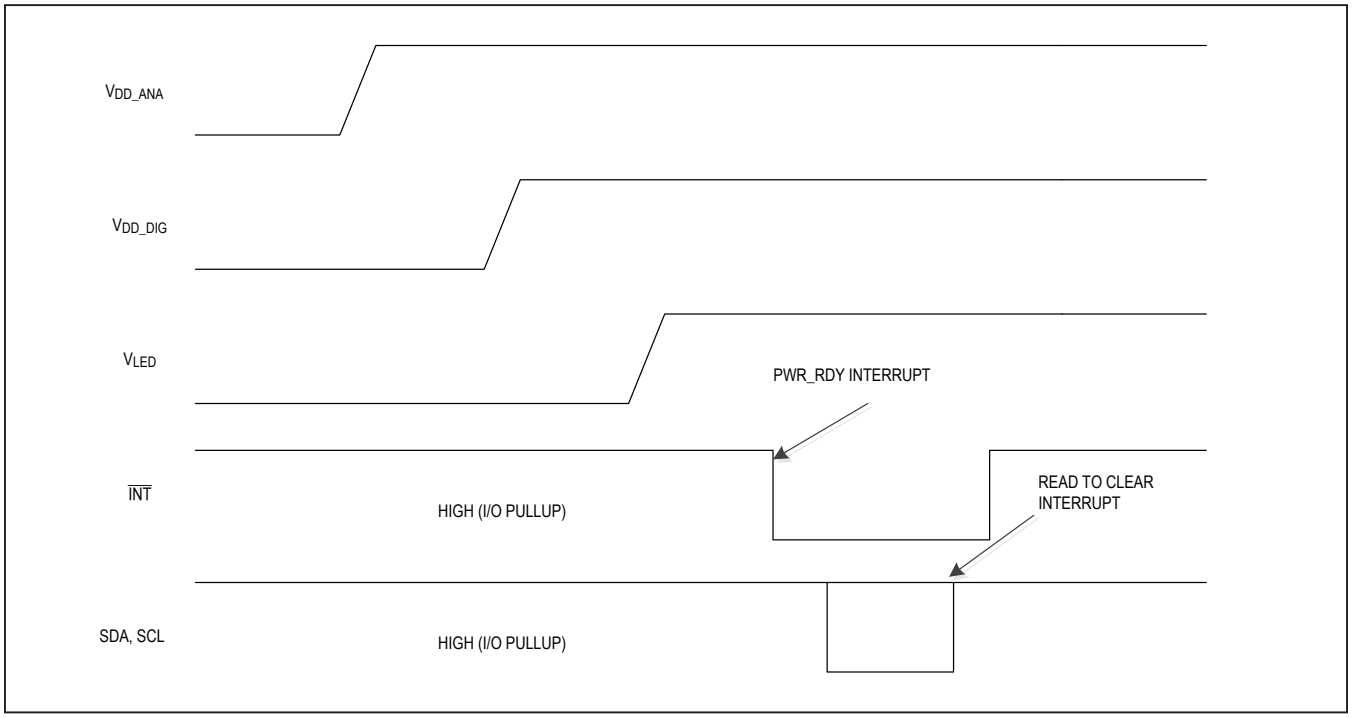


Figure 3. Power-Up Sequence of the Power Supply Rails

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high . A START condition from the master signals the beginning of a transmission to the MAX86150. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition. Figure 4 shows the START, STOP, and REPEATED START of the I2C conditions

Early STOP Conditions

The MAX86150 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave ID. When idle, the MAX86150 waits for a START condition followed by its slave ID. The serial interface compares each salve ID bit by bit, allowing the interface to power down and disconnect from SCL immediately if an incorrect slave ID is detected. After recognizing a START condition followed by the correct slave ID, the MAX86150 is programmed to accept or send data. The LSB of the slave ID word is the read/write (R/W) bit. R/W indicates whether the master is writing to or reading data from the MAX86150 (R/W = 0 selects a write condition, R/W = 1 selects a read condition). After receiving the proper slave ID, the MAX86150 issues an ACK by pulling SDA low for one clock cycle.

The MAX86150 slave ID consists of seven fixed bits, B7–B1 (set to 0b1011110). The most significant slave ID bit (B7) is transmitted first, followed by the remaining bits.

B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS	READ ADDRESS
1	0	1	1	1	1	0	RW	0xBC	0xBD

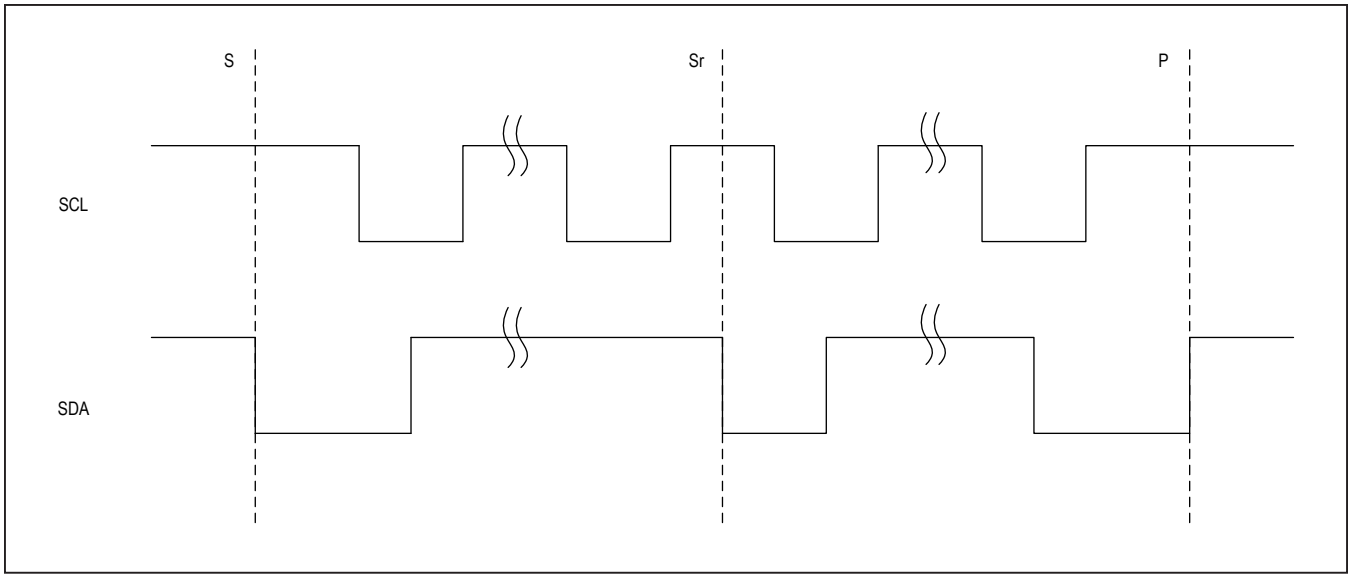


Figure 4. START, STOP, and REPEATED START Conditions

Acknowledge

The acknowledge bit (ACK) as shown in Figure 5 is a clocked 9th bit that the MAX86150 uses to handshake receipt each byte of data when in write mode. The MAX86150 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX86150 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX86150, followed by a STOP condition.

Write Data Format

For the write operation, send the slave ID as the first byte followed by the register address byte and then one or more data bytes. The register address pointer increments automatically after each byte of data received, so for example the entire register bank can be written by at one time. Terminate the data transfer with a STOP condition. The write operation is shown in the Figure 6.

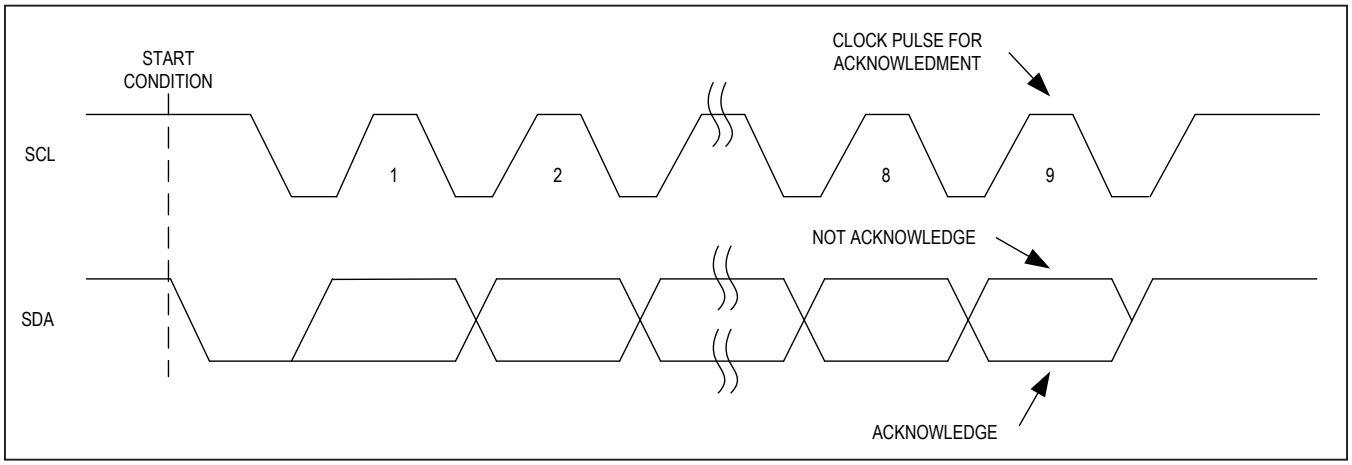


Figure 5. I²C Acknowledge

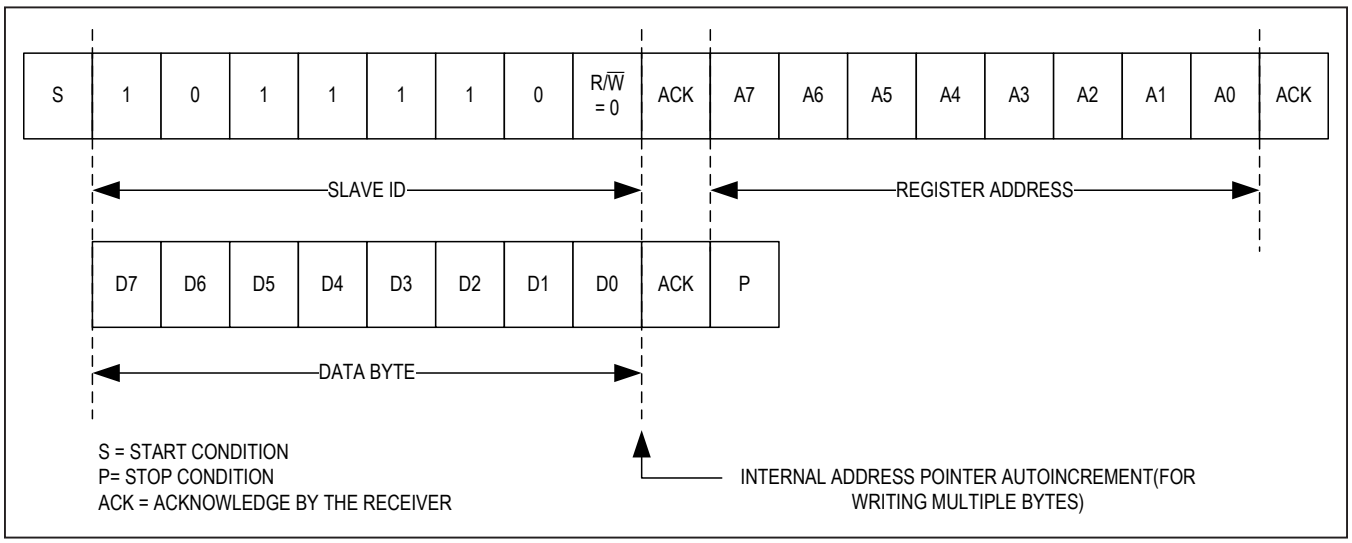


Figure 6. Writing One Data Byte to MAX86150

Read Data Format

For the read operation, two I2C operations must be performed. First, the slave ID byte is sent followed by the I2C register that you wish to read. Then a REPEAT START (Sr) condition is sent, followed by the read slave ID. The MAX86150 then begins sending data beginning with the register selected in the first operation. The read pointer increments automatically, so the MAX86150 continues sending data from additional registers in sequential order until a STOP (P) condition is received. The exception to this is the FIFO_DATA register, at which the read pointer no longer increments when reading additional bytes. To read the next register after FIFO_DATA, an I2C write command is necessary to change the location of the read pointer.

Figure 7 and Figure 8 show the process of reading one byte or multiple bytes of data respectively.

An initial write operation is required to send the read register address.

Data is sent from registers in sequential order, starting from the register selected in the initial I2C write operation. If the FIFO_DATA register is read, the read pointer does not automatically increment, and subsequent bytes of data contain the contents of the FIFO.

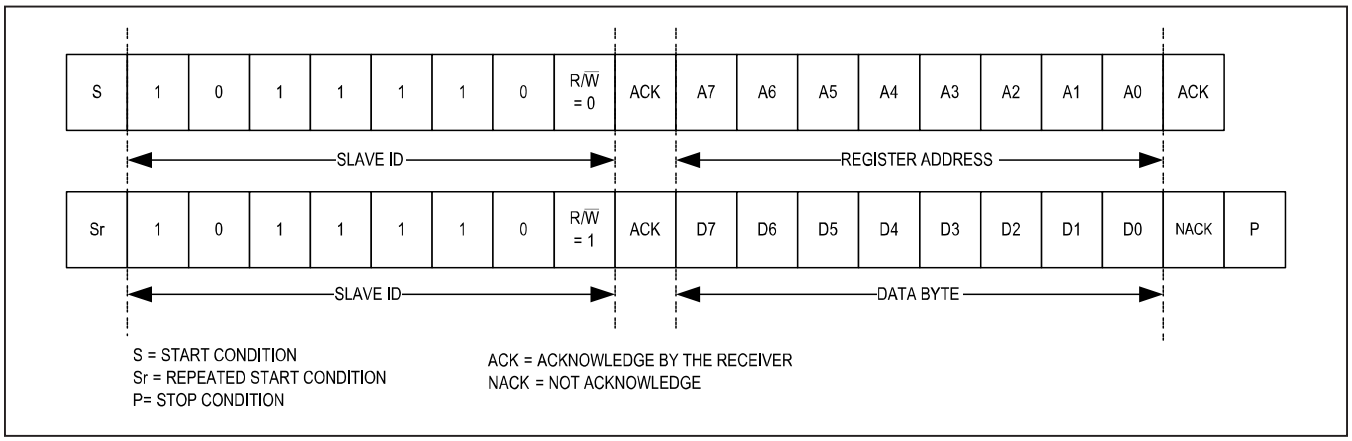


Figure 7. Reading One Byte of Data from MAX86150

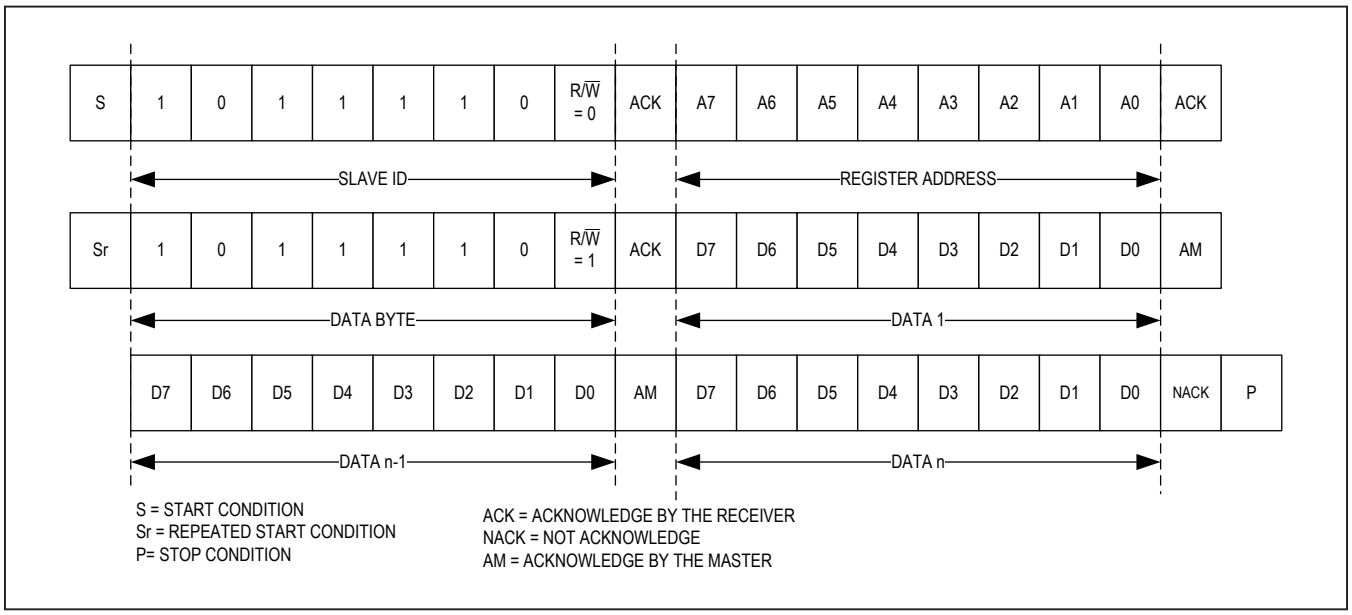


Figure 8. Reading Multiple Bytes of Data from the MAX86150

FIFO Description

Overview

The FLEX FIFO is designed to support configurable number of elements. So the number of elements in each sample is configurable. All elements are of same width, but can be interpreted differently, depending on how the FIFO data is configured. MS bits of any element that is smaller than this width is padded with zeroes. Reading FIFO through the I^2C returns only the active FIFO data corresponding to the current configuration.

The design is also scalable to support any:

- Element width in number of bits
- Sample length in number of elements
- FIFO depth in number of samples

Each sample comprises of up to four elements. The actual number of elements in a sample depends on:

- FIFO Data Control Register 1
- FIFO Data Control Register 2

FIFO Data Types

FIFO Data Control Registers

Table 1 shows the FIFO Data Control registers that are used for enabling any of the PPG modes (e.g., HR, SpO_2, etc), ECG mode.

FD1, FD2, FD3, and FD4 (FDx[3:0]) are configured as shown in the Table 2 to hold data as programmed. It also shows the format of the data in the FIFO.

Table 1. FIFO Data Control registers

ADDRESS	REGISTER NAME	HARDWIRED VALUE	B7	B6	B5	B4	B3	B2	B1	B0
0x09	FIFO Data Configuration Register 1	00	FD2[3:0]				FD1[3:0]			
0x0A	FIFO Data Configuration Register 2	00	FD4[3:0]				FDS3[3:0]			

Table 2. FDx Format Configurations

FDX[3:0]	DATA TYPE	FIFO CONTENT OR DATA DESCRIPTION	NOTE
0000	None	N/A	
0001	PPG	PPG_DATA[18:0] for LED1 (IR)	MS bits should be masked
0010	PPG	PPG_DATA[18:0] for LED2 (Red)	MS bits should be masked
0011	Reserved	Reserved	
0100	Reserved	Reserved	
0101	PPG	PPG_DATA[18:0] for Pilot LED1 (IR)	MS bits should be masked
0110	PPG	PPG_DATA[18:0] for Pilot LED2 (Red)	MS bits should be masked
0111	Reserved	Reserved	
1000	Reserved	Reserved	
1001	ECG	ECG_DATA[17:0]	MS bits padded with zeroes
1010	Reserved	Reserved	
1011	Reserved	Reserved	
1100	Reserved	Reserved	
1101	Reserved	Reserved	
1110	Reserved	Reserved	
1111	Reserved	Reserved	

If a configuration uses only one element, FD2, FD3, and FD4 are programmed as zeroes, and FD1 is programmed to the required data type.

- If a configuration uses only two elements, FD3 and FD4 are programmed as zeroes, and FD1 and FD2 are programmed to the required data types.
- If a configuration uses only three elements, FD4 is programmed as zeroes, and FD1, FD2, and FD3 are programmed to the required data types.
- If a configuration uses all four elements, FD1, FD2, FD3, and FD4 are programmed to the required data types.

PPG data is left justified as shown in Table 3. In other words, the MSB bit is always in the bit 18 position regardless of ADC resolution setting, and the LSBs are padded with '0'. FIFO_DATA[23:19] are don't care and should be masked.

ECG Data is right justified, FIFO_DATA[23:18]are always padded with '0'.

Table 3. FIFO Data Format

	FIFO_DATA																							
	BYTE 1								BYTE 2								BYTE 3							
ADC Resolution	FIFO_DATA[23]	FIFO_DATA[22]	FIFO_DATA[21]	FIFO_DATA[20]	FIFO_DATA[19]	FIFO_DATA[18]	FIFO_DATA[17]	FIFO_DATA[16]	FIFO_DATA[15]	FIFO_DATA[14]	FIFO_DATA[13]	FIFO_DATA[12]	FIFO_DATA[11]	FIFO_DATA[10]	FIFO_DATA[9]	FIFO_DATA[8]	FIFO_DATA[7]	FIFO_DATA[6]	FIFO_DATA[5]	FIFO_DATA[4]	FIFO_DATA[3]	FIFO_DATA[2]	FIFO_DATA[1]	FIFO_DATA[0]
PPG (19-bit)	x	x	x	x	x																			
ECG (18-bit)	0	0	0	0	0	0																		

PPG elements are stored first, followed by ECG, as shown in the examples below:

Example 1: Configurations for 3 elements: PPG (LED 1) + PPG (LED2) + ECG

FD1[3:0]	FD2[3:0]	FD3[3:0]	FD4[3:0]
0001 (PPG)	0010 (PPG)	1001 (ECG)	0000 (None)

Example 2: Configurations for 2 elements: PPG (LED 2) + ECG

FD1[3:0]	FD2[3:0]	FD3[3:0]	FD4[3:0]
0010 (PPG)	1001 (ECG)	0000 (None)	0000 (None)

Example 3: Configurations for 2 elements: PPG (LED 1) + PPG (LED2)

FD1[3:0]	FD2[3:0]	FD3[3:0]	FD4[3:0]
0001 (PPG)	0010 (PPG)	0000 (None)	0000 (None)

Example 4: Configurations for 1 element: ECG

FD1[3:0]	FD2[3:0]	FD3[3:0]	FD4[3:0]
1001 (ECG)	0000 (None)	0000 (None)	0000 (None)

Example 5: Configurations for 1 element: PPG (LED 1)

FD1[3:0]	FD2[3:0]	FD3[3:0]	FD4[3:0]
0001 (PPG)	0000 (None)	0000 (None)	0000 (None)

Table 4. Sample of FIFO Data Index

INDEX WITHIN A SAMPLE	FIFO_DATA[23:0]
0	FD1 data, if enabled
1	FD2 data, if enabled
2	FD3 data, if enabled
3	FD4 data, if enabled

A sample in the FIFO is shown in Table 4.

FIFO Handling

Only the elements corresponding to the active FIFO data are pushed onto the FIFO, and only these are read through the I2C. The unused FIFO data are not read through the I2C, so they are don't care and not padded with zeroes.

The FIFO handling registers are shown in Table 5.

Write Pointer to the FIFO, FIFO_WR_PTR[4:0]:

This points to the location where the next sample will be written. This pointer advances for each sample pushed on to the FIFO.

Read Pointer to the FIFO, FIFO_RD_PTR[4:0]:

This points to the location from where the AP gets the next sample from the FIFO through the I2C interface. This advances each time a sample is popped from the FIFO. The AP can also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO.

FIFO Data Read, FIFO_DATA[7:0]:

This is a read-only register and is used to get data from the FIFO. Reading FIFO_DATA register does not automatically increment the register address. So burst reading this register, reads the same address over and over. The length of a sample is determined by the number of active elements in the sample. Each element is three bytes long. In order to read one complete sample the FIFO_DATA register has to be read N times, where

N = (Number of active elements) * (Number of bytes, 3)

Reading from the FIFO

Normally, reading registers from the I2C interface autoincrements the register address pointer, so that all the registers can be read in a burst read without an I2C restart event. In this case, this holds true for all registers except for the FIFO_DATA register (register 0x07).

Reading the FIFO_DATA register does not automatically increment the register address. Burst reading this register reads data from the same address over and over. Each sample comprises multiple bytes of data, so multiple bytes should be read from this register (in the same transaction) to get one full sample.

FIFO_RD_PTR advances only after burst reading the entire sample.

Table 5. FIFO Handling Registers

ADDRESS	REGISTER NAME	HARDWIRED VALUE	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FIFO Write Pointer	00				FIFO_WR_PTR[4:0]				
0x05	Overflow Counter	00				OVF_COUNTER[4:0]				
0x06	FIFO Read Pointer	00				FIFO_RD_PTR[4:0]				
0x07	FIFO Data Register	00	FIFO_DATA[7:0]							
0x08	FIFO Configuration	00		A_FULL_CLR	A_FULL_TYPE	FIFO_ROLLS_ON_FULL	FIFO_A_FULL[3:0]			

Each sample is read from the FIFO in the following order, when all **four** Elements are active (Table 6).

Table 6. FIFO Sample Elements Order with four active elements

			FIFO_RD_PTR[4:0]
n Sample:	1st read	Element 1[23:16]	n
	2nd read	Element 1[15:8]	n
	3rd read	Element 1[7:0]	n
	4th read	Element 2[23:16]	n
	5th read	Element 2[15:8]	n
	6th read	Element 2[7:0]	n
	7th read	Element 3[23:16]	n
	8th read	Element 3[15:8]	n
	9th read	Element 3[7:0]	n
	10th read	Element 4[23:16]	n
	11th read	Element 4[15:8]	n
	12th read	Element 4[7:0]	n
n+1 Sample:	13th read	Element 1[23:16]	n+1
	14th read	Element 1[15:8]	n+1
	15th read	Element 1[7:0]	n+1
	16th read	Element 2[23:16]	n+1
	17th read	Element 2[15:8]	n+1
	18th read	Element 2[7:0]	n+1
	19th read	Element 3[23:16]	n+1
	20th read	Element 3[15:8]	n+1
	21st read	Element 3[7:0]	n+1
	22nd read	Element 4[23:16]	n+1
	23rd read	Element 4[15:8]	n+1
	24th read	Element 4[7:0]	n+1
. . . .	. . . .	. . . .	. . . .

Each sample is read from the FIFO in the following order, when any **two** Elements are active (Table 7).

Table 7. FIFO Sample Elements Order with two active elements

			FIFO_RD_PTR[4:0]
n Sample:	1st read	Element 1[23:16]	n
	2nd read	Element 1[15:8]	n
	3rd read	Element 1[7:0]	n
	4th read	Element 2[23:16]	n
	5th read	Element 2[15:8]	n
	6th read	Element 2[7:0]	n
n+1 Sample:	7th read	Element 1[23:16]	n+1
	8th read	Element 1[15:8]	n+1
	9th read	Element 1[7:0]	n+1
	10th read	Element 2[23:16]	n+1
	11th read	Element 2[15:8]	n+1
	12th read	Element 2[7:0]	n+1
. . . .	. . . .	. . . .	. . . .

Enable Push on FIFO FULL, FIFO_ROLLS_ON_FULL: This bit determines whether samples get pushed on to the FIFO when it is full. If push is enabled when FIFO is full, old samples are lost. Otherwise, new samples are lost.

Overflow counter, OVF_COUNTER[4:0]: When the FIFO is full, samples are lost. OVF_COUNTER counts the number of samples lost. It saturates at 0x1F. When a complete sample is popped from the FIFO (when the read pointer advances), and OVF_COUNTER is reset to zero.

FIFO Almost Full Counter, FIFO_AFULL_COUNT[3:0]: This determines the amount of space available in the FIFO, to declare that it is almost full.

FIFO Almost Full status, and Interrupt Enable, A_FULL and MSK_A_FULL: When the FIFO is almost full, the almost full interrupt is asserted if it is enabled by the MSK_A_FULL bit. This prompts the AP to read some samples before the FIFO gets full. A_FULL bit is cleared when the status register is read.

The AP reads the FIFO_WR_PTR and FIFO_RD_PTR to calculate the number of samples available in the FIFO, and read as many samples as it needs up to a maximum of available samples. The AP can then choose to write the new read pointer to the FIFO_RD_PTR register. If necessary to retry, the AP updates the FIF_RD_PTR register with appropriate value.

Example: Following is an example of the pseudo code:

First transaction: Get the FIFO_WR_PTR and FIFO_RD_PTR:

START;
Send device address + write mode
Send address of FIFO_WR_PTR;
REPEATED_START;
Send device address + read mode
Read FIFO_WR_PTR;
Read OVF_COUNTER;
Read FIFO_RD_PTR;
STOP;

AP evaluates the number of samples to be read from the FIFO:

If OVF_COUNTER is zero,
NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR – FIFO_RD_PTR
(Note: pointer wrap around should be taken into account)
If OVF_COUNTER is non-zero some samples are lost, and
NUM_AVAILABLE_SAMPLES = 32
NUM_SAMPLES_TO_READ = < less than or equal to NUM_AVAILABLE_SAMPLES >

Next transaction: Read NUM_SAMPLES_TO_READ samples from the FIFO:

```
START;
Send device address + write mode
Send address of FIFO_DATA;
REPEATED_START;
Send device address + read mode
for (i = 0; i < NUM_SAMPLES_TO_READ; i++) {
Read FIFO_DATA;
Save Data_Item1[23:16];
Read FIFO_DATA;
Save Data_Item1[15:8];
Read FIFO_DATA;
Save Data_Item1[7:0];
Read FIFO_DATA;
Save Data_Item2[23:16];
Read FIFO_DATA;
Save Data_Item2[15:8];
Read FIFO_DATA;
Save Data_Item2[7:0];
Read FIFO_DATA;
Save Data_Item3[23:16];
Read FIFO_DATA;
Save Data_Item3[15:8];
Read FIFO_DATA;
Save Data_Item3[7:0];
    }
STOP;
```

Next transaction: Write to FIFO_RD_PTR register. If the pervious transaction was successful, FIFO_RD_PTR points to the next sample in the FIFO, and this transaction is not necessary. Otherwise, the AP updates the FIFO_RD_PTR appropriately to New_FIFO_RD_PTR, so that the samples are reread.

```
START;
Send device address + write mode
Send address of FIFO_RD_PTR;
Write New_FIFO_RD_PTR;
STOP;
```

FIFO Flush

The FIFO gets flushed if FIFO_EN = 1, and if any of the following conditions are met:

- I2C write to any of the PPG Configuration registers
- I2C write to any of the ECG Configuration registers
- I2C write to any of the FIFO Data Control registers
- At the rising edge of FIFO_EN
- Enter and exit PROX mode

When the FIFO gets flushed, FIFO_WR_PTR and FIFO_RD_PTR are reset to zero, and the contents of the FIFO are lost.

If FIFO contents should not be lost, set FIFO_EN = 0, before writing to any of the registers listed above.

Note: FIFO_EN bit is in the System Control register. Data is pushed to the FIFO, when FIFO_EN = 1. When FIFO_EN = 0, push to FIFO is disabled, but it holds the status of the FIFO (FIFO pointers and the actual data).

FIFO Organization

Figure 9 shows how the samples are organized in the FIFO when all four elements in a sample are active.

Figure 10 shows how the samples are organized in the FIFO when only two elements in a sample are active.

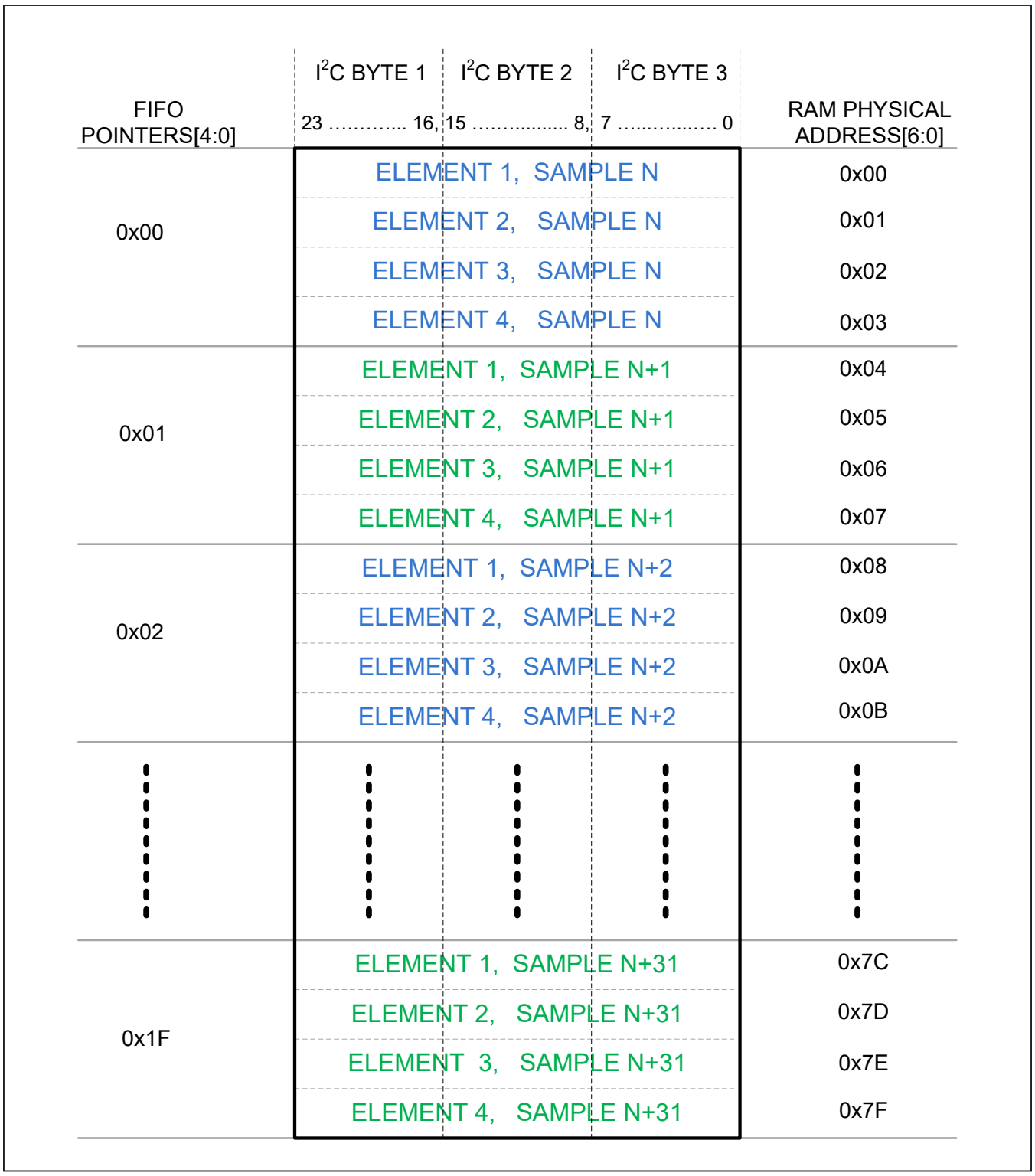


Figure 9. Example of FIFO Organization with Four Active Elements

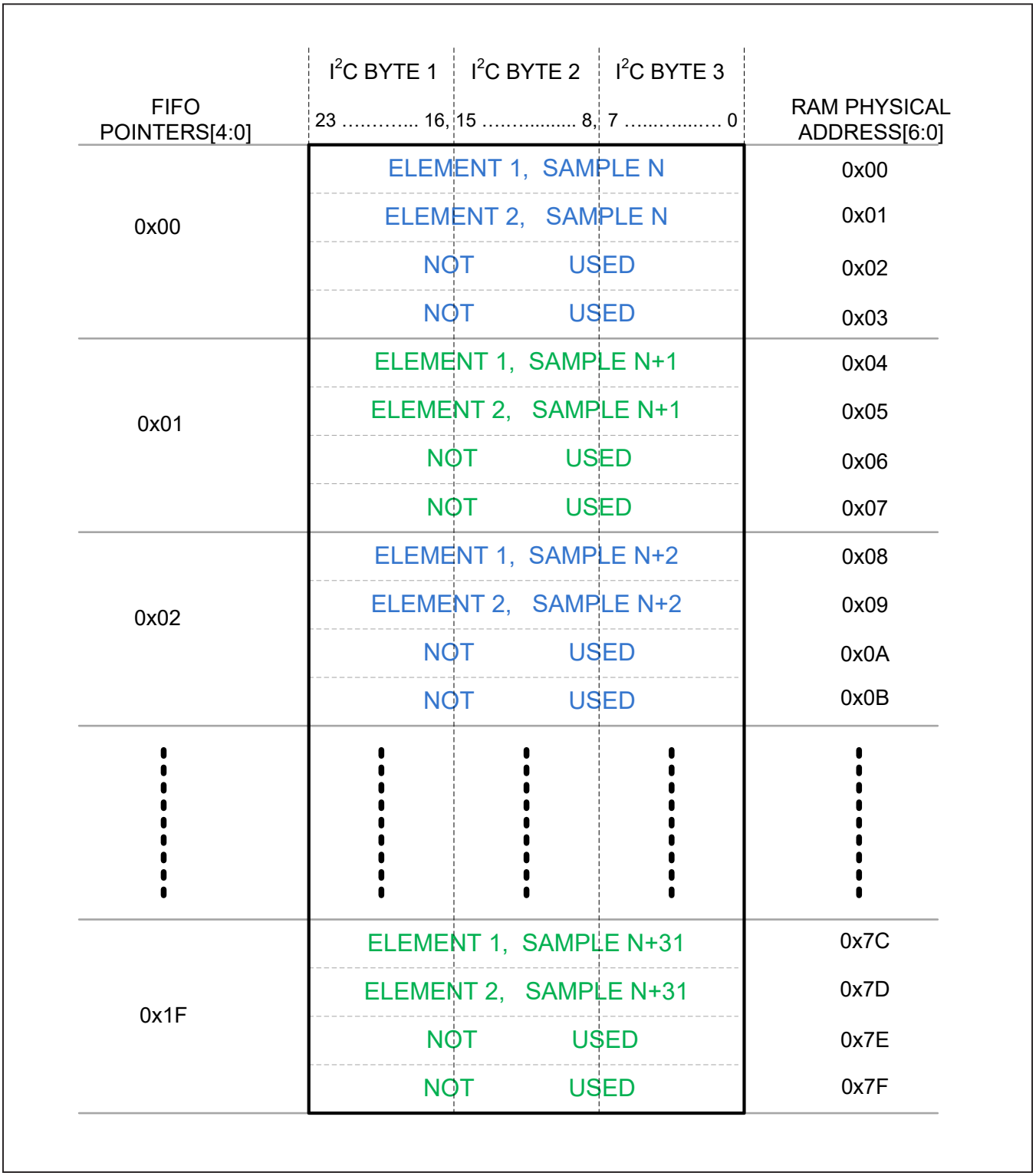
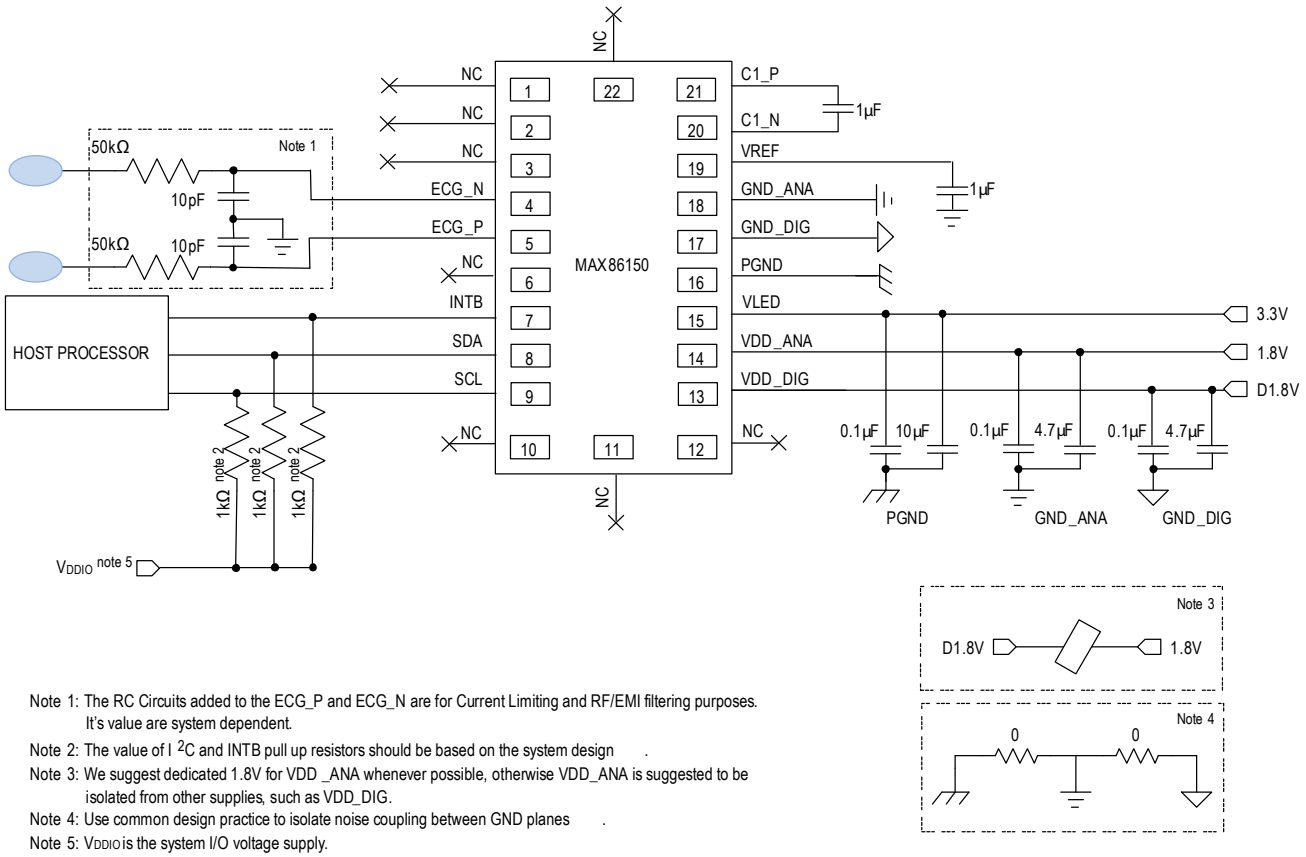


Figure 10. Example of FIFO Organization with Two Active Elements

Typical Application Circuit



Note 1: The RC Circuits added to the ECG_P and ECG_N are for Current Limiting and RF/EMI filtering purposes. It's value are system dependent.

Note 2: The value of I ^{2}C and INTB pull up resistors should be based on the system design .

Note 3: We suggest dedicated 1.8V for VDD _ANA whenever possible, otherwise VDD_ANA is suggested to be isolated from other supplies, such as VDD_DIG.

Note 4: Use common design practice to isolate noise coupling between GND planes .

Note 5: V_{DDIO} is the system I/O voltage supply.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX86150EFF+T	-40°C to +85°C	22-Lead OESIP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/15	Initial release	—
1	11/16	General updates and typo corrections	1–47
2	12/18	Updated the *General Description, Benefits and Features, Absolute Maximum Ratings, Package Information, Electrical Characteristics, Pin Description, Detailed Description, LED Driver,* and *Electrocardiogram (ECG)* sections; updated the *Register Map* and *Interrupt Enable 1 (0x02), FIFO Data Control Register 1 (0x09), PPG Configuration (0x0E), Prox Interrupt threshold (0x10), LED Pilot PA (0x15),* and *ECG Configuration (0x3C)* register tables; replaced all *Typical Operating Characteristics*; added *ECG and PPG Synchronization* section	1–13, 15–20 22, 27, 30, 31 32, 34–35

