19-2281; Rev 4; 11/08

2.7Gbps Laser Driver with Modulation Compensation

MAX3863

General Description

The MAX3863 is designed for direct modulation of laser diodes at data rates up to 2.7Gbps. An automatic power-control (APC) loop is incorporated to maintain a constant average optical power. Modulation compensation is available to increase the modulation current in proportion to the bias current. The optical extinction ratio is then maintained over temperature and lifetime.

The laser driver can modulate laser diodes at amplitudes up to 80mA. Typical (20% to 80%) edge speeds are 50ps. The MAX3863 can supply a bias current up to 100mA. External resistors can set the laser output levels.

The MAX3863 includes adjustable pulse-width control to minimize laser pulse-width distortion. The device offers a failure monitor output to indicate when the APC loop is unable to maintain the average optical power.

The MAX3863 accepts differential CML clock and data input signals with on-chip 50Ω termination resistors. If a clock signal is available, an input data-retiming latch can be used to reject input pattern-dependent jitter. The laser driver is fabricated with Maxim's in-house second-generation SiGe process.

Applications

SONET and SDH Transmission Systems

WDM Transmission Systems

3.2Gbps Data Communications

Add/Drop Multiplexers

Digital Cross-Connects

Section Regenerators

Long-Reach Optical Transmitters

Features

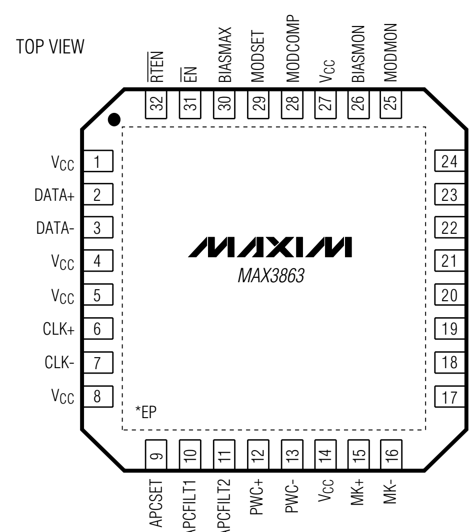
- ♦ Single +3.3V Power Supply
- ♦ 58mA Power-Supply Current
- ♦ Up to 2.7Gbps (NRZ) Operation
- ♦ On-Chip Termination Resistors
- ♦ Automatic Power Control (APC)
- ♦ Compensation for Constant Extinction Ratio
- ♦ Programmable Modulation Current Up to 80mA
- ♦ Programmable Bias Current Up to 100mA
- ♦ 50ps Typical Rise/Fall Time
- ♦ Pulse-Width Adjustment Circuit
- ♦ Selectable Data-Retiming Latch
- ♦ Failure Detector
- ♦ Mark-Density Monitor
- ♦ Current Monitors
- ♦ ESD Protection

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3863ETJ+	-40°C to +85°C	32 TQFN-EP*
MAX3863EGJ	-40°C to +85°C	32 QFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



TQFN-EP
QFN-EP

*THE EXPOSED PAD MUST BE SOLDERED TO GND ON THE CIRCUIT BOARD.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2.7Gbps Laser Driver with Modulation Compensation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}..-0.5V to +5.0V
DATA+, DATA- and CLK+, CLK- ....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
$\overline{RTEN}$, $\overline{EN}$, BIAS, MK+, MK-, PWC+, PWC-
MODMON, BIASMON, MDMON, MODCOMP,
APCFILT1, APCFILT2, BIASMAX, MODSET,
APCSET Voltage ....-0.5V to (V_{CC} + 0.5V)
MOD, MODN Voltage ....0 to (V_{CC} + 1.5V)
MOD, MODN Current.....................................-20mA to +150mA
BIAS Current ....-20mA to +150mA
MD Current...-5mA to +5mA
Operating Junction Temperature Range...........-55°C to +150°C
Storage Temperature Range ....-55°C to +150°C
Continuous Power Dissipation (T_A = +85°C)
32-Pin QFN, TQFN (derate 21.2mW/°C above +85°C)....1.3W
Processing Temperature (die) ....+400°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.15V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 50mA, I_{MOD} = 40mA, T_A = +25°C, unless otherwise noted.) (Notes 1, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current	I_{CC}	(Note 2)		58	85	mA
Power-Supply Noise Rejection	PSNR	f = 100kHz, 100mV_{P-P} (Note 10)		40		dB
Power-Supply Threshold		Output enabled		2.8		V
Single-Ended Input Resistance		Input to V_{CC}	40	50	60	Ω
Bias-Current Setting Range			4		100	mA
Bias-Current Setting Error		APC open loop, I_{BIAS} = 100mA, T_A = +25°C	-15		+15	%
		APC open loop, I_{BIAS} = 4mA, T_A = +25°C	-20		+20	
Bias Off-Current		$\overline{EN}$ high			0.1	mA
I_{BIAS} to $I_{BIASMON}$ Ratio			34	40	46	mA/mA
Bias-Current Temperature Stability		APC open loop, 10mA ≤ I_{BIAS} ≤ 100mA (Note 3)	-480		+480	ppm/°C
		APC open loop, 4mA ≤ I_{BIAS} ≤ 100mA (Note 3)		±390		
Modulation-Current Setting Range			7		80	mA
Modulation-Current Setting Error		APC open loop, 25Ω load, T_A = +25°C	-15		+15	%
Modulation Off-Current		$\overline{EN}$ high			0.1	mA
Modulation-Current Temperature Stability		APC open loop (Note 3)	-480		+480	ppm/°C
I_{MOD} to I_{MODMON} Ratio			38	46	53	mA/mA
Modulation Compensation Range	K	K = $\Delta I_{MODC}/\Delta I_{BIAS}$	0		1.5	mA/mA
MD Pin Voltage					1.75	V
Monitor Photodiode Current Range	I_{MD}		30		2000	µA
APC Loop Time Constant	t_{APC}	(Notes 3, 4)	1	4	1000	µs
APC Open Loop		4mA ≤ I_{BIAS} ≤ 10mA (Note 3)		±390		mA
V_{MDMON} to I_{MD} Ratio		R_{MDMON} = 4kΩ	0.8	1.0	1.2	mV/µA
$\overline{EN}$ and $\overline{RTEN}$ Input High	V_{IH}		2.0			V
$\overline{EN}$ and $\overline{RTEN}$ Input Low	V_{IL}				0.8	V
$\overline{FAIL}$ Output High	V_{OH}	Source 150µA	2.4			V
$\overline{FAIL}$ Output Low	V_{OL}	Sink 2mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.15V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 50mA, I_{MOD} = 40mA, T_A = +25°C, unless otherwise noted.) (Notes 1, 9)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Single-Ended Input (DC-Coupled)	V_{IS}	At high			V_{CC}		V
		At low		V_{CC} - 1.0		V_{CC} - 0.1	
Single-Ended Input (AC-Coupled)	V_{IS}	At high		V_{CC} + 0.05		V_{CC} + 0.4	V
		At low		V_{CC} - 0.4		V_{CC} - 0.05	
Differential Input Swing	V_{ID}	DC-coupled		0.2		2.0	V_{P-P}
		AC-coupled		0.2		1.6	
Input Data Rate		NRZ (Note 3)			3.2		Gbps
Input Return Loss	RL_{IN}	(Notes 3, 5)	f ≤ 2.7GHz		17		dB
			2.7GHz < f ≤ 4GHz		14		
Turn-Off Delay from $\overline{EN}$		$\overline{EN}$ = high (Note 3)				1.0	µs
Setup Time	t_{SU}	Figure 2 (Note 3)		90			ps
Hold Time	t_{HD}	Figure 2 (Note 3)		90			ps
Pulse-Width Adjustment Range		Z_L = 25Ω (Notes 3, 6)		±185	±220		ps
Pulse-Width Stability		PWC+ and PWC- open (Notes 3, 6)				±18.5	ps
Differential Pulse-Width Control Input Range		For PWC+ and PWC- (Notes 3, 7), V_{CM} = 0.5V		-1.0		1.0	V
Differential Mark Density		0% to 100%, V_{MK+} - V_{MK-}				±0.85	V
Differential Mark-Density Voltage to Mark-Density Ratio					15.5		V/%
Output Edge Speed	t_R, t_F	Z_L = 25Ω (20% to 80%) (Notes 3, 6)			50	85	ps
Output Overshoot	δ	Z_L = 25Ω (Note 3)			±7		%
Random Jitter		(Notes 3, 6)			0.8	1.3	ps_{RMS}
Deterministic Jitter		Data Rate = 2.7Gbps (Notes 3, 8)			8	40	ps_{P-P}
		Data Rate = 3.2Gbps (Notes 3, 8)			10	40	

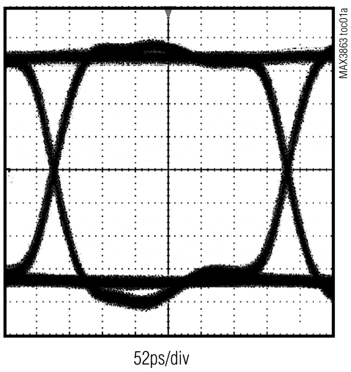
Note 1: Specifications at -40°C are guaranteed by design and characterization.
Note 2: Excluding I_{BIAS}, I_{MOD}, $I_{BIASMON}$, I_{MODMON}, $I_{\overline{FAIL}}$, and I_{PWC}. Input clock and data are AC-coupled.
Note 3: Guaranteed by design and characterization.
Note 4: An external capacitor at APCFILT1 and APCFILT2 is used to set the time constant.
Note 5: For both data inputs DATA+, DATA- and clock inputs CLK+, CLK-.
Note 6: Measured using a 2.7Gbps repeating 0000 0000 1111 1111 pattern.
Note 7: For pulse width, PW = 100%: Rp = Rn = 500Ω (or open) or PWC+ = PWC- ≈ +0.5V. For PW > 100%: Rp > Rn or PWC+ > PWC-. For PW < 100%: Rp < Rn or PWC+ < PWC-.
Note 8: Measured using a 2^{13} - 1 PRBS with 80 zeros + 80 ones input data pattern or equivalent.
Note 9: AC characterization performed using the circuit in Figure 1.
Note 10: Power-Supply Noise Rejection (PSNR) = $20\log_{10}(V_{NOISE\ (on\ VCC)}/\Delta V_{OUT})$. V_{OUT} is the voltage across the 25Ω load when no input is applied.

2.7Gbps Laser Driver with Modulation Compensation

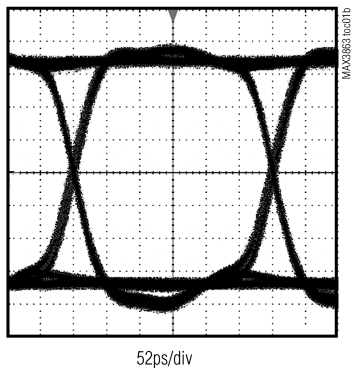
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted. See *Typical Operating Circuit.*)

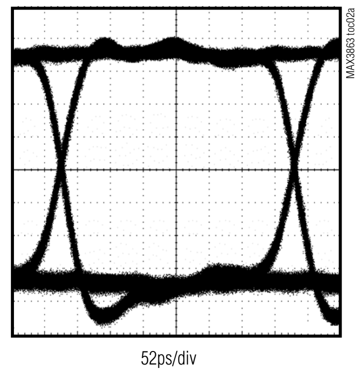
ELECTRICAL EYE DIAGRAM (I_{MOD} = 80mA, DATA RATE = 2.7Gbps, PATTERN 2^{13} - 1 + 80CID)



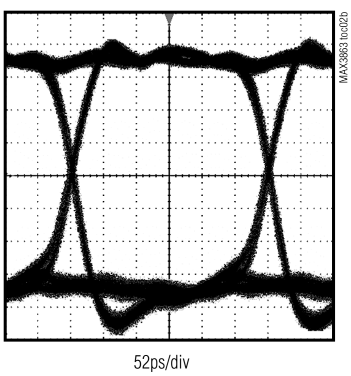
ELECTRICAL EYE DIAGRAM (I_{MOD} = 80mA, DATA RATE = 3.2Gbps, PATTERN 2^{13} - 1 + 80CID)



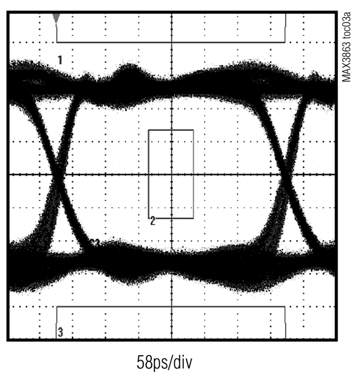
ELECTRICAL EYE DIAGRAM (I_{MOD} = 7mA, DATA RATE = 2.7Gbps, PATTERN 2^{13} - 1 + 80CID)



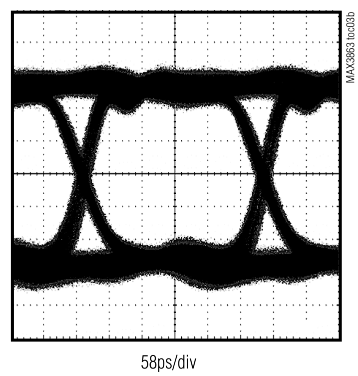
ELECTRICAL EYE DIAGRAM (I_{MOD} = 7mA, DATA RATE = 3.2Gbps, PATTERN 2^{13} - 1 + 80CID)



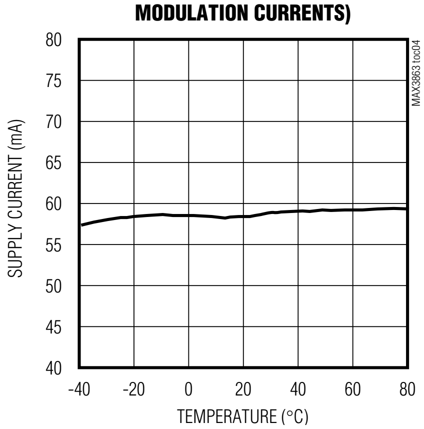
OPTICAL EYE DIAGRAM (I_{MOD} = 40mA, DATA RATE = 2.5Gbps, PATTERN 2^{13} - 1 + 80CID)



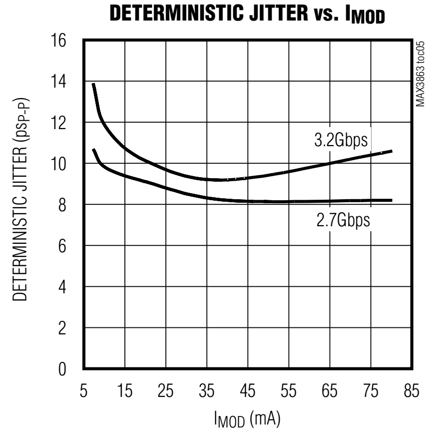
OPTICAL EYE DIAGRAM (I_{MOD} = 40mA, DATA RATE = 3.2Gbps, PATTERN 2^{13} - 1 + 80CID)



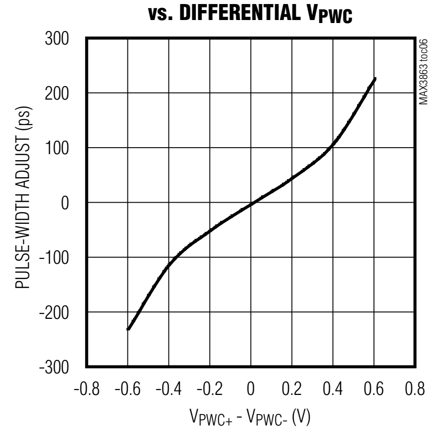
SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE (EXCLUDES BIAS AND MODULATION CURRENTS)



DETERMINISTIC JITTER vs. I_{MOD}



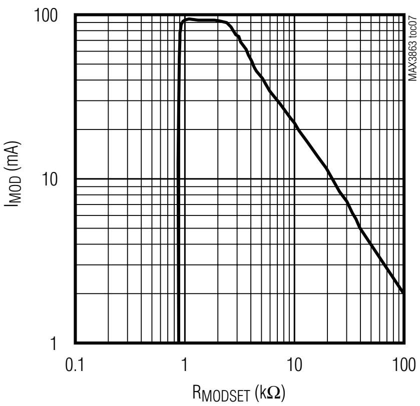
PULSE-WIDTH ADJUST vs. DIFFERENTIAL V_{PWC}



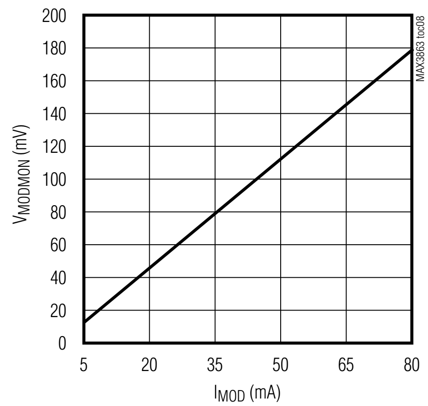
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. See *Typical Operating Circuit.*)

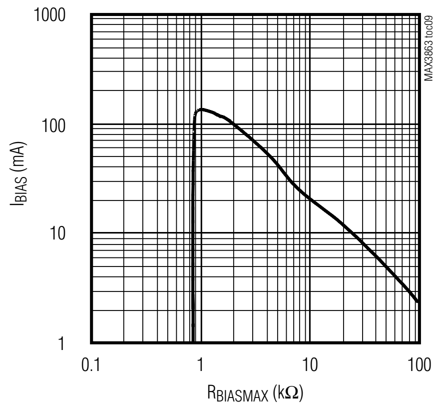
MODULATION CURRENT vs. MODULATION SET RESISTOR



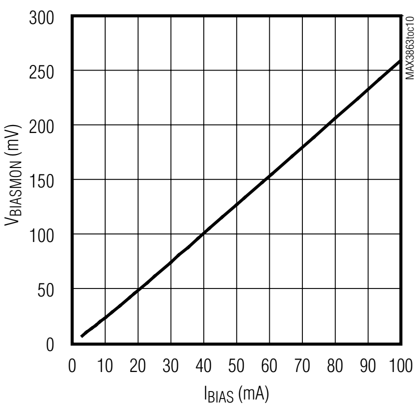
MODULATION MONITOR VOLTAGE vs. MODULATION CURRENT



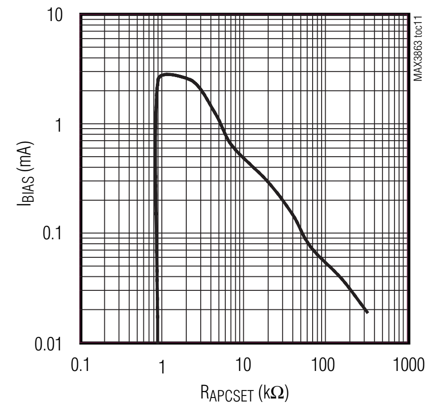
BIAS CURRENT vs. BIASMAX SET RESISTOR



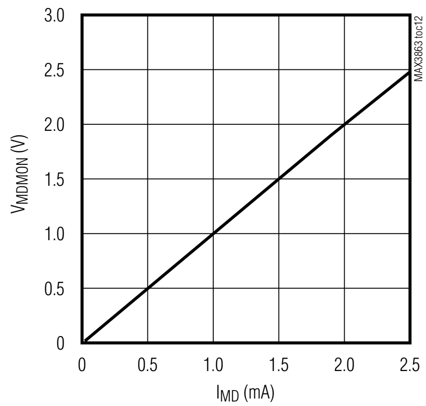
BIAS MONITOR VOLTAGE vs. BIAS CURRENT



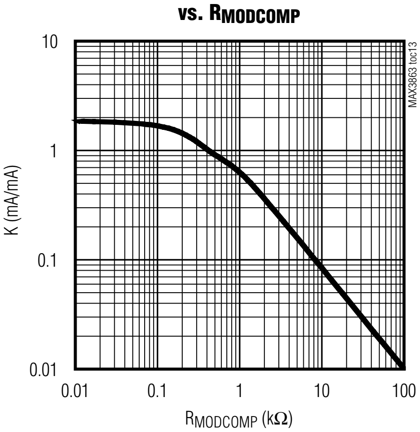
MONITOR DIODE CURRENT vs. APCSET RESISTOR



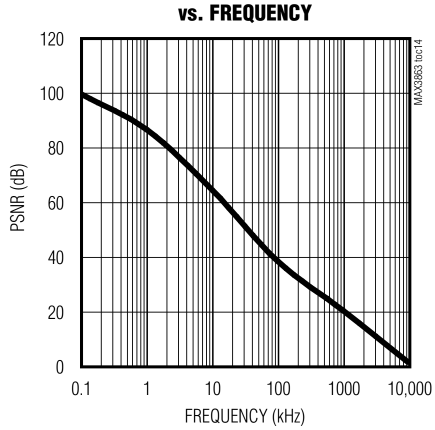
DIODE-CURRENT MONITOR VOLTAGE vs. MONITOR DIODE CURRENT



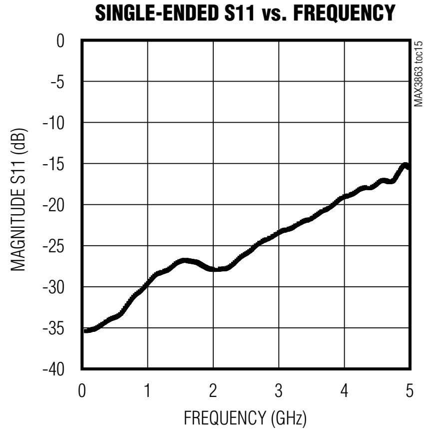
COMPENSATION (K) vs. $R_{MODCOMP}$



POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



SINGLE-ENDED S11 vs. FREQUENCY



2.7Gbps Laser Driver with Modulation Compensation

Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 8, 14, 19, 22, 27	V_{CC}	Positive Supply Voltage
2	DATA+	Data Input, with On-Chip Termination
3	DATA-	Complementary Data Input, with On-Chip Termination
6	CLK+	Clock Input for Data Retiming, with On-Chip Termination
7	CLK-	Complementary Clock Input for Data Retiming, with On-Chip Termination
9	APCSET	Monitor Diode Current Set Point
10	APCFILT1	APC Loop Filter Capacitor. Short to ground to disable the correction loop through the monitor diode.
11	APCFILT2	APC Loop Filter Capacitor
12	PWC+	Input for Modulation Pulse-Width Adjustment. Connected to GND through R_{PWC}.
13	PWC-	Complementary Input for Modulation Pulse-Width Adjustment. Connected to GND through R_{PWC}.
15	MK+	Voltage Proportional to the Mark Density. MK+ = MK- for 50% duty cycle.
16	MK-	Voltage Inversely Proportional to the Mark Density
17	$\overline{\text{FAIL}}$	Alarm for Shorts on Current Set Pins and APC Loop Failure Conditions, Active Low
18	BIAS	Laser Diode Bias Current Source (Sink Type) to Bias the Laser Diode. Connect to the laser with an inductor.
20	MOD	Driver Output. AC-coupled to the laser diode.
21	MODN	Complementary Driver Output. Connect to dummy load off-chip.
23	MD	Monitor Diode Connection
24	MDMON	Monitor for MD Current. Voltage developed across an external resistor from mirrored MD current.
25	MODMON	Monitor for Modulation Current. Voltage developed from I_{MOD} mirrored through an external resistor.
26	BIASMON	Monitor for Bias Current. Voltage developed from I_{BIAS} mirrored through an external resistor.
28	MODCOMP	Couples the Bias Current to the Modulation Current. Mirrors I_{BIAS} through an external resistor. Open for zero coupling.
29	MODSET	External Resistor to Program I_{MODC} ($I_{MOD} = I_{MODS} + I_{MODC}$)
30	BIASMAX	External Resistor to Program the Maximum I_{BIAS}
31	$\overline{\text{EN}}$	Modulation and Bias Current Enable, Active Low. Current disabled when floating or high.
32	$\overline{\text{RTEN}}$	Data Retiming Enable Input, Active Low. Retiming disabled when floating or high.
—	EP	Exposed Pad. The exposed pad must be soldered to circuit-board ground for proper thermal and electrical operation.

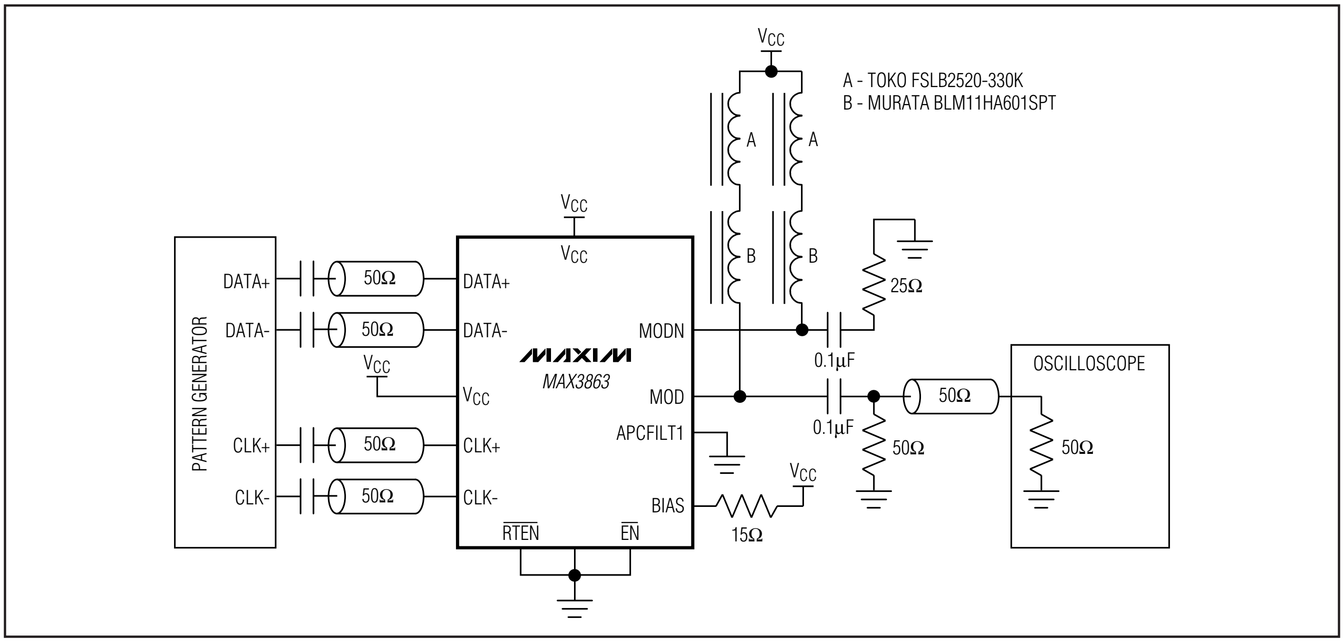


Figure 1. AC Characterization

Detailed Description

The MAX3863 laser driver has two main components: a high-speed modulation driver and a biasing block with APC. The clock and data inputs to the modulation driver use CML logic levels. The optional clock signal synchronizes data transitions for minimum pattern-dependent jitter. Outputs to the laser diode consist of a switched modulation current and a steady bias current. The APC loop adjusts the laser diode bias current to maintain constant average optical power. Compensation of the modulation current can be programmed to keep a constant extinction ratio over time and temperature. The modulation output stage uses a programmable current source with a maximum current of 80mA. A high-speed differential pair switches the source to the laser diode. The rise and fall times are typically 50ps.

Optional Input Data Retiming

To eliminate pattern-dependent jitter in the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{RTEN}$ control input should be connected low. The input data is retimed on the rising edge of CLK+. If $\overline{RTEN}$ is tied high or is left floating, the retiming function is disabled, and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

Mark-Density Outputs

The MK+ and MK- outputs monitor the input signal mark density. With a 50% mark density, both outputs are the same voltage. More ones cause the MK+ voltage to increase and the MK- voltage to decrease. Fewer ones than zeros cause MK- to be at a higher voltage than MK+.

Pulse-Width Control

A pulse-width adjustment range of 50% to 150% (±185ps) is available at 2.7Gbps. This feature compensates pulse-width distortion elsewhere in the system. Resistors at the PWC+ and PWC- pins program the pulse width. The sum of the resistors is 1kΩ. The pins can be left open for a 100% pulse width. A voltage also can control these pins. A differential voltage of 600mV (typ) gives ±185ps of pulse-width distortion.

Output Enable

The MAX3863 incorporates an input to enable current to the laser diode. When $\overline{EN}$ is low, the modulation and bias outputs at the MOD pin are enabled. When $\overline{EN}$ is high or floating, the output is disabled. In the disabled condition, bias and modulation currents are off.

Power-Supply Threshold

To prevent data errors caused by low supply, the MAX3863 disables the laser diode current for supply voltage less than 2.7V. The power-supply threshold and

2.7Gbps Laser Driver with Modulation Compensation

the output-enable must be true to enable bias and modulation currents.

APC Loop Enable

The APC loop is enabled when an external capacitor is placed between the APCFILT1 and APCFILT2 pins. This capacitor sets the time constant of the APC loop. To open the APC loop, the APCFILT1 pin is shorted to ground. This shorts the feedback from the monitor diode and causes the bias current to rise to the maximum value set by the BIASMAX pin.

APC Filter

The APC loop keeps the average optical power from the laser constant. An external filter capacitor is used to stabilize the APC loop. The typical capacitor value is 0.01µF.

APC Failure Monitor

The MAX3863 provides an APC failure monitor (TTL/CMOS) to indicate an APC loop tracking failure. $\overline{FAIL}$ is set low when the APC loop cannot adjust the bias current to maintain the desired monitor current.

Short-Circuit Protection

The MAX3863 provides short-circuit protection for modulation, bias, and monitor current sources. If BIASMAX, MODSET, or APCSET is shorted to ground, the bias and modulation output are turned off and $\overline{FAIL}$ is active.

Current Monitors

The MAX3863 features monitor outputs for bias current (BIASMON), modulation current (MODMON), and monitor diode current (MDMON). The monitors are realized by mirroring a fraction of the current and developing a voltage across an external resistor. For the specified voltage to monitor diode current, use an external 4kΩ resistor at the MDMON output. Resistors for BIASMON and MODMON are 100Ω. The minimum voltage at the BIASMON and MODMON must be 2.1V for compliance.

$$V_{BIASMON} = V_{CC} - \frac{I_{BIAS}}{40} \times 100\Omega$$

$$V_{MODMON} = V_{CC} - \frac{I_{MOD}}{45} \times 100\Omega$$

$$V_{MDMON} = \frac{I_{MD}}{4} \times 4k\Omega$$

Design Procedure

When designing a laser transmitter, the optical output is usually expressed in terms of average power and extinction ratio. Table 1 shows relationships helpful in converting between the optical average power and the modulation current. These relationships are valid only if the mark density and duty cycle of the optical waveform are 50%.

For a desired laser average optical power (P_{AVG}) and optical extinction ratio (r_e), the required modulation current can be calculated based on the laser slope efficiency (η) using the equations in Table 1.

Laser Current Compensation Requirements

Determine static bias and modulation current requirements from the laser threshold current and slope efficiency. To use the APC loop with modulation compensation,

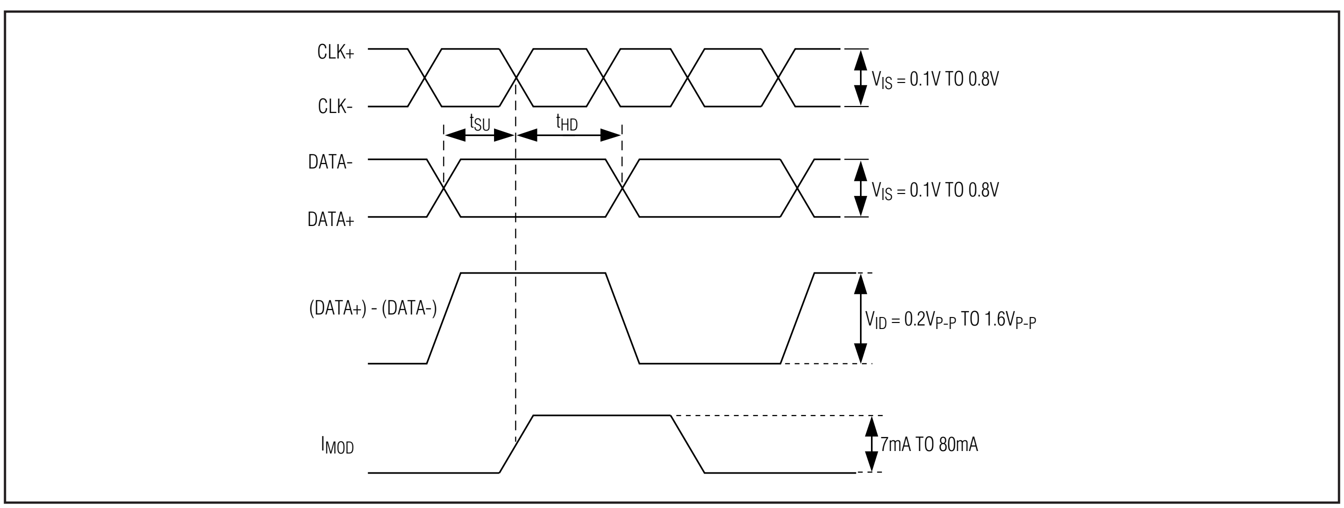


Figure 2. Required Input Signal, Setup/Hold-Time Definition and Output Polarity

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1)/2$
Extinction Ratio	r_e	$r_e = P_1/P_0$
Optical Power of a 1	P_1	$P_1 = 2P_{AVG}r_e/(r_e + 1)$
Optical Power of a Zero	P_0	$P_0 = 2P_{AVG}/(r_e + 1)$
Optical Amplitude	P_{P-P}	$P_{P-P} = P_1 - P_0$
Laser Slope Efficiency	η	$\eta = P_{P-P}/I_{MOD}$
Modulation Current	I_{MOD}	$I_{MOD} = P_{P-P}/\eta$
Threshold Current	I_{TH}	P_0 at $I \geq I_{TH}$
Bias Current	I_{BIAS}	$I_{BIAS} \geq I_{TH} + I_{MOD}/2$
Laser to Monitor Transfer	ρ_{MON}	I_{MD}/P_{AVG}

use information about the effects of temperature and aging. The laser driver automatically adjusts the bias to maintain the constant average power. The new bias condition requires proper compensation of the modulation current. The designer must predict the slope efficiency of the laser after its bias threshold current has changed. The modulation and bias currents under a single operating condition:

$$I_{MOD} = 2 \times \frac{P_{AVG}}{\eta} \times \frac{r_e - 1}{r_e + 1}$$

For AC-coupled diodes:

$$I_{BIAS} = I_{TH} + \frac{I_{MOD}}{2}$$

The required compensation factor is then:

$$K = \frac{I_{MOD2} - I_{MOD1}}{I_{BIAS2} - I_{BIAS1}}$$

Once the value of the compensation factor is known, the fixed portion of the modulation current is calculated from:

$$I_{MODS} = I_{MOD} - K \times I_{BIAS}$$

Current Limits

To allow larger modulation current, the laser is AC-coupled to the MAX3863. In this configuration, a constant current is supplied from the inductor L_P. When the MOD pin is conducting, half of I_{MOD} is supplied from L_P and half is from the laser diode. When MOD is off, the current from the inductor flows to the bias input. This reduces the current through the laser diode from the average of I_{BIAS} by half of I_{MOD}. The resulting peak-to-peak current through the laser diode is then I_{MOD}. See the *Typical Operating Circuit*. The requirement for compliance in the AC-coupled circuit:

- V_D—Diode bias point voltage (1.2V typ)
- R_L—Diode bias point resistance (5Ω typ)
- L—Diode lead inductance (1nH typ)
- R_D—Series matching resistor (20Ω typ)

$$V_{CC} - \frac{I_{MOD}}{2} \times (R_D + R_L) \geq 1.8V$$

The time constant associated with the output pullup inductor and the AC-coupling capacitor, impacts the pattern-dependent jitter. For this second-order network L_P usually limits the low-frequency cutoff. The capacitor C_D is selected so:

$$C_D \times (R_D + R_L) > \frac{L_P}{(R_D + R_L)}$$

Keep the peak voltage droop less than 3% of the peak-to-peak amplitude during the maximum CID period t. The required time constant:

$$2.8\% = 1 - e^{\frac{-t}{\tau}}$$
$$\tau = 35 \times t$$

If $\tau = L_P/25\Omega$, and t = 100UI = 40ns, then L_P = 35µH. Place a good high-frequency inductor of 2µH on the transmission line to the laser. Then you can place a low-frequency inductor of 33µH at a convenient distance from the driver output.

Programming the Bias Current

When the APC loop is enabled, the actual bias current is reduced from the maximum value to maintain constant current from the monitor diode. With closed-loop control, the bias current will be set by the transfer function of the monitor diode to laser diode current. For example, if the transfer function to the monitor diode is 10.0µA/mA, then setting I_{MD} for 500µA results in I_{BIAS} equal to 50mA. The bias current must be limited in case the APC loop becomes open. The bias current also needs a set point in case the APC control is not used. The BIASMAX pin sets the maximum bias current. The BIASMAX current is established by an internal current regulator, which maintains the bandgap voltage of 1.2V across the external

2.7Gbps Laser Driver with Modulation Compensation

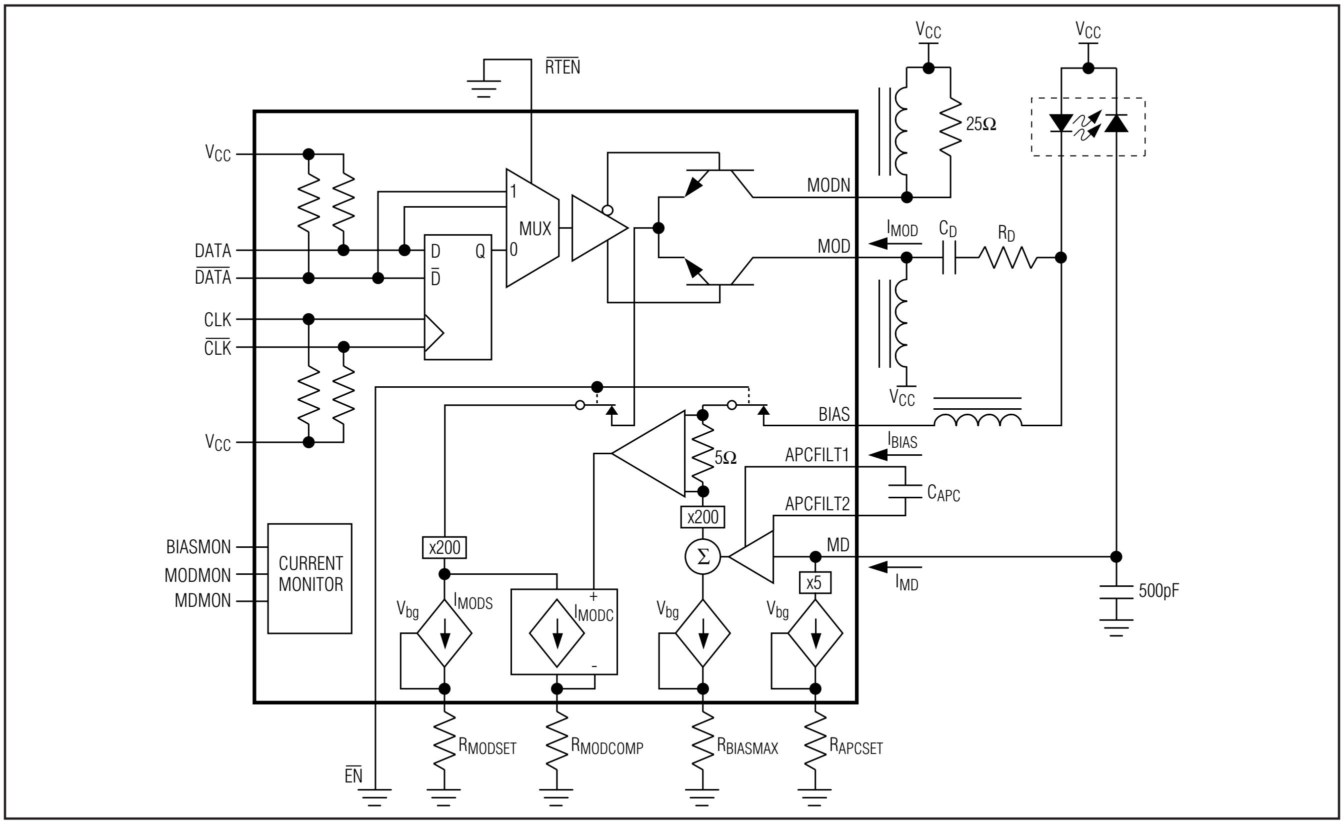


Figure 3. Functional Diagram

programming resistor. See the $I_{BIASMAX}$ vs. $R_{BIASMAX}$ graph in the *Typical Operating Characteristics*, and select the value of $R_{BIASMAX}$ that corresponds to the required current at +25°C.

$$I_{BIASMAX} = 200 \times \frac{1.2V}{R_{BIASMAX}}$$

Programming the Monitor Diode Current Set Point

The APCSET pin controls the set point for the monitor diode current. An internal current regulator establishes the APCSET current in the same manner as the BIASMAX pin. See the I_{MD} vs. R_{APCSET} graph in the *Typical Operating Characteristics*, and select the value of R_{APCSET} that corresponds to the required current at +25°C.

$$I_{MD} = 5 \times \frac{1.2V}{R_{APCSET}}$$

Programming the Modulation Current

Two current sources combine to make up the modulation current of the MAX3863 as seen in Figure 3. A constant modulation current programmed at the MODSET pin and a current, proportional to I_{BIAS}, that varies under control by the APC loop. See the *Laser Current Compensation Requirements* section for the desired values for I_{MODS} and K. The portion of I_{MOD} set by MODSET is established by an internal current regulator, which maintains the bandgap voltage of 1.2V across the external programming resistor. See the I_{MOD} vs. R_{MODSET} graph in the *Typical Operating Characteristics* and select the value of R_{MODSET} that corresponds to the required current at +25°C. The current proportional to I_{BIAS} is set by an external resistor at the MODCOMP pin. Open circuiting the MODCOMP pin can turn off the interaction between I_{BIAS} and I_{MOD}.

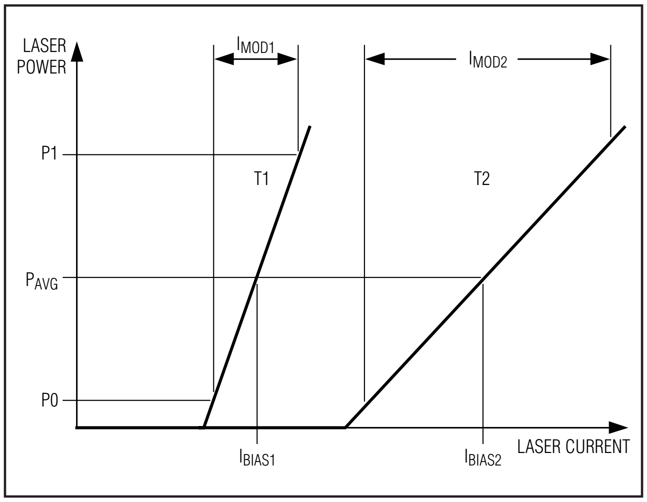


Figure 4. Laser Power vs. Current for a Change in Temperature

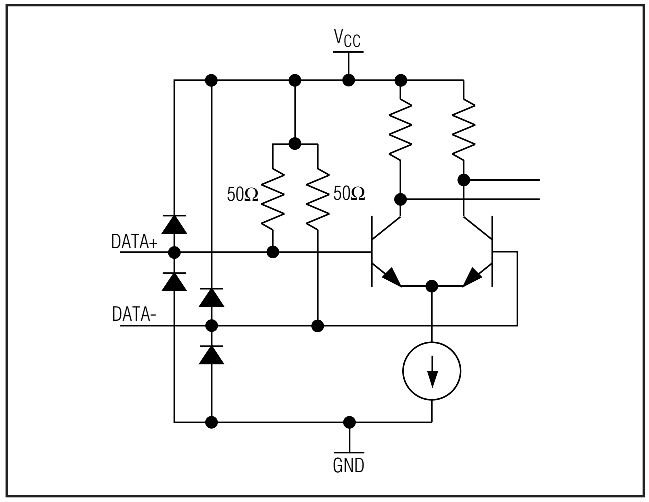


Figure 5. Equivalent Input Circuit

$$I_{MOD} = I_{MODS} + K \times I_{BIAS}$$

$$I_{MODS} = 200 \times \frac{1.2V}{R_{MODSET}}$$

$$K = 200 \times \frac{5}{500 + R_{MODCOMP}}$$

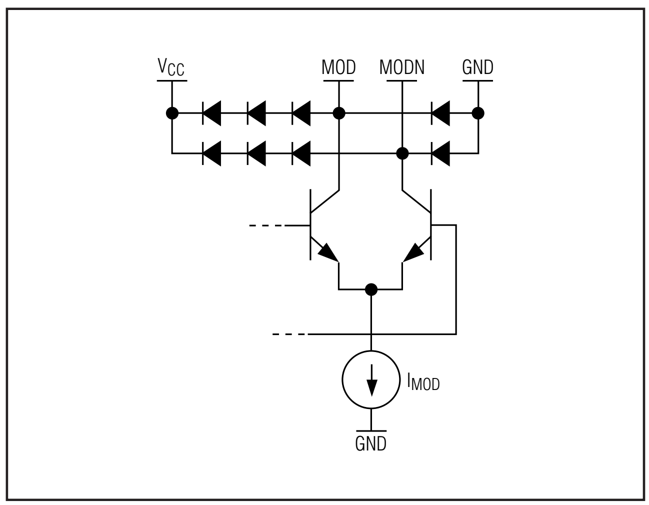


Figure 6. Equivalent Output Circuit

Applications Information

Layout Considerations

To minimize loss and crosstalk, keep connections between the MAX3863 output and the laser diode as short as possible. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground plane to minimize EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs, as well as the module output.

Laser Safety and IEC 825

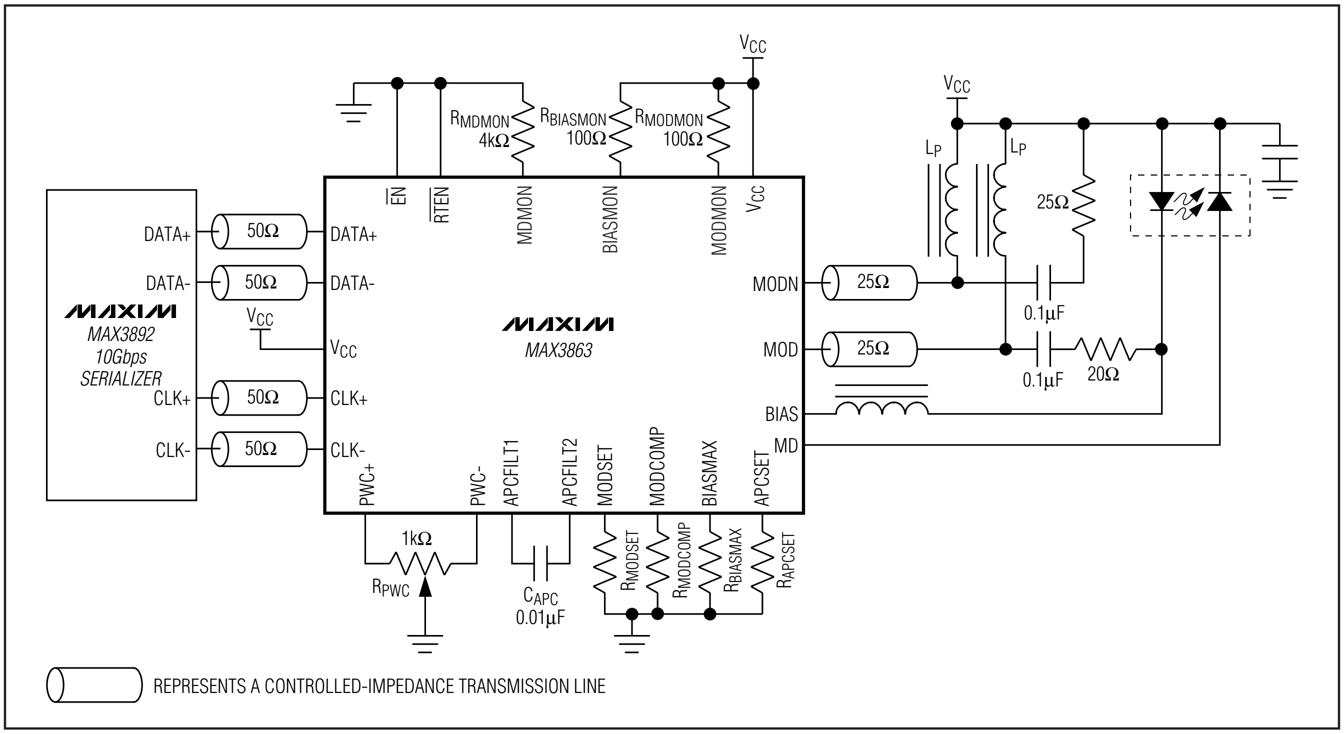
Using the MAX3863 laser driver alone does not ensure that a transmitter design is compliant with IEC825. The entire transmitter circuit and component selections must be considered. Determine the level of fault tolerance required by each application and recognize that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

Exposed Pad Package

The exposed pad on the 32-pin QFN provides a very low thermal resistive path for heat removal from the IC. The pad is also electrical ground on the MAX3863 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

2.7Gbps Laser Driver with Modulation Compensation

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 1786

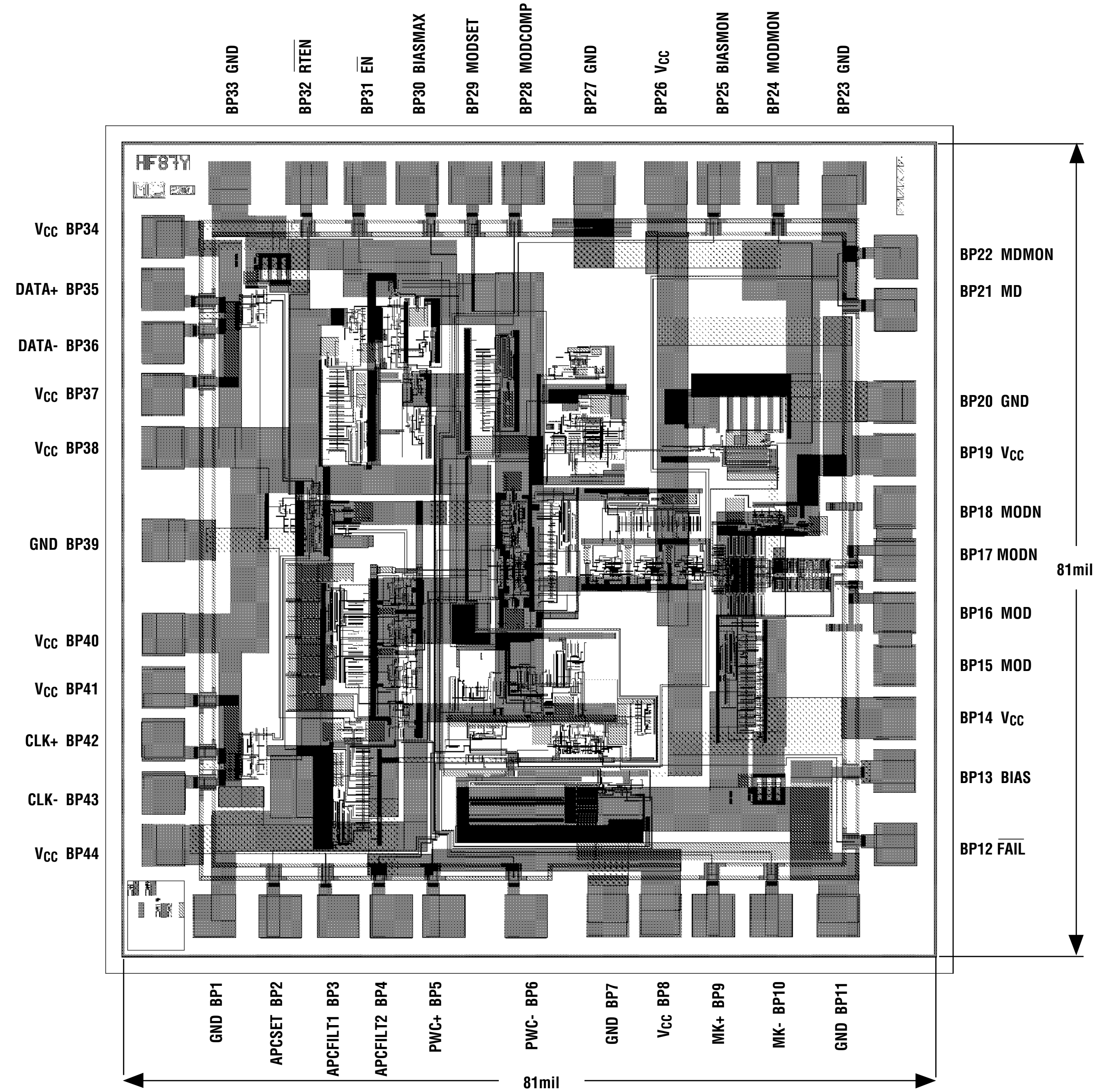
PROCESS: Bipolar

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255-3	21-0140
32 QFN-EP	G3255-1	21-0091

Chip Topography



2.7Gbps Laser Driver with Modulation Compensation

Pad Coordinates

NAME	PAD	COORDINATES (µM)	NAME	PAD	COORDINATES (µM)
GND	BP1	169, -122	GND	BP23	1675, 1630
APCSET	BP2	327, -122	MODMON	BP24	1515, 1630
APCFILT1	BP3	465, -122	BIASMON	BP25	1374, 1630
APCFILT2	BP4	591, -122	V_{CC}	BP26	1248, 1630
PWC+	BP5	717, -122	GND	BP27	1077, 1630
PWC-	BP6	913, -122	MODCOMP	BP28	906, 1630
GND	BP7	1109, -120	MODSET	BP29	780, 1630
V_{CC}	BP8	1235, -120	BIASMAX	BP30	654, 1630
MK+	BP9	1361, -120	$\overline{EN}$	BP31	528, 1630
MK-	BP10	1500, -120	$\overline{RTEN}$	BP32	390, 1630
GND	BP11	1660, -120	GND	BP33	205, 1630
$\overline{FAIL}$	BP12	1797, 50	V_{CC}	BP34	45, 1501
BIAS	BP13	1795, 225	DATA+	BP35	45, 1375
V_{CC}	BP14	1795, 351	DATA-	BP36	45, 1249
MOD	BP15	1795, 477	V_{CC}	BP37	45, 1123
MOD	BP16	1795, 603	V_{CC}	BP38	45, 997
MODN	BP17	1795, 729	GND	BP39	47, 776
MODN	BP18	1795, 855	V_{CC}	BP40	47, 551
V_{CC}	BP19	1795, 981	V_{CC}	BP41	47, 425
GND	BP20	1795, 1107	CLK+	BP42	47, 299
MD	BP21	1797, 1328	CLK-	BP43	47, 173
MDMON	BP22	1797, 1454	V_{CC}	BP44	47, 47

Coordinates are for the center of the pad.

Coordinate 0, 0 is the lower left corner of the passivation opening for pad 1.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/02	Initial release.	—
1	10/02	Corrected bond pad 24 to MODMON in the *Chip Topography*.	13
2	5/03	Added the PKG CODE column to the *Ordering Information* table.	1
		Updated the package outline drawing in the *Package Information* section.	15
3	1/06	Added the TQFN package to the *Ordering Information* table and *Absolute Maximum Ratings*.	1, 2
		Added the EP description to the *Pin Description* table.	6
		Changed the formulas in the *Current Monitors* section.	8
		Added the *Exposed Pad Package* section.	11
		Changed the R_{MDMON} and $R_{BIASMON}$ values from 100Ω and 4kΩ to 4kΩ and 100Ω, respectively, in the *Typical Operating Circuit*.	12
4	11/08	Removed the dice package from the *Ordering Information* table and *Chip Information* section.	1, 12
		Removed the package outline drawings and replaced with the table.	12