SCOPE: IMPROVED, SPST/SPDT ANALOG SWITCHES

Device Type	Generic Number	Circuit Function
01	DG417A(x)/883B	CMOS, SPST analog switch
02	DG418A(x)/883B	CMOS, SPST analog switch
03	DG419A(x)/883B	CMOS, SPDT analog switch

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
K	GDIP1-T08 or CDIP2-T08	8 LEAD CERDIP	J08
L	CDFP3-F10	10 LEAD FLATPACK	F10

Absolute Maximum Ratings

Voltage Referenced to V^-

V^- 44V
GND 25V
VL ..... (GND-0.3V) to V^+ +0.3V)
Digital Inputs, V_S, V_D 1/ ..... .(V^- -2V) to (V^+ +2V)
or 30mA whichever occurs first.
Continuous Current, Any terminal 1/ 30mA
Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max) 100mA

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
8 lead CERDIP(derate 8.0mW/°C above +70°C) 640mW
10 lead FLATPACK(derate 5.3mW/°C above +70°C) 421mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 8 lead CERDIP..... 55°C/W
Case Outline 10 lead FLATPACK ..... 85°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 8 lead CERDIP..... 125°C/W
Case Outline 10 lead FLATPACK ..... 190°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V^+) ..... +15V
Negative Supply Voltage (V^-) ..... -15V
V_{INL} (max) 0.8V
V_{INH} (min) 2.4V
Logic Supply Voltage (VL) ..... +5V

1/ Signals on S, D or IN exceeding V^+ or V^- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, VL=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	3/	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V^+=+13.5V, V^-=-13.5V, I_S=-10mA, V_D=±10V	1 2,3	All		35 45	Ω
Drain-Source ON Resistance Matching between Channels 4/	Δr_{DS} (ON)	V^+=+15V, V^-=-15V, I_S=-10mA, V_D=±10V	1 2,3	All		3.0 4.0	Ω
On-Resistance Flatness 4/	$r_{FLAT(ON)}$	V^+=+15V, V^-=-15V, I_S=-10mA, V_D=±5V	1 2,3	All		4.0 6.0	Ω
Source-OFF Leakage Current	$I_{S(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	All	-0.25 -20	0.25 20	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	01,02	-0.25 -20	0.25 20	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	03	-0.75 -40	0.75 40	nA
Drain-ON Leakage Current	$I_{D(ON)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	01,02	0.4 40	0.4 40	nA
Drain-ON Leakage Current	$I_{D(ON)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	03	-0.75 -40	0.75 40	nA
INPUT							
Input Current/Voltage High	I_{INH}	V_{IN}= 2.4V	1,2,3	All	-0.5	0.5	µA
Input Current/Voltage Low	I_{INL}	V_{IN}= 0.8V	1,2,3	All	-0.5	0.5	µA
SUPPLY							
Positive Supply Current	I+	V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Negative Supply Current	I-	V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Logic Supply Current	I_L	V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Ground Current	I_{GND}	V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
DYNAMIC							
Turn-On Time	t_{ON}	V_D=±10V, Figure 2	9 10,11	01,02		175 250	ns
Turn-Off Time	t_{OFF}	V_D=±10V, Figure 2	9 10,11	01,02		145 210	ns
Transition Time	t_{TRANS}	V_S=±10V, Figure 3	9 10,11	03		175 250	ns
Break-Before-Make Interval	t_D	V_{S1}=V_{S2}=±10V, Figure 4	9	03	5		ns
Charge Injection 3/	Q	V_{GEN}=0V, Figure 5	9	All		10	pC
TYPICALS		**DUAL SUPPLIES**			**5/**		
Off-Isolation Rejection Ratio	OIRR	R_L=500Ω, C_L=5pF, f=1MHz, figure 6 NOTE 6	Typical 4	All	68		dB
Crosstalk		R_L=50Ω, C_L=5pF, f=1MHz, figure 7 NOTE 7	Typical 4	03	85		dB
Drain & Source Off-Capacitance	$C_{D(OFF)}$ $C_{S(OFF)}$	V_D=0V, f=1MHz, Figure 8	Typical 4	All	8		pF
Drain & Source On-Capacitance	$C_{D(ON)}$ $C_{S(ON)}$	V_S=0V, f=1MHz, Figure 9	Typical 4	01,02 03	30 35		pF

TABLE 1. ELECTRICAL TESTS: SINGLE SUPPLY

TEST	Symbol	CONDITIONS T_A=+25°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	3/	1	All	0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V^+=+10.8V, I_S=-10mA, V_D=3.8V	1	All		100	Ω
DYNAMIC							
Charge Injection 3/	Q	C_L=10nF, V_{GEN}=0V, R_{GEN}=0Ω Figure 5	9	All		10	pC
TYPICALS		**SINGLE SUPPLY**			**5/**		
Positive & Negative Supply Current	I+ & I-	All channels on or off, V^+=+13.2, V_{IN}=0V or 5V	Typical 1	All	-0.0001		µA
Logic Supply Current and Ground Current	I_L & I_{GND}	All channels on or off, V_L=5.25V, V_{IN}=0V or 5V	Typical 1	All	-0.0001		µA
Turn-On Time	t_{ON}	V_D=8V, Figure 2	Typical 9	01,02	110		ns
Turn-Off Time	t_{OFF}	V_D=8V, Figure 2	Typical 9	01,02	40		ns
Break-Before-Make Interval	t_D	RL=1000Ω, C_L=35pF, Figure 4	Typical 9	03	60		ns

NOTE 2: This data sheet uses the algebraic convention, where the most negative value is a minimum and the most positive value is a maximum.
NOTE 3: Guaranteed by design.
NOTE 4: On-resistance match between channels and flatness are guarantee only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog range.
NOTE 5: Typical values at 25°C are for design aid only, are not guaranteed, and are not subject to production testing.
NOTE 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D=output, V_S=input to off switch.
NOTE 7: Between any two switches.

FIGURE 2: SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 3: TRANSITION TIME: See Commercial Data Sheet
FIGURE 4: BREAK-BEFORE-MAKE INTERVAL: See Commercial Data Sheet
FIGURE 5: CHARGE INJECTION: See Commercial Data Sheet
FIGURE 6: OFF-ISOLATION REJECTION RATIO: See Commercial Data Sheet
FIGURE 7: DG419 CROSSTALK: See Commercial Data Sheet
FIGURE 8: DRAIN-SOURCE OFF-CAPACITANCE: See Commercial Data Sheet
FIGURE 9: DRAIN-SOURCE ON-CAPACITANCE: See Commercial Data Sheet

Package		**ORDERING INFORMATION:**	
16 pin CERDIP	DG417AK/883B	DG418AK/883B	DG419AK/883B
16 pin Flatpack	DG417AL/883B	DG418AL/883B	DG419AL/883B

TRUTH TABLES:

DG417	DG417	DG418	DG418	DG419	DG419	DG419
LOGIC	SWITCH	LOGIC	SWITCH	LOGIC	SWITCH 1	SWITCH 2
0	ON	0	OFF	0	ON	OFF
1	OFF	1	ON	1	OFF	ON

TERMINAL CONNECTIONS:

	DG417/418	DG417/418	DG419	DG419
	J8	F10	J8	F10
1	S	S	D	D
2	NC	NC	S1	S1
3	GND	GND	GND	GND
4	V+	V+	V+	V+
5	VL	NC	VL	NC
6	IN	NC	IN	NC
7	V-	V_L	V-	V_L
8	D	IN	S2	IN
9		V-		V-
10		D		S2

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9,10,11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.