

Features

- Attenuation: 0.5 dB Steps to 15.5 dB
- Temperature Stability: ± 0.18 dB from -55°C to $+85^{\circ}\text{C}$ Typical
- Low DC Power Consumption
- Hermetic Surface Mount Package
- Integral TTL Driver
- $50\ \Omega$ Nominal Impedance
- Lead-Free CR-12 Package
- 260°C Reflow Compatible
- RoHS* Compliant

Description

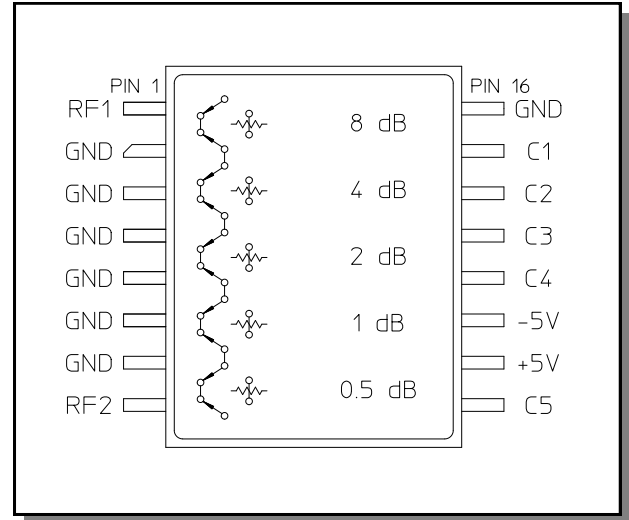
M/A-COM's AT-283-PIN is a GaAs FET 5-bit digital attenuator with a 0.5 dB minimum step size and 15.5 dB total attenuation. This attenuator and integral TTL driver is in a hermetically sealed ceramic 16 lead surface mount package. The AT-283-PIN is ideally suited for use where accuracy, fast switching, very low power consumption and low intermodulation products are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits. Environmental screening is available. Contact the factory for information.

Ordering Information

| Part Number | Package |
|--------------------|-------------------|
| AT-283-PIN | Bulk Packaging |
| MAAD-007229-0001TR | 1000 piece reel |
| MAAD-007229-0001TB | Sample Test Board |

Note: Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---------|----------|---------|----------|
| 1 | RF1 | 9 | C5 |
| 2 | GND | 10 | +5V |
| 3 | GND | 11 | -5V |
| 4 | GND | 12 | C4 |
| 5 | GND | 13 | C3 |
| 6 | GND | 14 | C2 |
| 7 | GND | 15 | C1 |
| 8 | RF2 | 16 | GND |

The metal bottom of the case must be connected to RF and DC ground.

Digital Attenuator 15.5 dB, 5-Bit, TTL Driver, DC-2.0 GHz

Rev. V7

Electrical Specifications: $T_A = 25^\circ\text{C}^1$

| Parameter | Test Conditions | Units | Min | Typ | Max |
|---|---|--------------------------|---|-----|-------|
| Reference Insertion Loss | DC-0.5 GHz | dB | — | — | 2.2 |
| | DC-1.0 GHz | dB | — | — | 2.5 |
| | DC-2.0 GHz | dB | — | — | 2.9 |
| Attenuation Accuracy ² | Any Single Bit Any Combination of Bits | DC-2.0 GHz DC-2.0 GHz | ± (0.25 +3% of attenuation setting in dB) dB ± (0.25 +3% of attenuation setting in dB) dB or ± 0.4 dB, whichever is greater | | |
| VSWR | DC-1.0 GHz | — | — | — | 1.6:1 |
| | DC-2.0 GHz | — | — | — | 1.7:1 |
| Trise, Tfall Ton, Toff Transients | 10% to 90% | nS | — | 10 | — |
| | 50% Control to 90/10% RF | nS | — | 27 | — |
| | In-band (peak—peak) | mV | — | 22 | — |
| 1 dB Compression ³ | Input Power | 0.05 GHz | dBm | +20 | — |
| | Input Power | 0.5-2.0 GHz | dBm | +28 | — |
| Input IP ₃ ³ | For two-tone input power up to +5 dBm | 0.05 GHz | dBm | +40 | — |
| | | 0.5-2.0 GHz | dBm | +47 | — |
| Input IP ₂ ³ | For two-tone input power up to +5 dBm | 0.05 GHz | dBm | +53 | — |
| | | 0.5-2.0 GHz | dBm | +68 | — |
| V _{CC} | — | V | 4.5 | 5.0 | 5.5 |
| V _{EE} | — | V | -8.0 | — | -5.0 |
| I _{CC} | V _{CC} = 4.5 to 5.5V V _{ctl} = 0 to 0.8V, or V _{CC} - 2.1V to V _{CC} | mA | — | — | 5.0 |
| I _{EE} | V _{EE} = -5.0 to -8.0V | mA | — | — | 1.0 |
| V _{ctl} | Logic 0 (TTL) | V | 0.0 | — | 0.8 |
| | Logic 1 (TTL) | V | 2.0 | — | 5.0 |
| Input Leakage Current (Low) | 0 to 0.8V | μA | — | — | 1.0 |
| Input Leakage Current (High) | 2.0 to 5.0V | μA | — | — | 1.0 |

1. All specifications apply when operated with bias voltages of +5.0V for V_{CC} and -5.0V to -8.0V for V_{EE}, and 50 Ω impedance at all ports unless otherwise specified.
2. This attenuator is guaranteed monotonic.
3. V_{EE} = -5.0V for the typical numbers given.

Absolute Maximum Ratings ^{4,5}

| Parameter | Absolute Maximum |
|--|---|
| Maximum Input Power 0.05 GHz 0.5-2.0 GHz | +27 dBm +34 dBm |
| V_{CC} | $-0.5V \leq V_{CC} \leq +7.0V$ |
| V_{EE} | $-8.5V \leq V_{EE} \leq +0.5V$ |
| $V_{CC} - V_{EE}$ | $-0.5V \leq V_{CC} - V_{EE} \leq 14.5V$ |
| V_{in}^6 | $-0.5V \leq V_{in} \leq V_{CC} + 0.5V$ |
| Operating Temperature | $-55^{\circ}C$ to $+125^{\circ}C$ |
| Storage Temperature | $-65^{\circ}C$ to $+150^{\circ}C$ |

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Handling Procedures

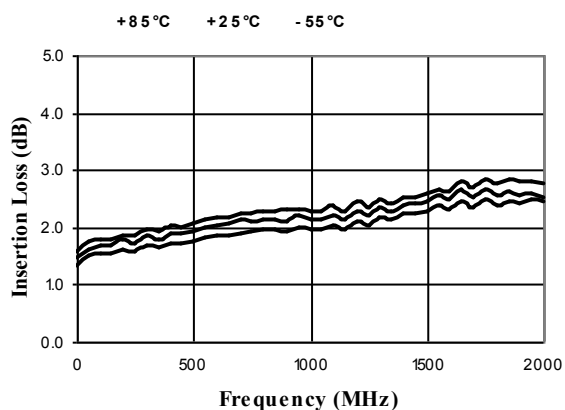
Please observe the following precautions to avoid damage:

Static Sensitivity

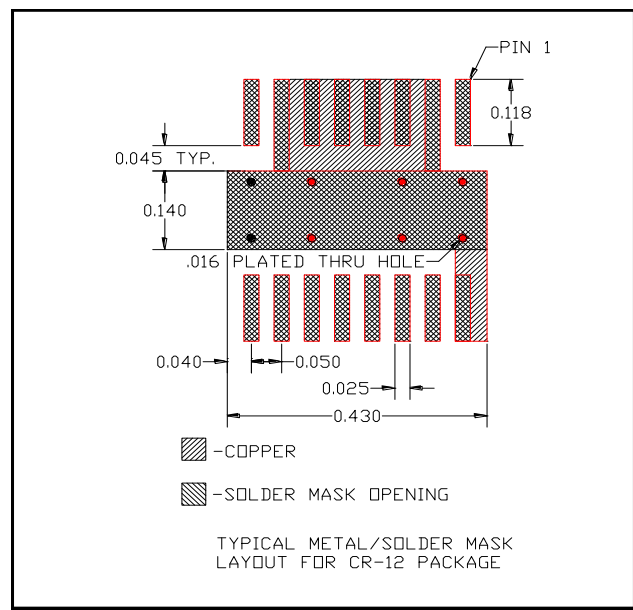
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves

Reference Insertion Loss vs. Frequency @ Temperature



Recommended PCB Configuration

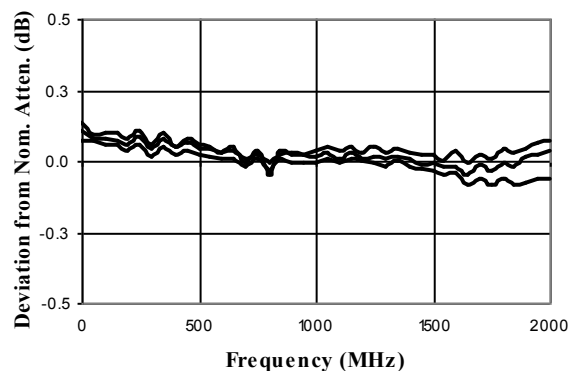


Truth Table (Digital Attenuator)

| Control Inputs | | | | | |
|----------------|----|----|----|----|-------------|
| C1 | C2 | C3 | C4 | C5 | Attenuation |
| 0 | 0 | 0 | 0 | 0 | Reference |
| 1 | 0 | 0 | 0 | 0 | 0.5 dB |
| 0 | 1 | 0 | 0 | 0 | 1 dB |
| 0 | 0 | 1 | 0 | 0 | 2 dB |
| 0 | 0 | 0 | 1 | 0 | 4 dB |
| 0 | 0 | 0 | 0 | 1 | 8 dB |
| 1 | 1 | 1 | 1 | 1 | 15.5 dB |

0 = TTL Low; 1 = TTL High

Attenuation Accuracy vs. Frequency 0.5, 1, 2 dB Bits

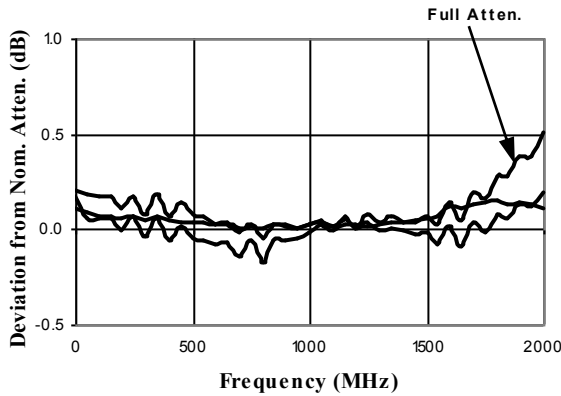


Digital Attenuator
15.5 dB, 5-Bit, TTL Driver, DC-2.0 GHz

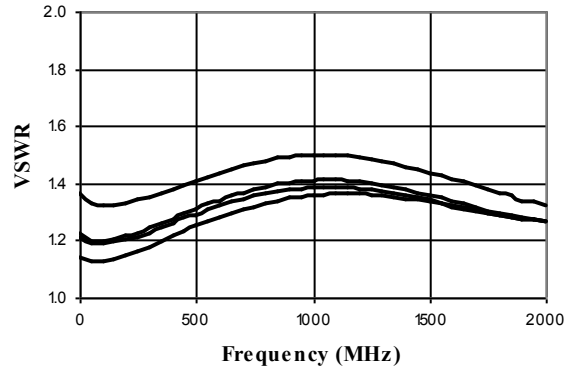
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Typical Performance Curves

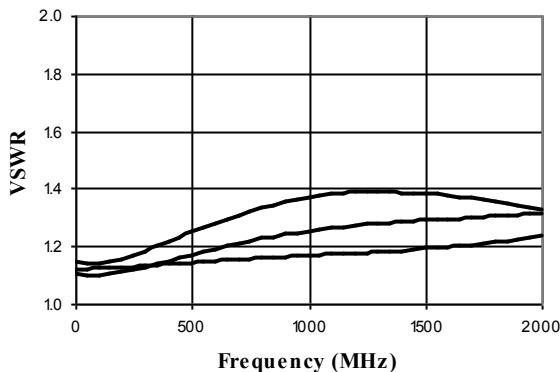
Attenuation Accuracy vs. Frequency 4, 8 dB Bits and Full Attenuation



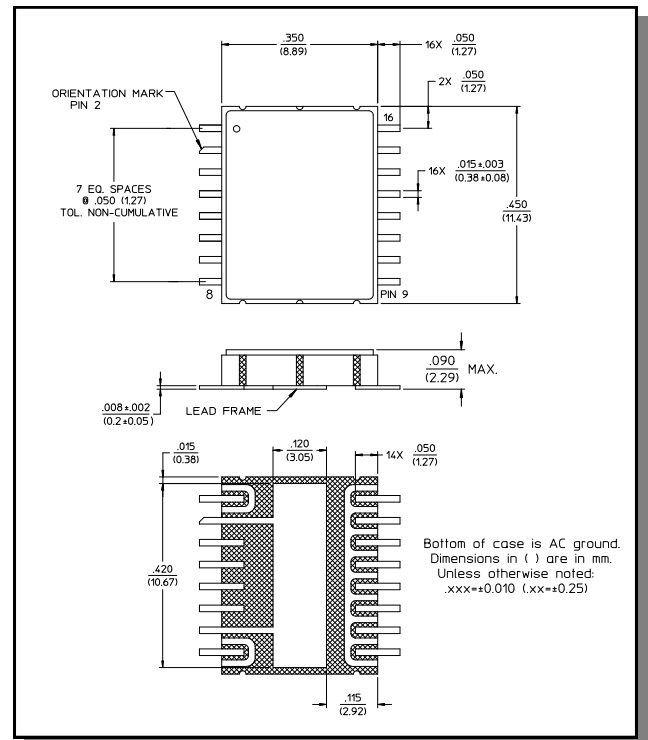
VSWR vs. Frequency Reference Loss, 0.5, 1, 2 dB Bits



VSWR vs. Frequency 4, 8 dB Bits and Full Attenuation



Lead-Free, CR-12 Ceramic Package[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations.

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