

Low power dual voltage comparator

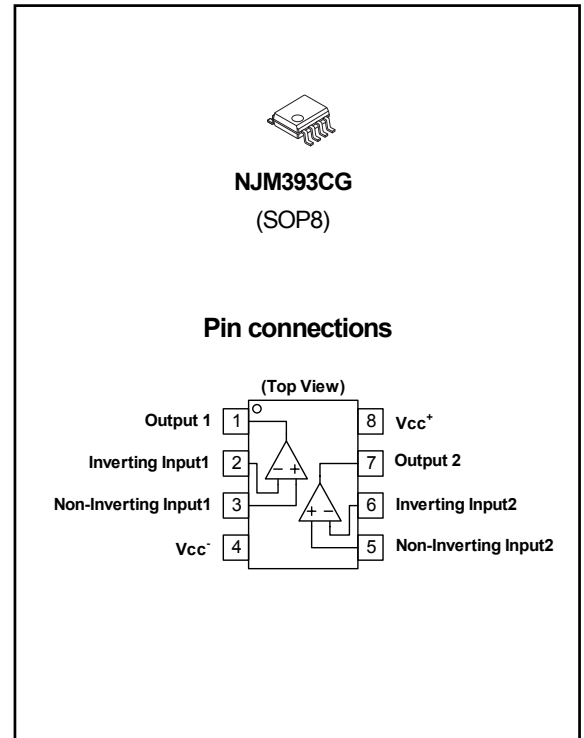
Features

- Wide single supply voltage range or dual supplies
+2V to +36V or $\pm 1V$ to $\pm 18V$
- Very low supply current : 0.45mA typ. at $V_{CC} = 5V$
- Low input bias current: 20nA typ.
- Low input offset current: 0.5nA typ.
- Low input offset voltage: 0.5mV typ.
- Input common-mode voltage range includes ground
- Low output saturation voltage: 80mV typ. ($I_{sink} = 4mA$)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs
- Internal ESD protection
Human body model (HBM) $\pm 2000V$ typ.

Description

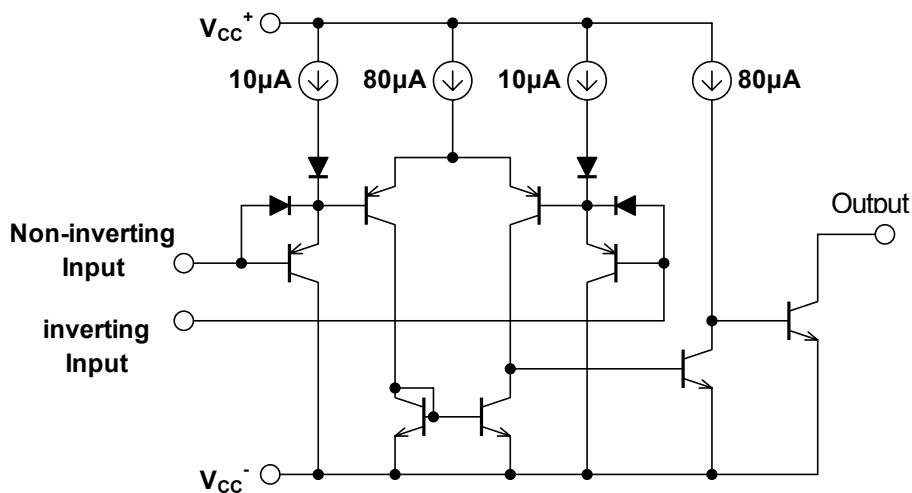
The NJM393C consist of two independent low power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.



1 Schematic diagram

Figure 1. Schematic diagram (1/2 NJM393C)



2 Absolute maximum ratings and operating conditions

Table1. Absolute maximum ratings (Tamb=25°C)

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage(V _{CC} ⁺ - V _{CC} ⁻)	36	V
V _{ID}	Differential input voltage	±36	V
V _{IN}	Input voltage ⁽¹⁾	- 0.3 to +36	V
-	Output short-circuit to V _{CC} ⁻ ⁽²⁾	Infinite	-
T _{stg}	Storage temperature range	-65 to +150	°C
T _j	Maximum junction temperature	150	°C
P _D	Power Dissipation	690 ⁽⁴⁾ 1000 ⁽⁵⁾	mW
θ _{ja}	thermal resistance junction to ambient ⁽³⁾	180 ⁽⁴⁾ 122 ⁽⁵⁾	°C/W
ψ _{jt}	thermal resistance junction to top surface of IC package ⁽³⁾	49 ⁽⁴⁾ 43 ⁽⁵⁾	°C/W

1. Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V_{CC}⁺.

2. Short-circuits from the output to V_{CC}⁺ can cause excessive heating and potential destruction.

3. Short-circuit can cause excessive heating and destructive dissipation. Values are typical.

4. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting

5. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4) mounting

Table2. Operating conditions (Tamb=25°C)

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage (V _{CC} ⁺ - V _{CC} ⁻)	2 to 36	V
V _{icm}	Common mode input voltage range (V _{CC} ⁺ =30V)		
	T _{amb}	0 to V _{CC} ⁺ -1.5	V
	T _{min} ≤ T _{amb} ≤ T _{max}	0 to V _{CC} ⁺ -2.0	
T _{oper}	Operating free-air temperature range	-40 to +85	°C

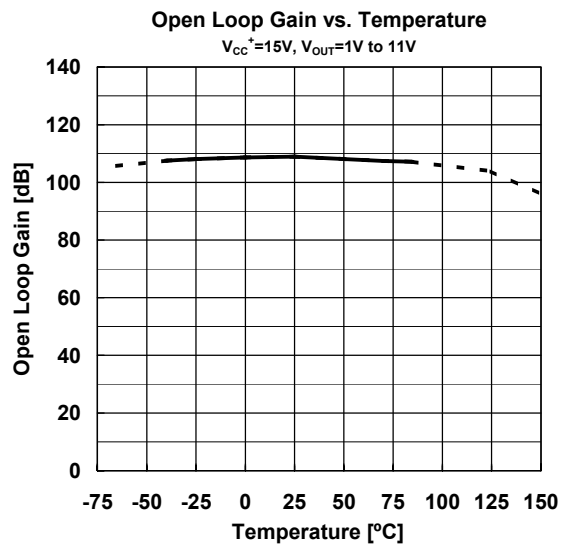
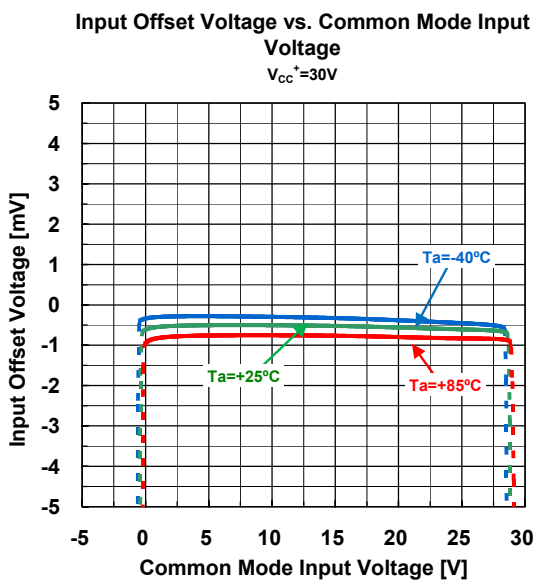
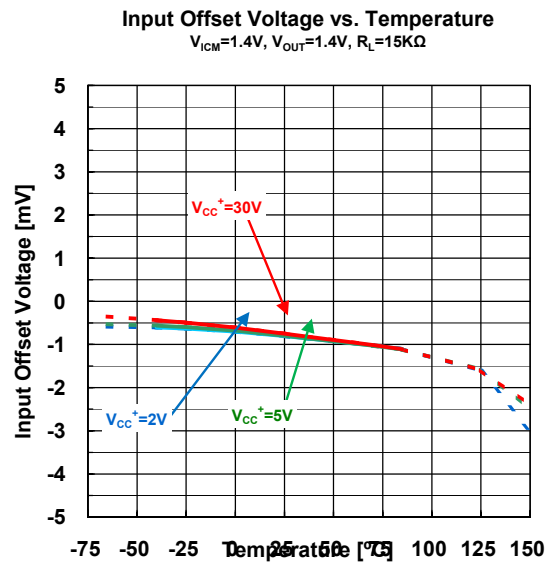
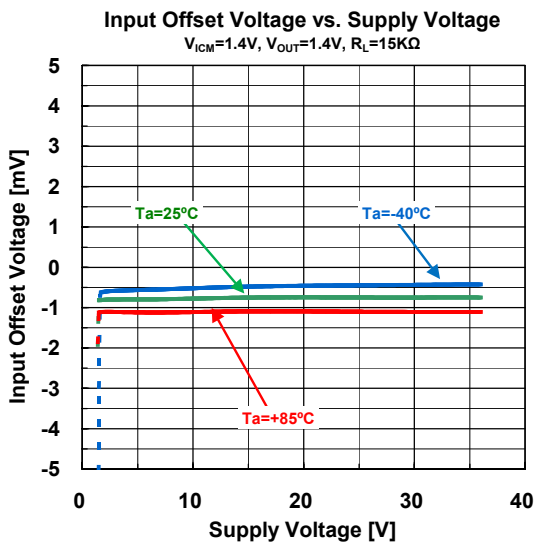
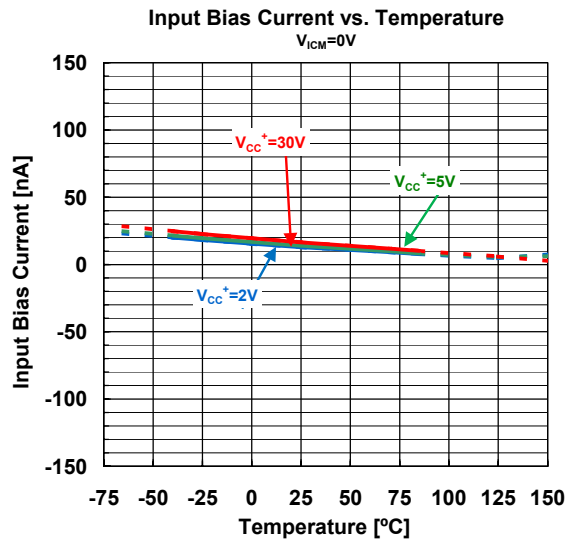
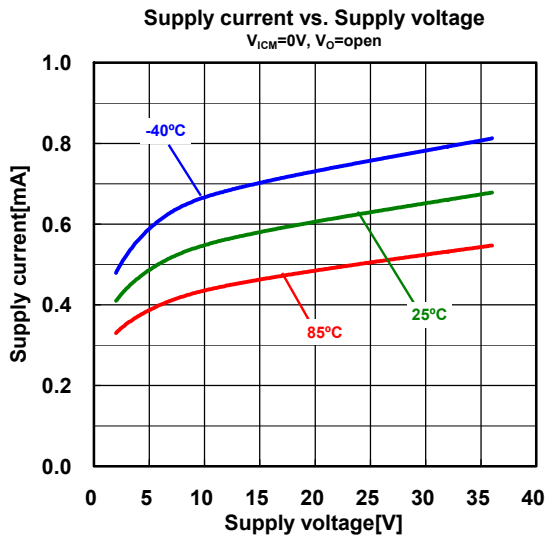
2 Electrical characteristics

Table3. $V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25^\circ C, T_{min}=0, T_{max}=70$ (unless otherwise specified)

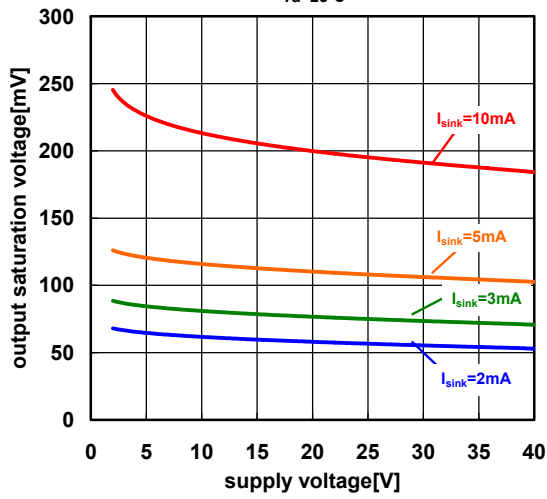
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾				
	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$ ⁽⁵⁾		0.5	5 9	mV
I_{io}	Input offset current				
	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$ ⁽⁵⁾		0.5	50 150	nA
I_{ib}	Input bias current ⁽²⁾				
	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$ ⁽⁵⁾		20	250 400	nA
A_{vd}	Large signal voltage gain $V_{CC} = 15V, R_L = 15k\Omega, V_o = 1V$ to 11V	50	200		V/mV
I_{CC}	Supply current (all comparators)				
	$V_{CC} = +5V, \text{no load}$ $V_{CC} = +30V, \text{no load}$		0.45 0.6	1 2.5	mA
V_{id}	Differential input voltage ⁽³⁾			V_{CC}^+	V
V_{OL}	Low level output voltage				
	$T_{amb}, V_{id} = -1V, I_{sink} = 4mA$ $T_{min} \leq T_{amb} \leq T_{max}$ ⁽⁵⁾		80	400 700	mV
I_{OH}	High level output current				
	$T_{amb}, V_{CC} = V_o = 30V, V_{id} = 1V$ $T_{min} \leq T_{amb} \leq T_{max}$ ⁽⁵⁾		0.1	1	nA μA
I_{sink}	Output sink current $V_{id} = 1V, V_o = 1.5V$	6	16		mA
t_{re}	Response Time ⁽⁴⁾ $R_L = 5.1k\Omega$ connected to V_{CC}^+		1.3		μs
t_{rel}	Large Signal Response Time $R_L = 5.1k\Omega$ connected to V_{CC}^+ $e_i = TTL, V_{(ref)} = +1.4V$		250		ns

1. At output switch point, $V_o = 1.4V, R_S = 0$ with V_{CC}^+ from 5V to 30V, and over the full common-mode range (0V to $V_{CC}^+ - 1.5V$).
2. The direction of the input current is out of the IC due to the PNP input stage.
3. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage must not be less than $-0.3V$ (or $0.3V$ below the negative power supply, if used).
4. The response time specified is for a 100mV input step with 5mV overdrive.
5. This parameter is not 100% test.

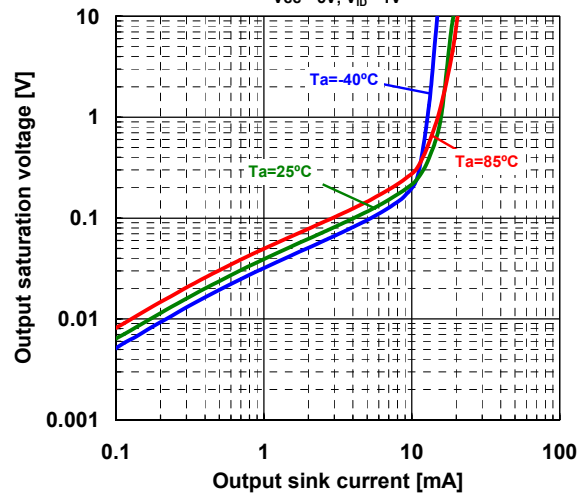
■ TYPICAL CHARACTERISTICS



Output saturation voltage vs. supply voltage
 $T_a=25^\circ\text{C}$

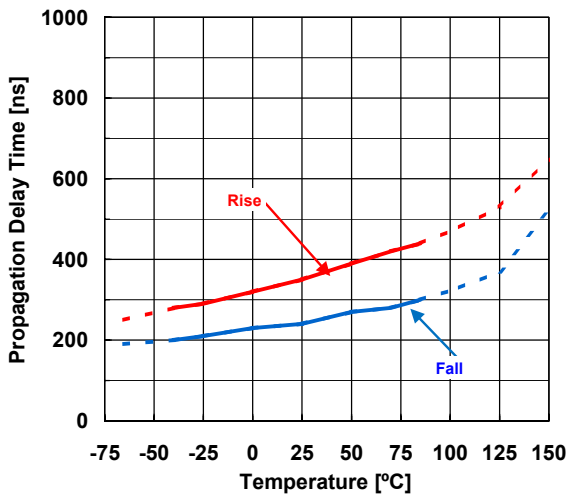


Output saturation voltage vs. output sink current
 $V_{\text{CC}}=5\text{V}, V_{\text{ID}}=-1\text{V}$



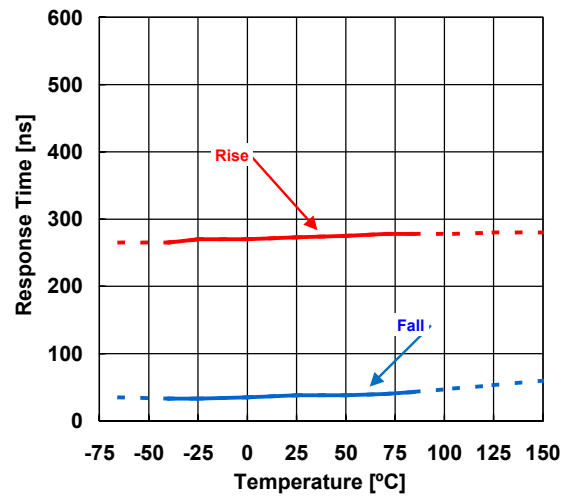
Propagation Delay Time vs. Temperature

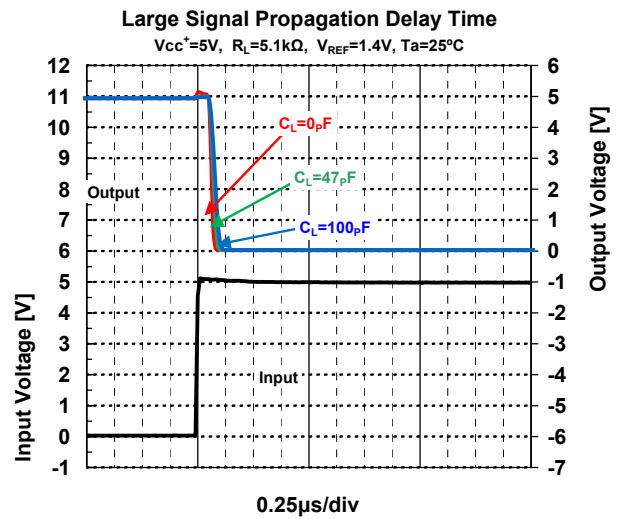
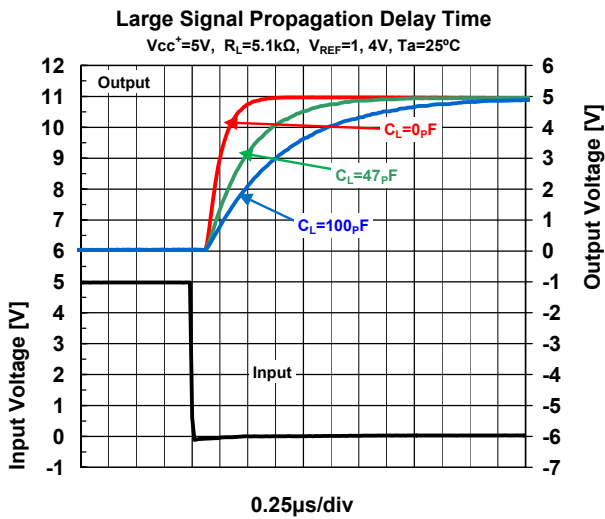
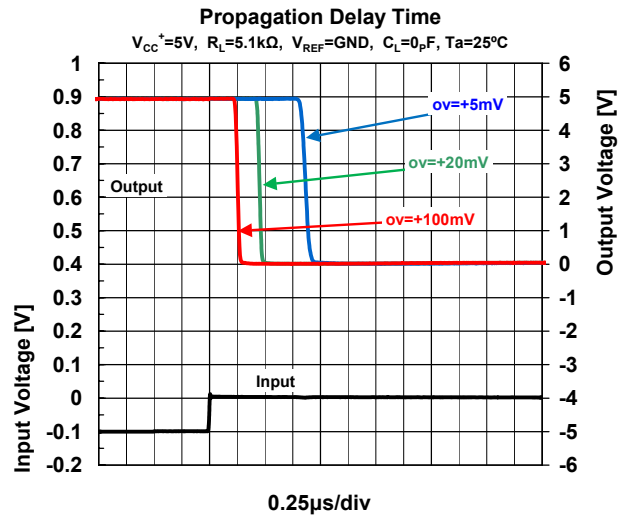
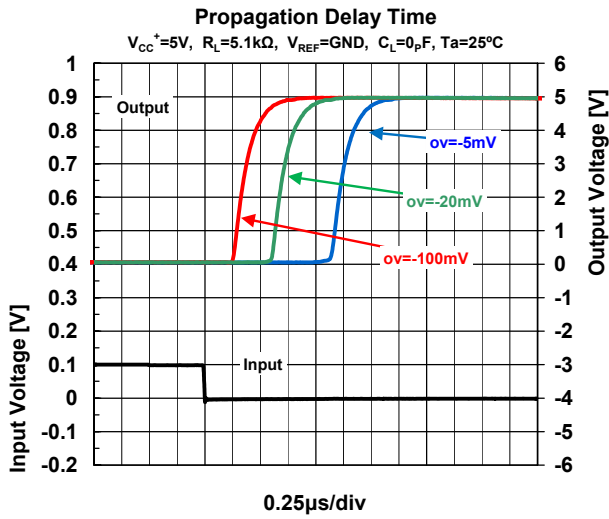
$V_{\text{CC}}=5\text{V}, V_{\text{IN}}=\text{GND}, V_{\text{IN}}=200\text{mV}_{\text{pp}}, \text{ov}=100\text{mV}, R_{\text{L}}=5.1\text{k}\Omega$



Response Time vs. Temperature

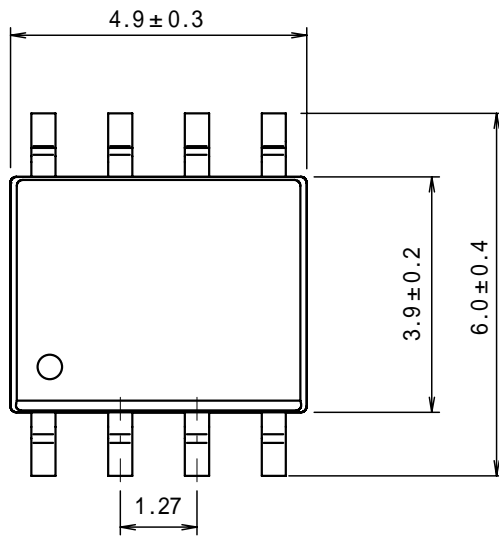
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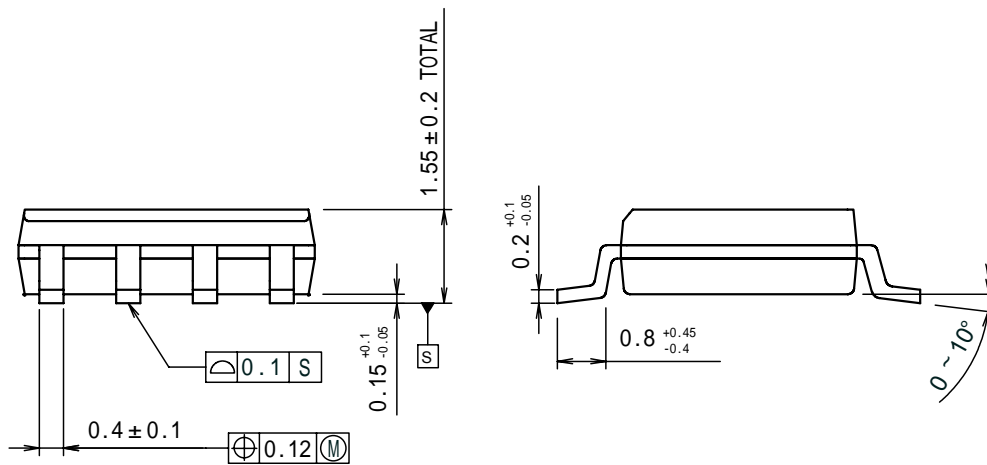


PACKAGE OUTLINE UNIT : mm

SOP8



UNIT: mm



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