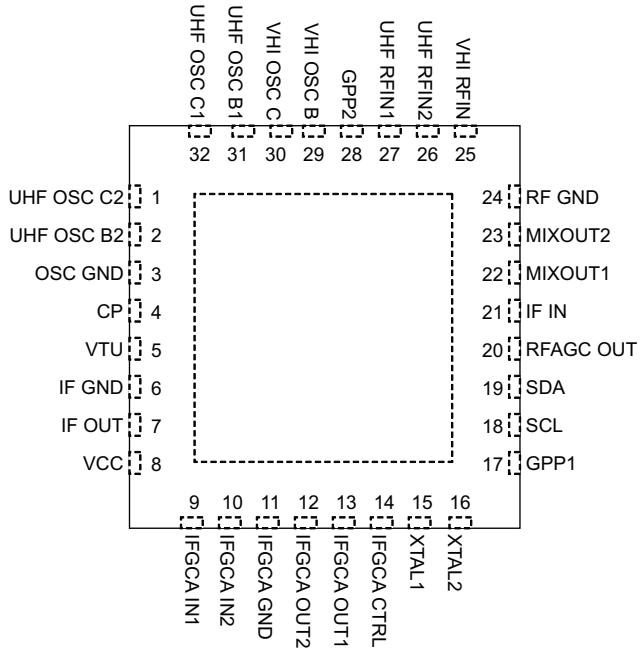
DIGITAL TV TUNER IC

Check for Samples: SN761646

FEATURES

- **Integrated Mixer/Oscillator/PLL and IF GCA**
- **VHF-H, UHF 2-Band Local Oscillator**
- **I²C Bus Protocol (Fixed Address)**
- **30-V Tuning Voltage Output**
- **Two General Purpose Ports**
- **Selectable Wide/Narrow Band RF AGC Detector**
- **Crystal Oscillator 4 MHz/8 MHz/16 MHz Support**
- **Programmable Reference Divider Ratio (24/28/48/56/64/96/128)**
- **IF GCA Enable/Disable Control**
- **Standby Mode**
- **5-V Power Supply**
- **32-Pin Quad Flatpack No Lead (QFN) Package**

RHB PACKAGE
(TOP VIEW)



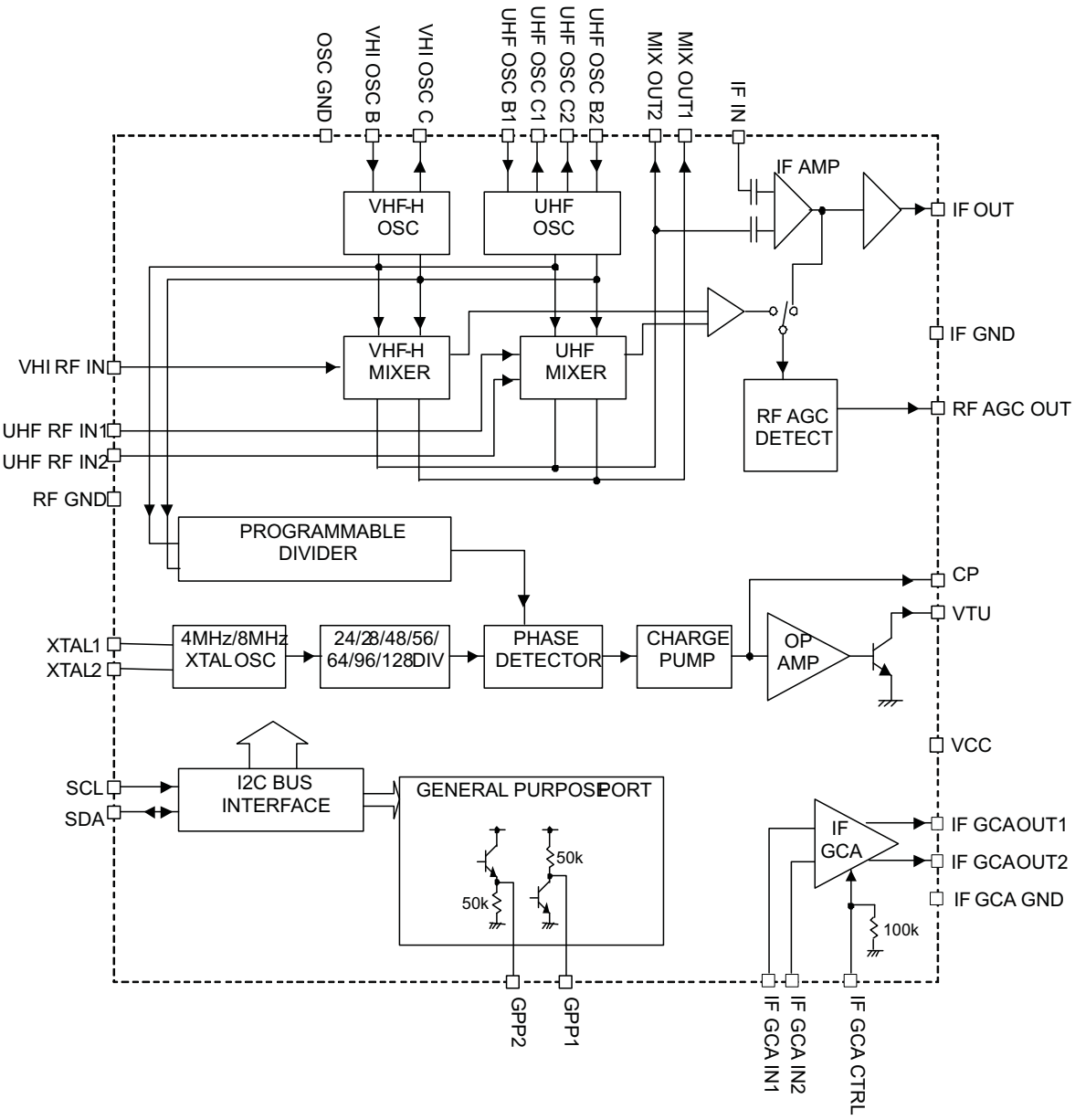
APPLICATIONS

- **Digital TVs**
- **Digital CATVs**
- **Set-Top Boxes**

DESCRIPTION

The SN761646 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, two-band local oscillator and mixer, RF AGC detector circuit and IF gain controlled amplifier, and is available in a small outline package.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

Table 1.

TERMINAL		DESCRIPTION	SCHEMATIC
NAME	NO.		
CP	4	Charge-pump output	Figure 1
GPP1	17	General purpose port output 1 (open collector type)	Figure 2
GPP2	28	General purpose port output 2 (emitter follower type)	Figure 3
IFGCA CTRL	14	IF GCA control voltage input	Figure 4
IFGCA GND	11	IF GCA ground	
IFGCA IN1	9	IF GCA input	Figure 5
IFGCA IN2	10	IF GCA input	Figure 5
IFGCA OUT1	13	IF GCA output	Figure 6
IFGCA OUT2	12	IF GCA output	Figure 6
IF GND	6	IF ground	
IF IN	21	IF amplifier input	Figure 7
IF OUT	7	IF amplifier output	Figure 8
MIXOUT1	22	Mixer output 1	Figure 9
MIXOUT2	23	Mixer output 2	Figure 9
OSC GND	3	Oscillator ground	
RF AGC OUT	20	RF AGC output	Figure 10
RF GND	24	Mixer ground	
SCL	18	Serial clock input	Figure 11
SDA	19	Serial data input/output	Figure 12
UHF OSC B1	31	UHF oscillator base 1	Figure 13
UHF OSC B2	2	UHF oscillator base 2	Figure 13
UHF OSC C1	32	UHF oscillator collector 1	Figure 13
UHF OSC C2	1	UHF oscillator collector 2	Figure 13
UHF RF IN1	27	UHF RF input 1	Figure 14
UHF RF IN2	26	UHF RF input 2	Figure 14
V_{CC}	8	Supply voltage	
VHI OSC B	29	VHF-H oscillator base	Figure 15
VHI OSC C	30	VHF-H oscillator collector	Figure 15
VHI RF IN	25	VHF-H RF input	Figure 16
VTU	5	Tuning voltage amplifier output	Figure 17
XTAL1	15	Crystal oscillator	Figure 18
XTAL2	16	Crystal oscillator	Figure 18

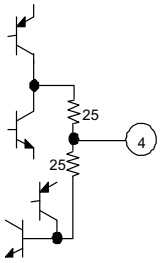


Figure 1. CP

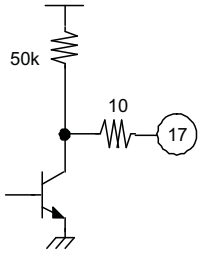


Figure 2. GPP1

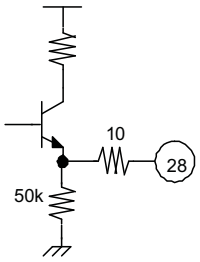


Figure 3. GPP2

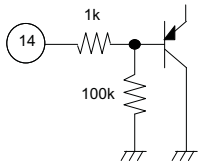


Figure 4. IF GCA CTRL

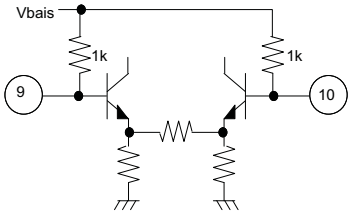


Figure 5. . IF GCA IN1 and IF GCA IN2

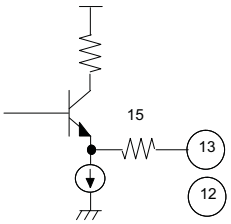


Figure 6. IF GCA OUT1 and IF GCA OUT2

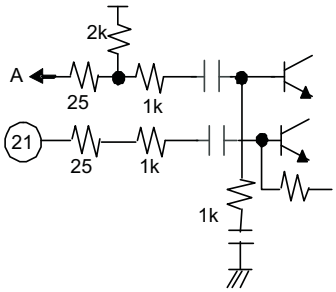


Figure 7. IF IN

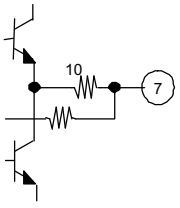


Figure 8. IF OUT

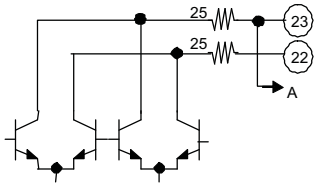


Figure 9. MIXOUT1 and MIXOUT2

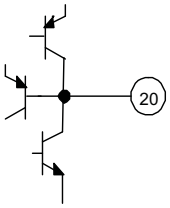


Figure 10. RF AGC OUT

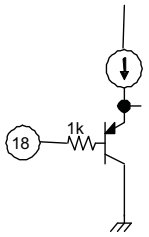


Figure 11. SCL

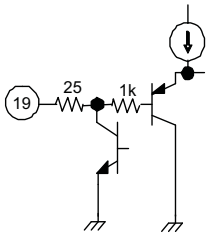


Figure 12. SDA

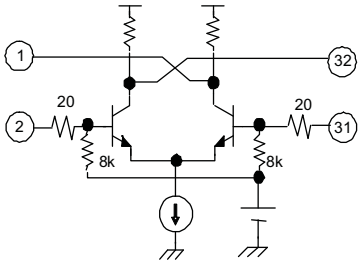


Figure 13. UHF OSC B1, UHF OSC B2, UHF OSC C1, and UHF OSC C2

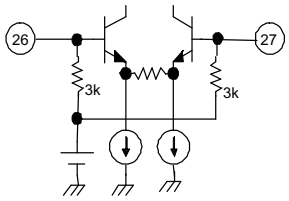


Figure 14. UHF RF IN1 and UHF RF IN2

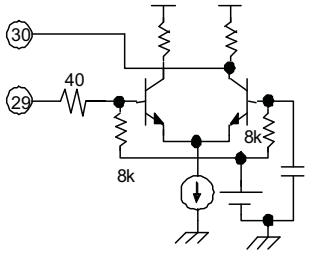


Figure 15. VHI OSC B and VHI OSC C

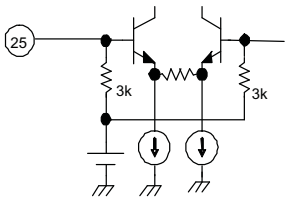


Figure 16. VHI RF IN

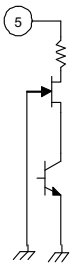


Figure 17. VTU

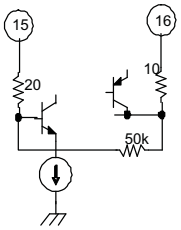


Figure 18. XTAL1 and XTAL2

ABSOLUTE MAXIMUM RATINGS(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{CC}	Supply voltage range (3)	V_{CC}	–0.4 to 6.5	V
V_{GND}	Input voltage range 1 (3)	RF GND, OSC GND	–0.4 to 0.4	V
V_{VTU}	Input voltage range 2 (3)	VTU	–0.4 to 35	V
V_{IN}	Input voltage range 3 (3)	Other pins	–0.4 to 6.5	V
T_A	Operating free-air temperature range		–20 to 85	°C
θ_{JA}	Package thermal impedance(4)		32.4	°C/W
T_{stg}	Storage temperature range		–65 to 150	°C
T_J	Maximum junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Overshoot or undershoot of input voltage beyond absolute maximum rating may induce failure. Latch up performance exceeds +/-100mA per JESD78, except for GPP1 (pin 17).
(3) Voltage values are with respect to the IF GND of the circuit.
(4) The package thermal impedance is calculated in accordance with JESD 51-5 (High-K).

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}	4.5	5	5.5	V
V_{VTU}	Tuning supply voltage	VTU		30	33	V
I_{GPP1}	Output current of general purpose port 1	GPP1			–5	mA
I_{GPP2}	Output current of general purpose port 2	GPP2			10	mA
T_A	Operating free-air temperature		–20		85	°C

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

IF IN, MIXOUT1, and MIXOUT2 (pins 21–23) withstand 1.5 kV; all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

ELECTRICAL CHARACTERISTICS

Total Device and Serial Interface

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}1$	Supply current 1	BS[2:1] = 10, $I_{GPP1,2}$ = 0 mA, IFGCA disabled		80		mA
$I_{CC}2$	Supply current 2	BS[2:1] = 10, $I_{GPP1,2}$ = 0 mA, IFGCA enabled		110		mA
$I_{CC-STBY}$	Standby supply current	BS[2:1] = 11		8	14	mA
V_{IH}	High-level input voltage (SCL, SDA)		2.3			V
V_{IL}	Low-level input voltage (SCL, SDA)				1.05	V
I_{IH}	High-level input current (SCL, SDA)				10	µA
I_{IL}	Low-level input current (SCL, SDA)		–10			µA
V_{POR}	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
I^2C Interface						
V_{OL}	Low-level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
I_{SDAH}	High-level output leakage current (SDA)	V_{SDA} = 5.5 V			10	µA
f_{SCL}	Clock frequency (SCL)			100	400	kHz
t_{HD-DAT}	Data hold time	See Figure 19	0		0.9	µs
t_{BUF}	Bus free time		1.3			µs
t_{HD-STA}	Start hold time		0.6			µs
t_{LOW}	SCL-low hold time		1.3			µs
t_{HIGH}	SCL-high hold time		0.6			µs
t_{SU-STA}	Start setup time		0.6			µs
t_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time (SCL, SDA)				0.3	µs
t_f	Fall time (SCL, SDA)				0.3	µs
t_{SU-STO}	Stop setup time		0.6			µs

PLL and General Purpose Port

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	512		32767	
f_{XTAL}	Crystal oscillator frequency	See Figure 21		4	16	MHz
Z_{XTAL}	Crystal oscillator input impedance	8 MHz, V_{CC} = 5 V, T_A = 25°C		1.5		kΩ
V_{VTUL}	Tuning amplifier low-level output voltage	R_L = 22 kΩ, VTU = 30 V	0.2	0.45	0.6	V
I_{VTUOFF}	Tuning amplifier leakage current	Tuning amplifier = off, VTU = 30 V			10	µA
I_{CP11}	Charge-pump current	CP[2:0] = 011	450	600	750	µA
I_{CP10}		CP[2:0] = 010	250	350	450	
I_{CP01}		CP[2:0] = 001	100	140	200	
I_{CP00}		CP[2:0] = 000	35	70	95	
I_{CP100}		CP[2:0] = 100, Mode = 1	650	900	1200	
V_{CP}	Charge-pump output voltage	PLL locked		1.95		V
I_{CPOFF}	Charge-pump leakage current	V_{CP} = 2 V, T_A = 25°C	–15		15	nA
I_{GPP1}	General purpose port 1 (GPP1) output current				–5	mA
V_{GPP1ON}	General purpose port 1 (GPP1) output ON voltage	I_{GPP1} = –2 mA, V_{CC} = 5 V, T_A = 25°C			0.6	V
I_{GPP2}	General purpose port 2 (GPP2) output current				10	mA
V_{GPP21}	General purpose port 2 (GPP2) output voltage	I_{GPP2} = 10 mA	2.9			V
V_{GPP22}		I_{GPP2} = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.4	3.6		
$I_{GPP2OFF}$	General purpose port 2 (GPP2) OFF leakage current	V_{GPP2} = 0 V			8	µA

RF AGC

V_{CC} = 5 V, T_A = 25°C, measured in Figure 20 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OAGC0}	RF AGC output source current	ATC = 0		300		nA
I_{OAGC1}		ATC = 1		9		µA
$I_{OAGCSINK}$	RF AGC peak sink current	ATC = 0		100		µA
V_{OAGCH}	RFAGCOUT output high voltage (max level)	ATC = 1	3.5	4.0	4.5	V
V_{OAGCL}	RFAGCOUT output low voltage (min level)	ATC = 1		0.3		V
$V_{AGCSP00}$	Start-point IF output level	ATP[2:0] = 000, ATC=0, AISL=0		114		dBµV
$V_{AGCSP01}$		ATP[2:0] = 001, ATC=0, AISL=0		112		
$V_{AGCSP02}$		ATP[2:0] = 010, ATC=0, AISL=0		110		
$V_{AGCSP03}$		ATP[2:0] = 011, ATC=0, AISL=0		108		
$V_{AGCSP04}$		ATP[2:0] = 100, ATC=0, AISL=0		106		
$V_{AGCSP05}$		ATP[2:0] = 101, ATC=0, AISL=0		104		
$V_{AGCSP06}$		ATP[2:0] = 110, ATC=0, AISL=0		102		

Mixer, Oscillator, IF Amplifier (DIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 20 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
G_{C4D}	Conversion gain (mixer-IF amplifier), VHF-HIGH	f_{in} = 177 MHz(1)	29	dB
G_{C6D}		f_{in} = 467 MHz(1)	29	
G_{C7D}	Conversion gain (mixer-IF amplifier), UHF	f_{in} = 473 MHz(1)	29	dB
G_{C9D}		f_{in} = 864 MHz(1)	29	
NF_{4D}	Noise figure, VHF-HIGH	f_{in} = 177 MHz	9	dB
NF_{6D}		f_{in} = 467 MHz	10	
NF_{7D}	Noise figure, UHF	f_{in} = 473 MHz	10	dB
NF_{9D}		f_{in} = 864 MHz	12	
CM_{4D}	Input voltage causing 1% cross-modulation distortion, VHF-HIGH	f_{in} = 177 MHz(2)	79	dBµV
CM_{6D}		f_{in} = 467 MHz(2)	79	
CM_{7D}	Input voltage causing 1% cross-modulation distortion, UHF	f_{in} = 473 MHz(2)	77	dBµV
CM_{9D}		f_{in} = 864 MHz(2)	77	
V_{IFO4D}	IF output voltage, VHF-HIGH	f_{in} = 177 MHz	117	dBµV
V_{IFO6D}		f_{in} = 467 MHz	117	
V_{IFO7D}	IF output voltage, UHF	f_{in} = 473 MHz	117	dBµV
V_{IFO9D}		f_{in} = 864 MHz	117	
Φ_{PLVL4D}	Phase noise, VHF-HIGH	f_{in} = 177 MHz(3)	–85	dBc/Hz
Φ_{PLVL6D}		f_{in} = 467 MHz(4)	–77	
Φ_{PLVL7D}	Phase noise, UHF	f_{in} = 473 MHz(3)	–80	dBc/Hz
Φ_{PLVL9D}		f_{in} = 864 MHz(4)	–77	

(1) IF = 44 MHz, RF input level = 70 dBµV
(2) $f_{undes} = f_{des} \pm 6$ MHz, Pin = 70 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 1 kHz, CP current = 350 µA, reference divider = 128, crystal = 8 MHz
(4) Offset = 1 kHz, CP current = 900 µA, reference divider = 128, crystal = 8 MHz

IF Gain Controlled Amplifier

V_{CC} = 5 V, T_A = 25°C, measured in Figure 20 reference measurement circuit at 50-Ω system, IF = 45.75 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IFGCA}	Input current (IF GCA CTRL)	V_{IFGCA} = 3 V		30	60	µA
$V_{IFGCAMAX}$	Maximum gain control voltage	Gain Maximum	3		V_{CC}	V
$V_{IFGCAMIN}$	Minimum gain control voltage	Gain Minimum	0		0.2	V
$G_{IFGCAMAX}$	Maximum gain	V_{IFGCA} = 3 V		65		dB
$G_{IFGCAMIN}$	Minimum gain	V_{IFGCA} = 0 V		–1		dB
GCR_{IFGCA}	Gain control range	V_{IFGCA} = 0 V to 3 V		66		dB
$V_{IFGCAOUT}$	Output voltage	Single-ended output, V_{IFGCA} = 3 V		2.1		Vp-p
NF_{IFGCA}	Noise figure	VIFGCA=3V		11		dB
$IM3_{IFGCA}$	Third order intermodulation distortion	$f_{IFGCAIN1}$ = 43 MHz, $f_{IFGCAIIN2}$ = 44 MHz, $V_{IFGCAOUT}$ = –2 dBm, V_{IFGCA} = 3 V		–50		dBc
$IIP3_{IFGCA}$	Input intercept point	V_{IFGCA} = 0 V		11		dBm
$R_{IFGCAIN}$	Input resistance (IF GCA IN1, IF GCA IN2)			1		kΩ
$R_{IFGCAOUT}$	Output resistance (IF GCA OUT1, IF GCA OUT2)			25		Ω

FUNCTIONAL DESCRIPTION

I²C Bus Mode

I²C Write Mode (R/$\overline{W}$ = 0)

Table 2. Write Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	0	0	R/$\overline{W}$ = 0	A(1)
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A(1)
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A(1)
Control byte 1 (CB1)	1	0	ATP2	ATP1	ATP0	RS2	RS1	RS0	A(1)
Band switch byte (BB)	CP1	CP0	AISL	0	GPP2	GPP1	BS2	BS1	A(1)
Control byte 2 (CB2)	1	1	ATC	MODE	T3/DISGCA	T2	T1/CP2	T0	A(1)

(1) A : acknowledge

Table 3. Write Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
ADB	Address byte (Write mode) ADB[7:0]=11000000	
N[14:0]	Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$	N14 = N13 = N12 = ... = N0 = 0
ATP[2:0]	RF AGC start-point control bits (see Table 4)	ATP[2:0] = 000
RS[2:0]	Reference divider ratio-selection bits (see Table 5)	RS[2:0] = 000
CP[1:0]	Charge-pump current-set bit (see Table 6)	CP[1:0] = 00
AISL	RF AGC detector input selection bit AISL = 0: IF amplifier AISL = 1: Mixer output	AISL = 0
GPP[2:1]	General purpose port output control bit GPPn = 0: Output transistor = OFF GPPn = 1: Output transistor = ON	GPP[2:1]=00
BS[4:1]	Band selection bits **BS2 BS1** 0 1 Not allowed 1 0 VHF-HI 0 0 UHF 1 1 Standby mode/stop MOP function	BS[2:1]=00
ATC	RF AGC current-set bit ATC = 0: Current = 300 nA ATC = 1: Current = 9 µA	ATC = 0
Mode T3/DISGCA T2 T1/CP2 T0	Mode = 0: IF GCA enabled T3/DISGCA, T2, T1/CP2, T0 are test bits (see Table 7)	MODE = 0 T[3:0] = 0000
	Mode = 1: T3/DISGCA =0 : IF GCA enabled T3/DISGCA =1 : IF GCA disabled T1/CP2 : Icp control bit, See Table 6	

Table 4. RF AGC Start Point

ATP2	ATP1	ATP0	IFOUT LEVEL (dBµV)
0	0	0	114
0	0	1	112
0	1	0	110
0	1	1	108
1	0	0	106
1	0	1	104
1	1	0	102
1	1	1	Disabled (Hi-Z)

Table 5. Reference Divider Ratio

RS2	RS1	RS0	REFERENCE DIVIDER RATIO
0	0	0	24
0	0	1	28
0	1	0	48
0	1	1	56
1	0	0	64
1	0	1	96
1	1	0	128
1	1	1	Reserved

Table 6. Charge-Pump Current

MODE	CP2	CP1	CP0	CHARGE PUMP CURRENT (µA)
X	0	0	0	70
X	0	0	1	140
X	0	1	0	350
X	0	1	1	600
1	1	0	0	900

Table 7. Test Bits (1)

MODE	T3/DISGCA	T2	T1/CP2	T0	DEVICE OPERATION
0	0	0	0	X	Normal operation
1	X	X	X	X	Normal operation
0	X	1	X	X	Test mode
0	1	X	X	X	Test mode

(1) RFAGC is not available in test mode.

I^2C Read Mode (R/$\overline{W}$ = 1)

Table 8. Read Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	0	0	R/$\overline{W}$ = 1	A (1)
Status byte (SB)	POR	FL	1	1	1	1	1	1	–

(1) A : acknowledge

Table 9. Read Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
ADB	Address byte (Read mode) ADB[7:0] = 11000001	
POR	Power-on-reset flag POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL (1)	In-lock flag PLL locked (FL = 1), unlocked (FL = 0)	

(1) Lock detector works by using phase error pulse at the phase detector. Lock flag (FL) is set or reset according to this pulse width disciminator. Hence unstableness of PLL may cause the lock detect circuit to malfunction. In order to stable PLL, it is required to evaluate application circuit in various condition of loop-gain (loo-p filter, CP current), and to verify with whole conditions of actual application

Example I²C Data Write Sequences

Telegram examples:

Start - ADB - DB1 - DB2 - CB1 – BB - CB2 - Stop
Start - ADB - DB1 - DB2 - Stop
Start - ADB - CB1 - BB - CB2 - Stop
Start - ADB - CB1 - BB - Stop
Start - ADB - CB2 - Stop

Abbreviations:

ADB: Address byte
BB: Bandswitch byte
CB1: Control byte 1
CB2: Control byte 2
DB1: Divider byte 1
DB2: Divider byte 2
Start: Start condition
Stop: Stop condition

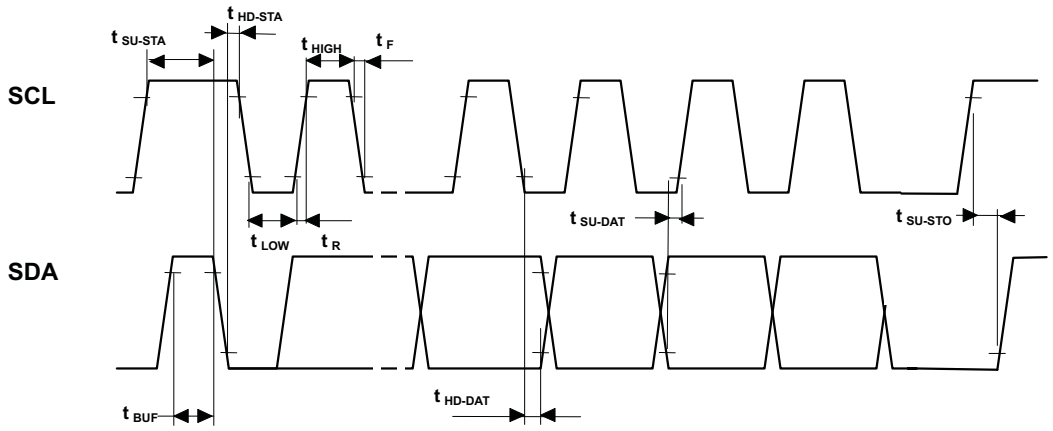
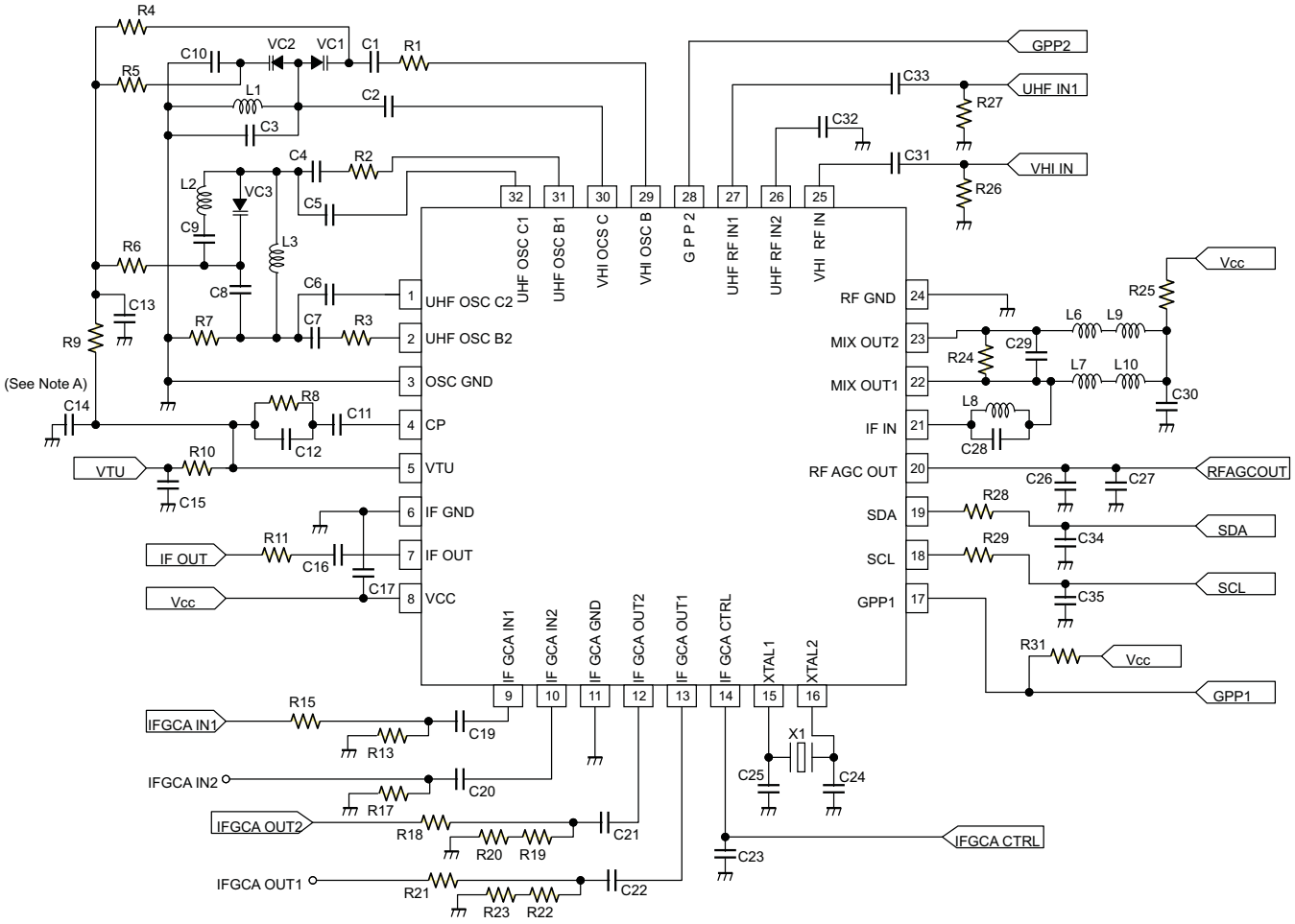


Figure 19. I²C Timing Chart

APPLICATION INFORMATION



A. To prevent abnormal oscillation, connect C14, which does not affect a PLL.

B. This application information is advisory and performance-check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

Figure 20. Reference Measurement Circuit

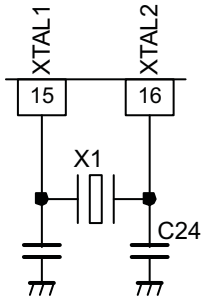
Table 10. Component Values for Measurement Circuit(1)

PARTS NAME	VALUE	PARTS NAME	VALUE
C1 (VHI OSC B)	7 pF	L6 (MIXOUT)	680 nH (LK1608R68K-T)
C2 (VHI OSC C)	5 pF	L7 (MIX OUT)	680 nH (LK1608R68K-T)
C3 (VHI OSC)	0.5 pF	L8 (IF IN)	Short
C4 (UHF OSCB1)	1.5 pF	L9 (MIX OUT)	Short
C5 (UHF OSCC1)	1 pF	L10 (MIXOUT)	Short
C6 (UHF OSCC2)	1 pF	R1 (VHI OSC B)	4.7 Ω
C7 (UHF OSCB2)	1.5 pF	R2 (UHF OSC B1)	7.5 Ω
C8 (UHF OSC)	10 pF	R3 (UHF OSC B2)	7.5 Ω
C9 (UHF OSC)	100 pF	R4 (VHI OSC)	3.3 kΩ
C10 (VHI OSC)	51 pF	R5 (VHI OSC)	3.3 kΩ
C11 (CP)	0.01 µF/50 V	R6 (UHF OSC)	1kΩ
C12 (CP)	22 pF/50 V	R7 (UHF OSC)	2.2 kΩ
C13 (VTU)	2.2 nF	R8 (CP)	47 kΩ
C14 (VTU)	150 pF	R9 (VTU)	3kΩ
C15 (VTU)	2.2 nF/50 V	R10 (VTU)	22 kΩ
C16 (IF OUT)	2.2 nF	R11 (IF OUT)	200 Ω
C17 (VCC)	0.1 µF	R13 (IFGCA IN1)	50 Ω
C19 (IFGCA IN1)	2.2 nF	R15 (IF GCA IN)	0 Ω
C20 (IFGCA IN2)	2.2 nF	R17 (IFGCA IN2)	0 Ω
C21 (IFGCA OUT2)	2.2 nF	R18 (IFGCA OUT2)	200 Ω
C22 (IFGCA OUT1)	2.2 nF	R19 (IFGCA OUT2)	Open
C23 (IFGCA CTRL)	0.1 µF	R20 (IFGCA OUT2)	Open
C24 (XTAL)	15 pF	R21 (IFGCA OUT1)	Open
C25 (XTAL)	15 pF	R22 (IFGCA OUT1)	200 Ω
C26 (RFAGC OUT)	0.1 µF	R23 (IFGCA OUT1)	50 Ω
C27 (RFAGC OUT)	0.047 µF	R24 (MIXOUT)	Open
C28 (IF IN)	Open	R25 (MIXOUT)	0 Ω
C29 (MIXOUT)	6 pF	R26 (VHI IN)	50 Ω
C30 (MIXOUT)	2.2 nF	R27 (UHF RFIN1)	50 Ω
C31 (VHI RF IN)	2.2 nF	R28 (SDA)	330 Ω
C32 (UHF RFIN2)	2.2 nF	R29 (SCL)	330 Ω
C33 (UHF RFIN1)	2.2 nF	R31 (GPP1)	Open
C34 (SDA)	Open	VC1 (VHI OSC)	MA2S372
C35 (SCL)	Open	VC2 (VHI OSC)	MA2S374
L1 (VHI OSC)	φ2.0 mm, 3T, wire 0.4 mm, L	VC3 (UHF OSC)	MA2S372
L2 (UHF OSC)	φ1.8 mm, 3T, wire 0.4 mm, R	X1	8 MHz crystal
L3 (UHF OSC)	φ1.8 mm, 3T, wire 0.4 mm, R		

(1) If frequency = 44 MHz,
local frequency range:
VHF-HIGH: 221–511 MHz
UHF: 517–908 MHz

APPLICATION INFORMATION (CONTINUED)

Reference Crystal Oscillation Circuit



CRYSTAL X1		CAPACITORS	
FREQUENCY	TYPE	C24	C25
4 MHz	HC49SFNB04000H0 (Kyocera)	27 pF	27 pF
8 MHz	CX5032GB08000H0 (Kyocera)	15 pF	15 pF
16 MHz	CX3225GB16000D0 (Kyocera)	14 pF	14 pF

Figure 21. Reference Crystal Oscillation Circuit

Test Circuits

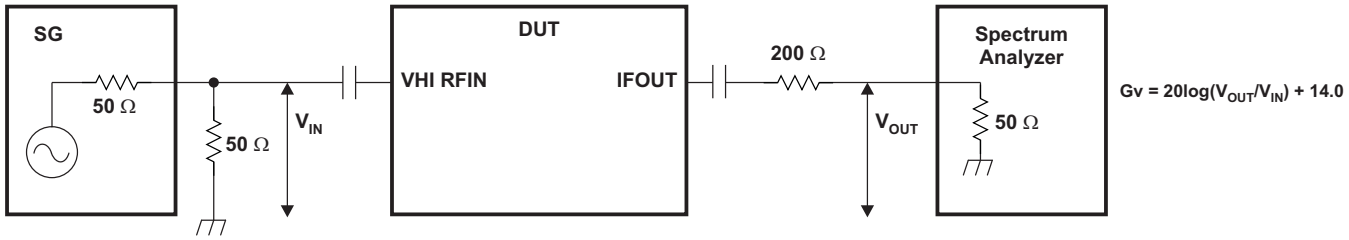


Figure 22. Conversion Gain Measurement Circuit

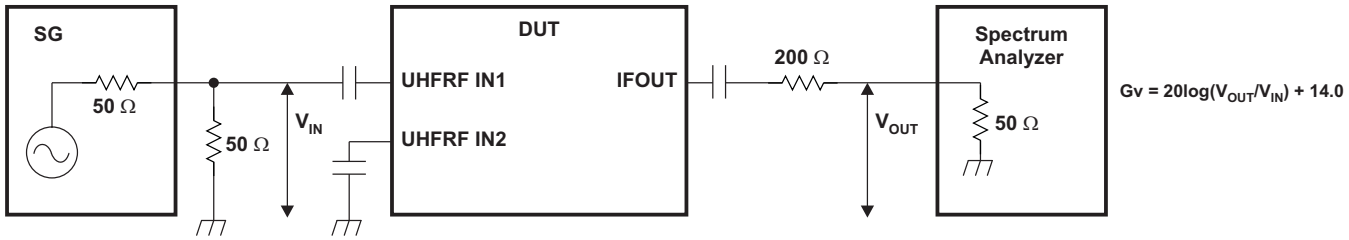


Figure 23. UHF Conversion Gain Measurement Circuit

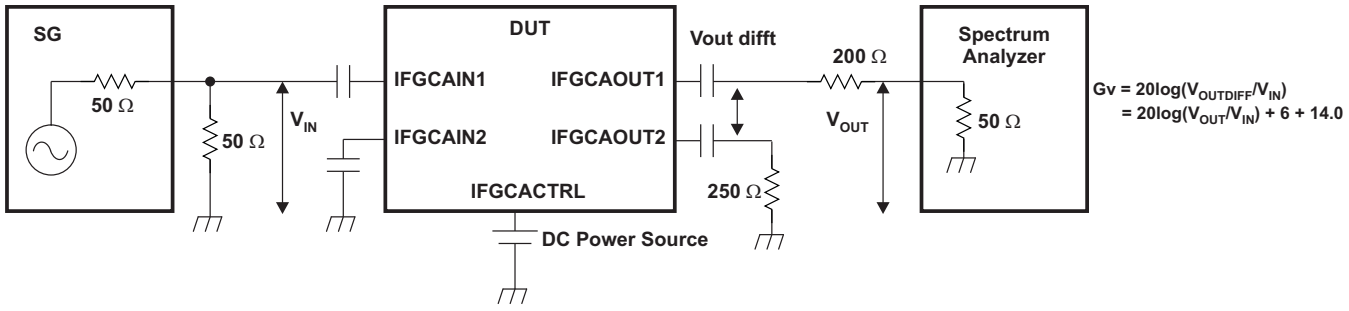


Figure 24. IF GCA Gain Measurement Circuit

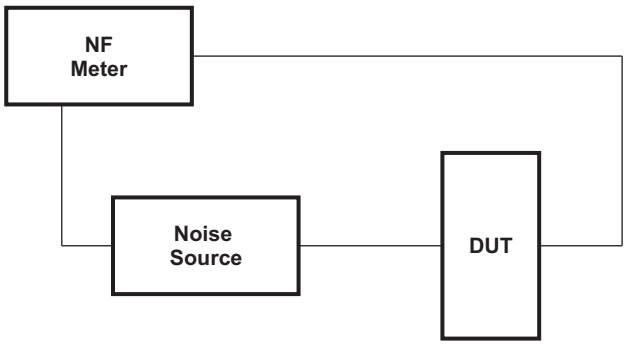


Figure 25. Noise Figure Measurement Circuit

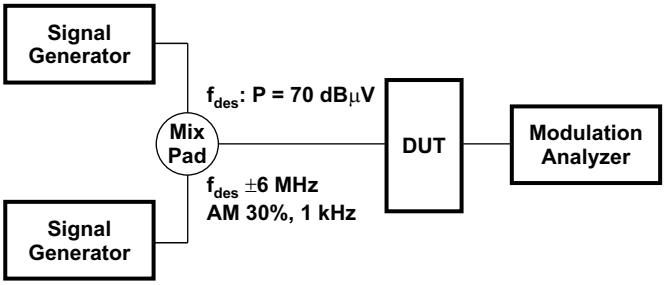


Figure 26. 1% Cross-Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

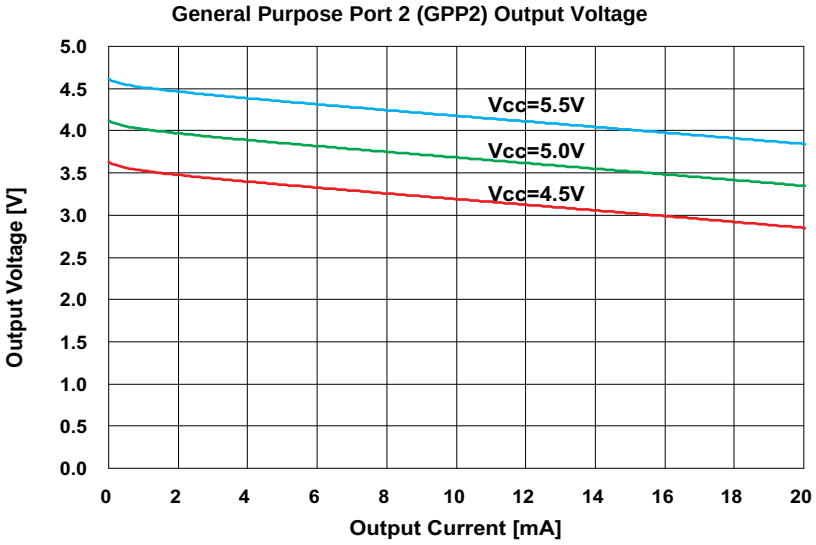


Figure 27. GPP2 Output Current vs Output Voltage

TYPICAL CHARACTERISTICS (continued)

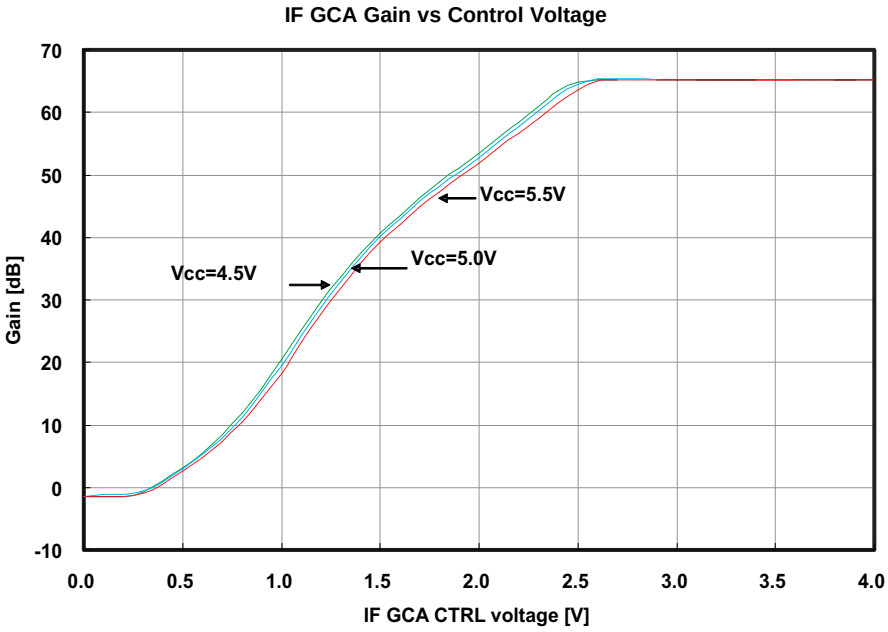


Figure 28. IF GCA Gain vs Control Voltage

S-Parameter

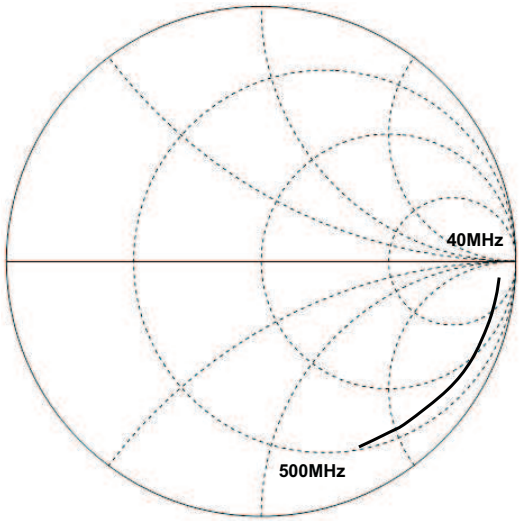


Figure 29. VHI RFIN

TYPICAL CHARACTERISTICS (continued)

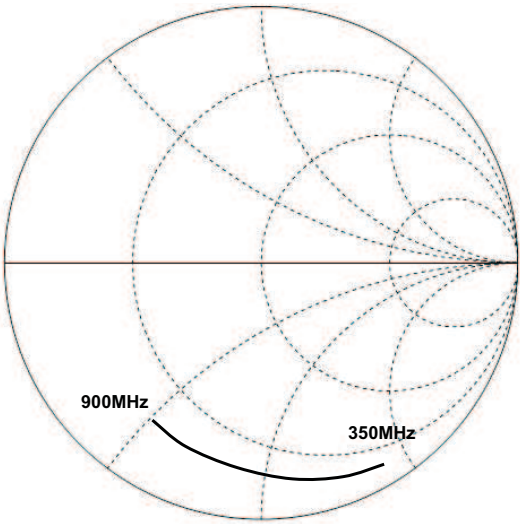


Figure 30. UHF RFIN

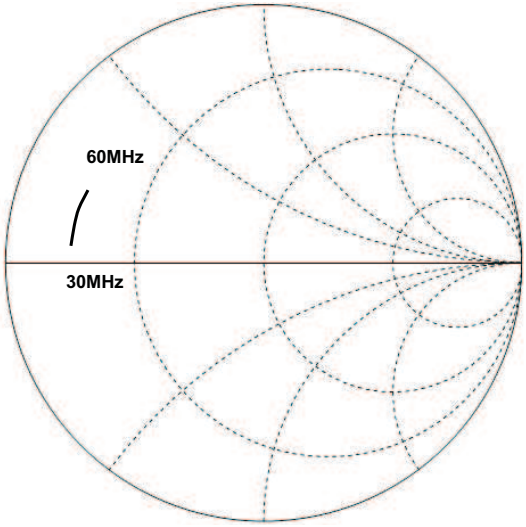


Figure 31. IFOUT

TYPICAL CHARACTERISTICS (continued)

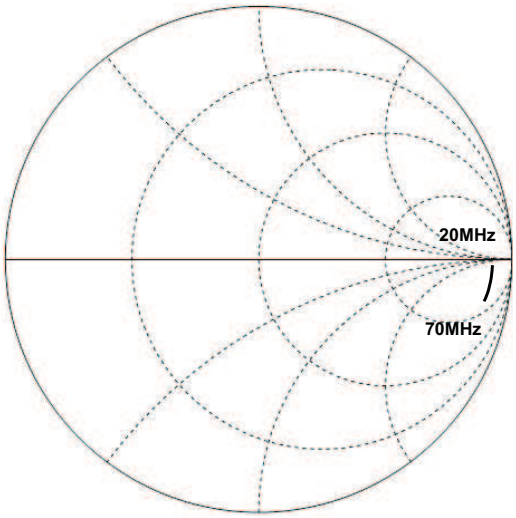


Figure 32. IF GCA IN

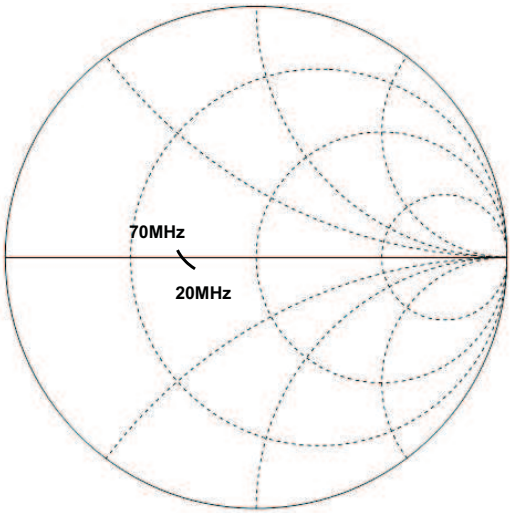


Figure 33. IF GCA OUT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN761646RHBR	OBSOLETE	VQFN	RHB	32		TBD	Call TI	Call TI	-20 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

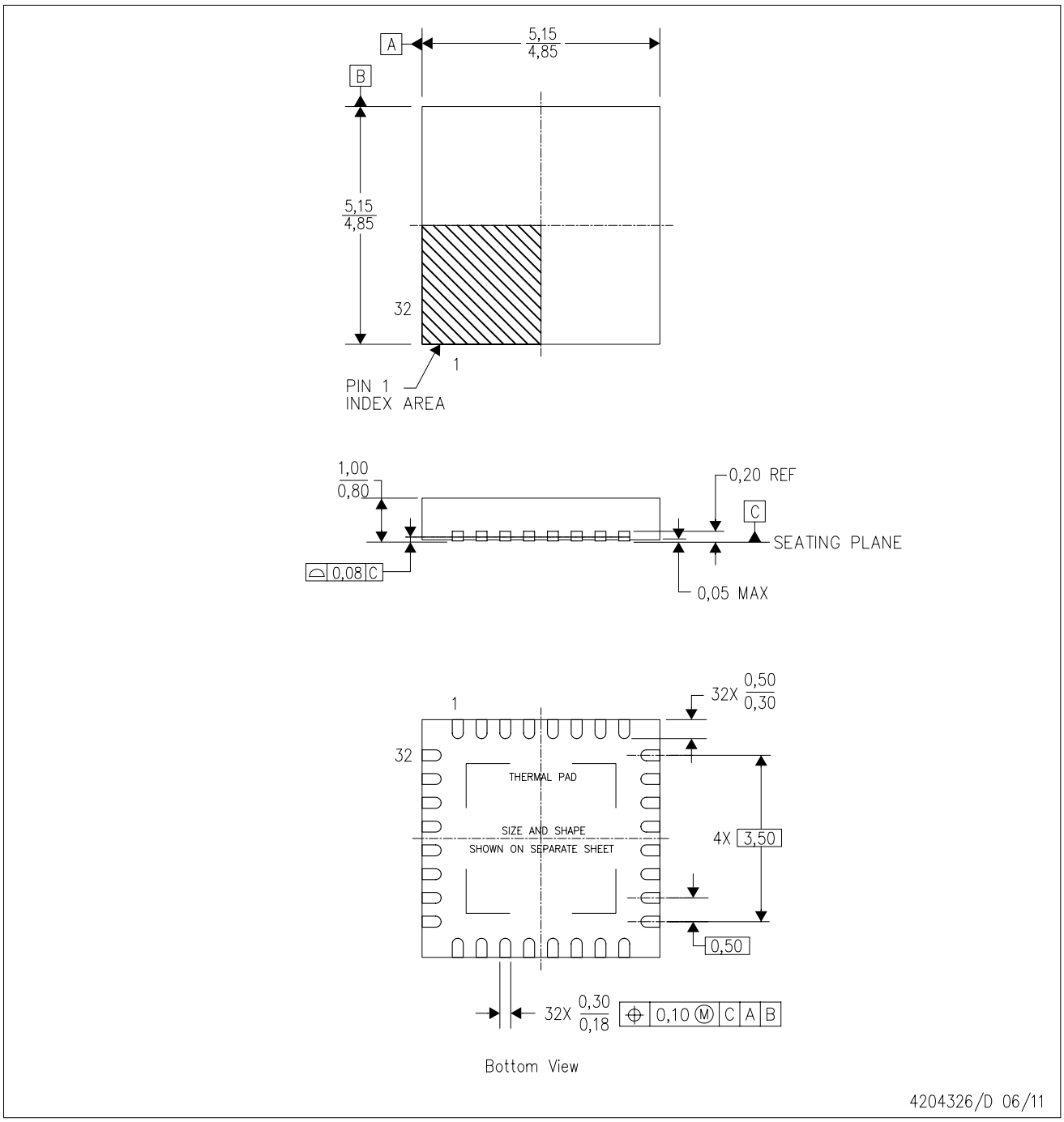
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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