KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Schematics

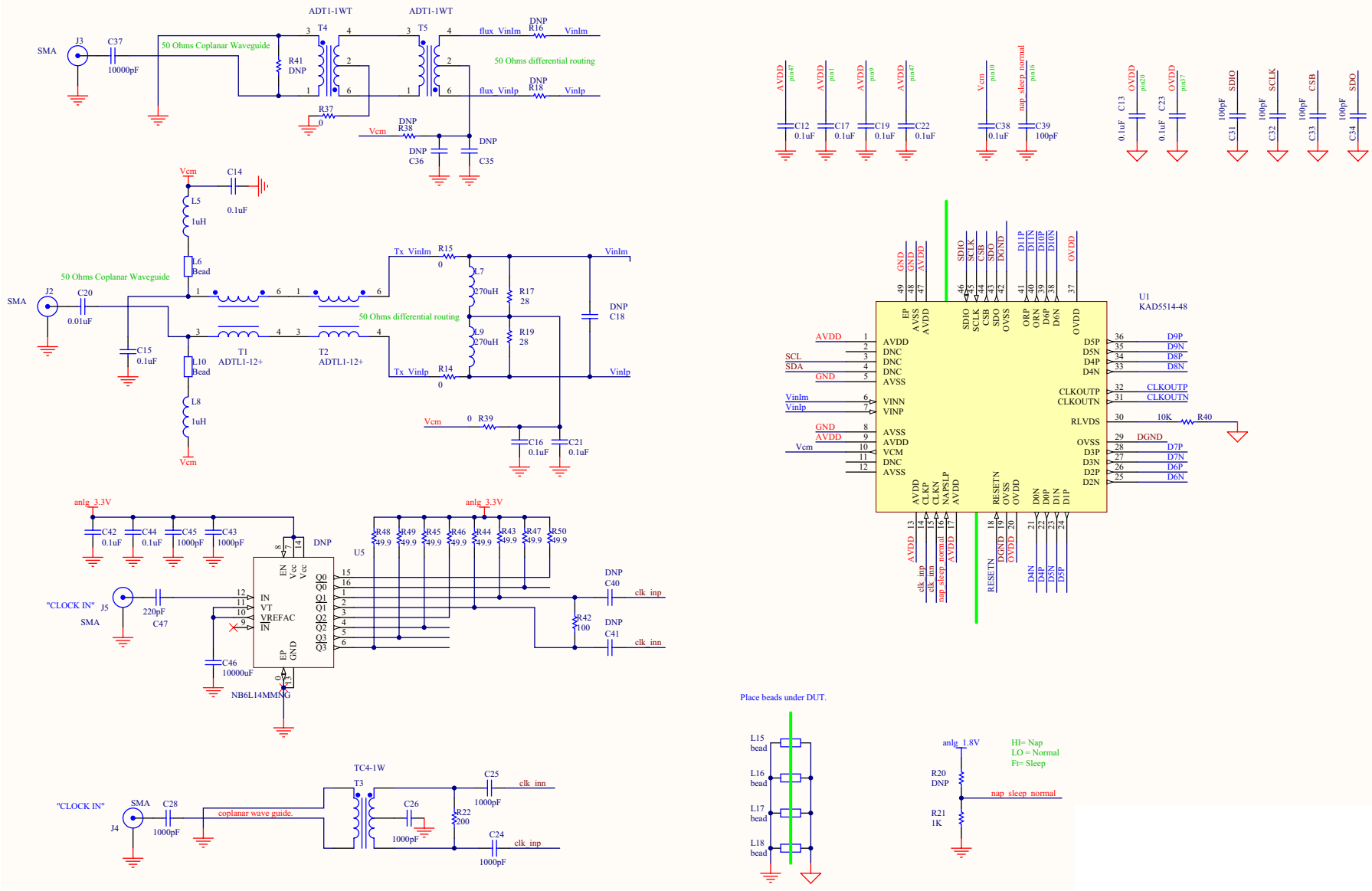

FIGURE 1. ADC, CLOCK AND ANALOG INPUTS, MODE PINS AND POWER SUPPLY BYPASS

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Schematics (Continued)

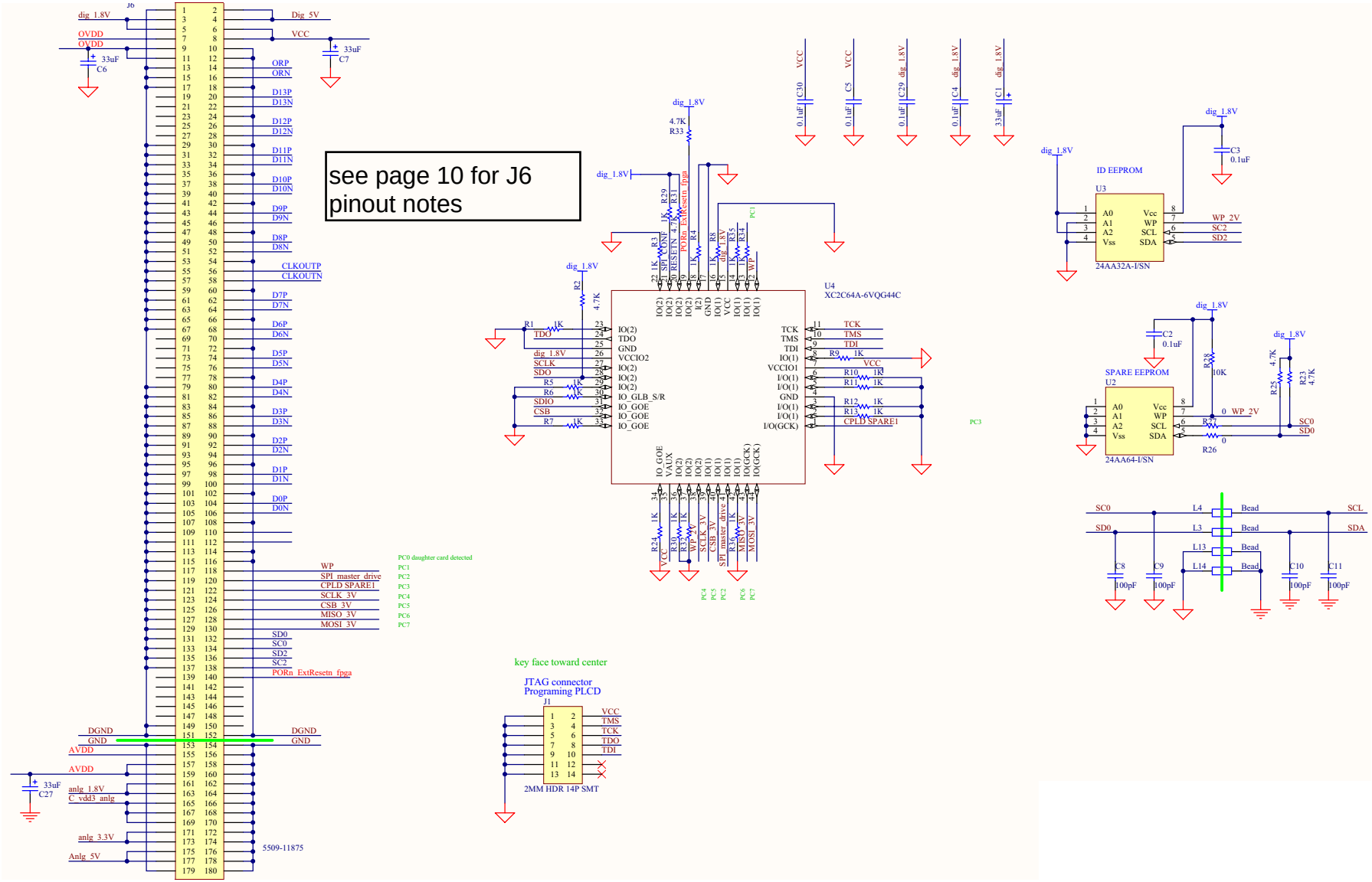

FIGURE 2. INPUT/OUTPUT MEZZANINE CONNECTOR

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers

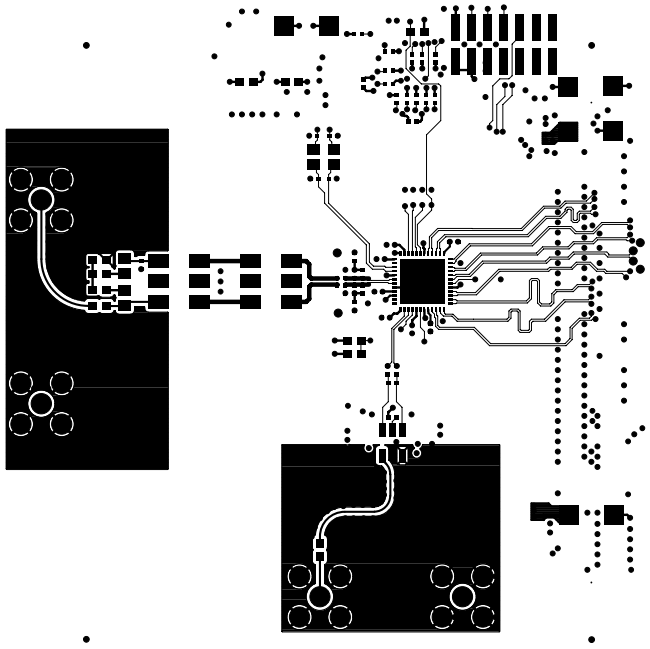

FIGURE 3. PRIMARY SIDE

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

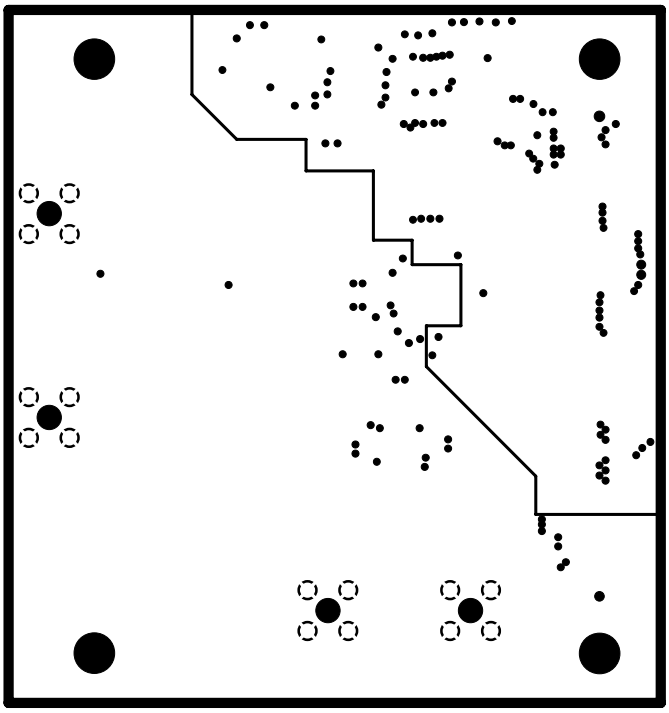

FIGURE 4. GND PLANE 1

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

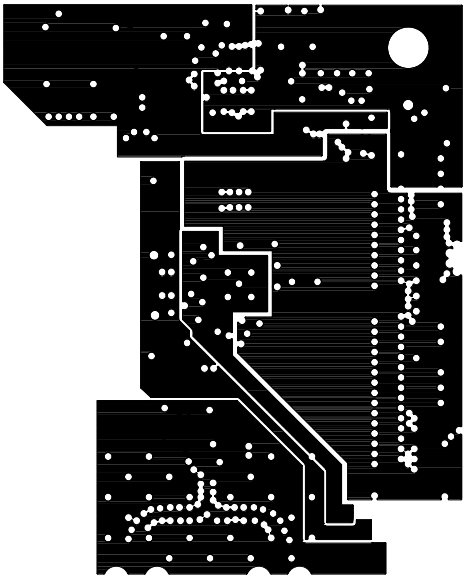

FIGURE 5. PWR PLANE

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

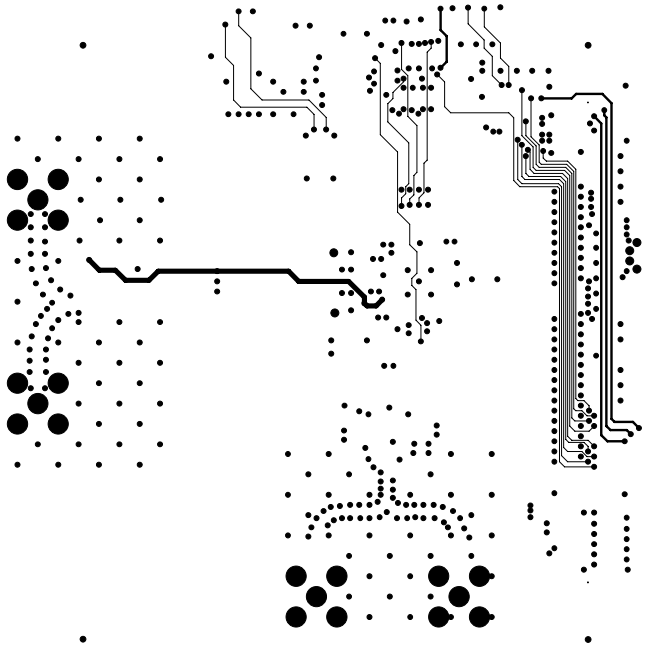

FIGURE 6. INTERNAL SIGNAL

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

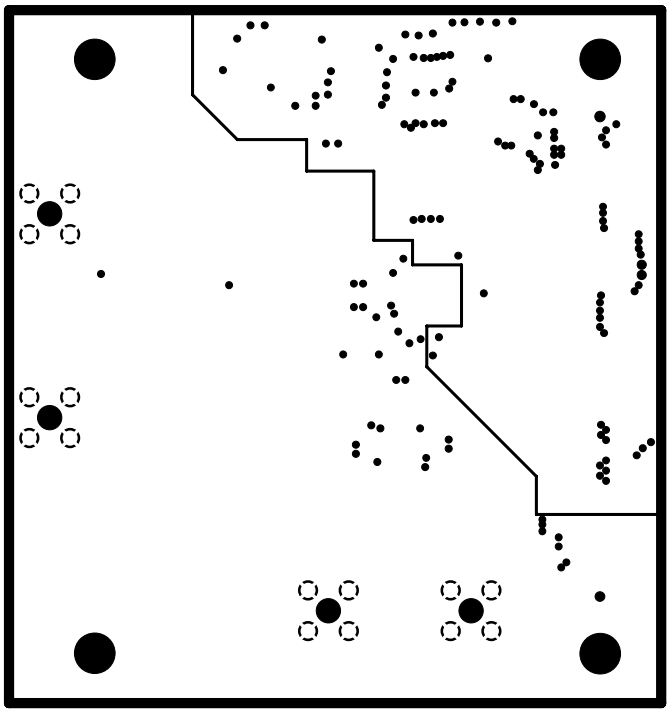

FIGURE 7. GND PLANE 2

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

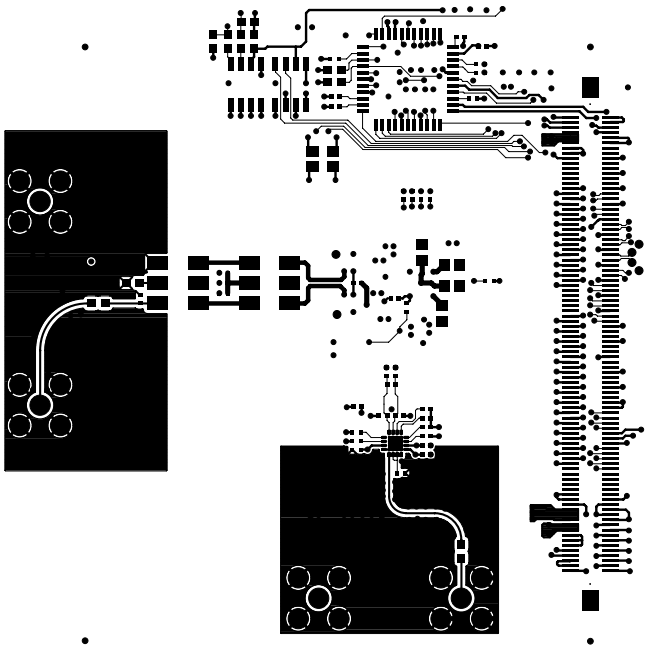

FIGURE 8. SECONDARY SIDE

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

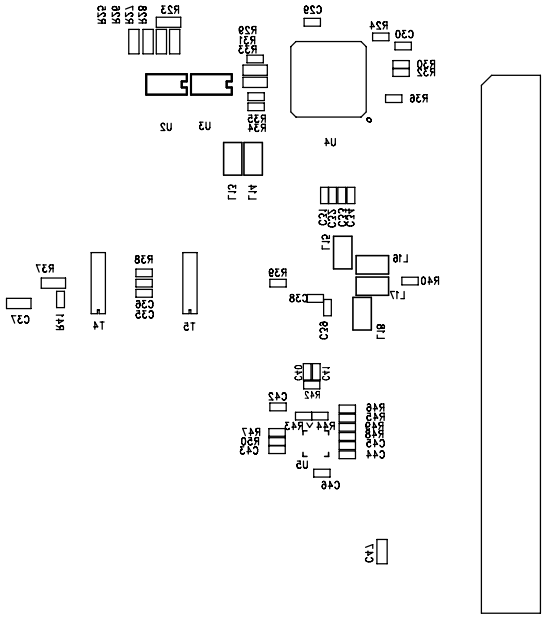

FIGURE 9. SECONDARY SIDE SILKSCREEN

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL Layers (Continued)

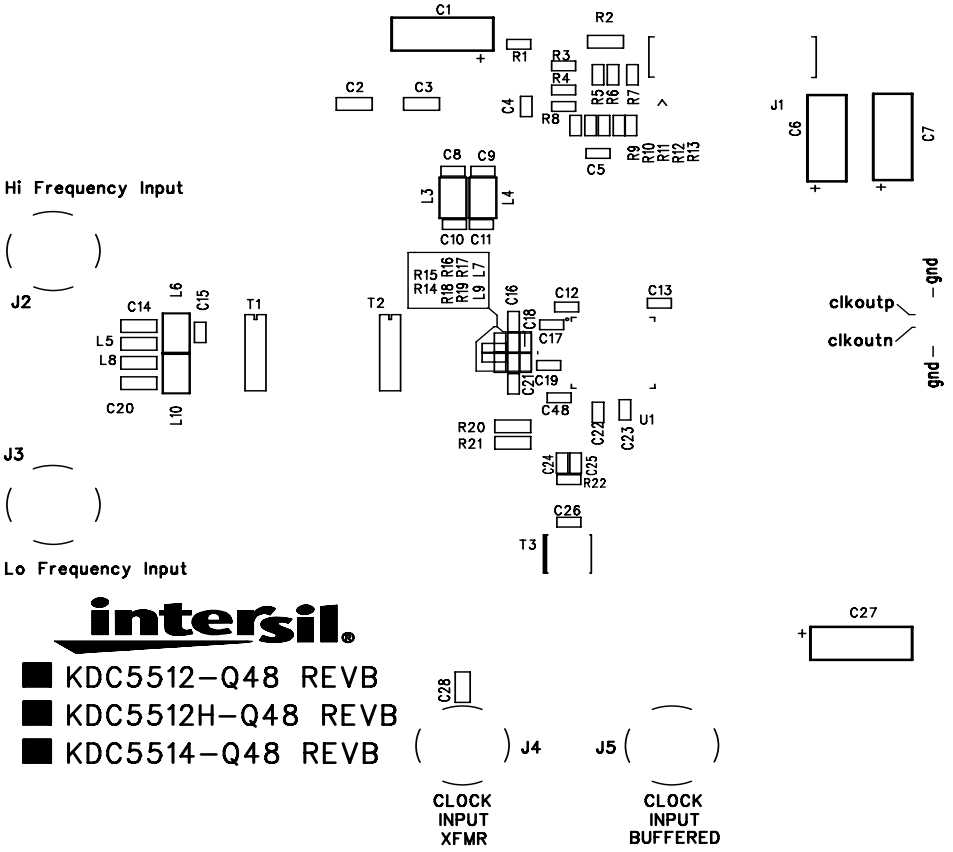

FIGURE 10. LAYER - PRIMARY SIDE SILKSCREEN

J6 pinout is shown for 14bit device. ADC Output Data pins are MSB justified at J6. Pins 38,40 at J6 are ADC signals D6P,D6N for 14 bit device. Pins 38,40 at J6 are ADC signals D5P,D5N for 12 bit device. Contact factory for additional information if needed.