Low Noise, Low Power I^2C® Bus, 256 Taps

The ISL90840 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. When powered on the ISL90810's wiper will always commence at mid-scale (128 tap position).

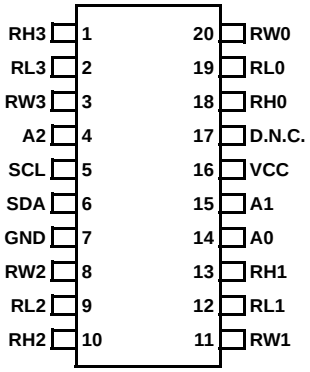
The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Four potentiometers in one package
- 256 resistor taps - 0.4% resolution
- I^2C serial interface
  - Three address pins, up to eight devices/bus
  - Write/Read capability
- Power-on preset to mid-scale (128 tap position)
- Wiper resistance: 70Ω typical @ 3.3V
- Standby current <5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ, 10kΩ total resistance
- 20 Ld TSSOP package
- Pb-free plus anneal available (RoHS compliant)

Pinout

ISL90840
(20 LD TSSOP)
TOP VIEW



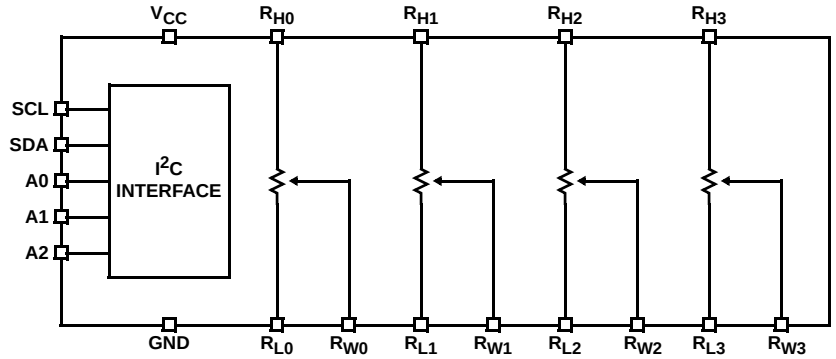
Ordering Information

PART NUMBER	PART MARKING	RESIST-ANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE	PKG. DWG #
ISL90840UIV2027Z (Notes 1 and 2)	ISL90840UI27Z	50k	-40 to +85	20 Ld TSSOP (Pb-free)	MDP0044
ISL90840UIV2027	ISL90840UI27	50k	-40 to +85	20 Ld TSSOP	MDP0044
ISL90840UAV2027Z (Notes 1 and 2)	ISL90840UA27Z	50k	-40 to +105	20 Ld TSSOP (Pb-free)	MDP0044
ISL90840WIV2027Z (Notes 1 and 2)	ISL90840WI27Z	10k	-40 to +85	20 Ld TSSOP (Pb-free)	MDP0044
ISL90840WIV2027	ISL90840WI27	10k	-40 to +85	20 Ld TSSOP	MDP0044
ISL90840WAV2027Z (Notes 1 and 2)	ISL90840WA27Z	10k	-40 to +105	20 Ld TSSOP (Pb-free)	MDP0044

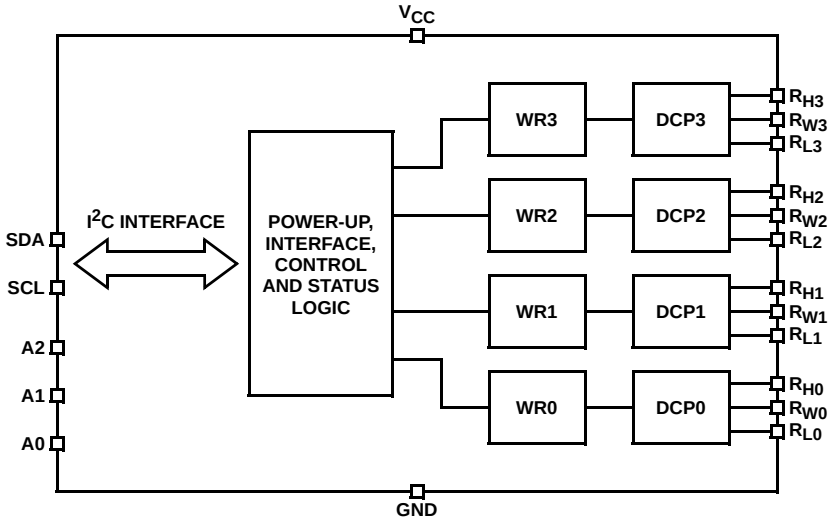
NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "T2" suffix for tape and reel.

Functional Diagram



Block Diagram



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	RH3	“High” terminal of DCP3
2	RL3	“Low” terminal of DCP3
3	RW3	“Wiper” terminal of DCP3
4	A2	Device address for the I^2C interface
5	SCL	I^2C interface clock
6	SDA	Serial data I/O for the I^2C interface
7	GND	Device ground pin
8	RW2	“Wiper” terminal of DCP2
9	RL2	“Low” terminal of DCP2
10	RH2	“High” terminal of DCP2
11	RW1	“Wiper” terminal of DCP1
12	RL1	“Low” terminal of DCP1
13	RH1	“High” terminal of DCP1
14	A0	Device address for the I^2C interface
15	A1	Device address for the I^2C interface
16	VCC	Power supply pin
17	D.N.C.	Do not connect
18	RH0	“High” terminal of DCP0
19	RL0	“Low” terminal of DCP0
20	RW0	“Wiper” terminal of DCP0

Typical Performance Curves (Continued)

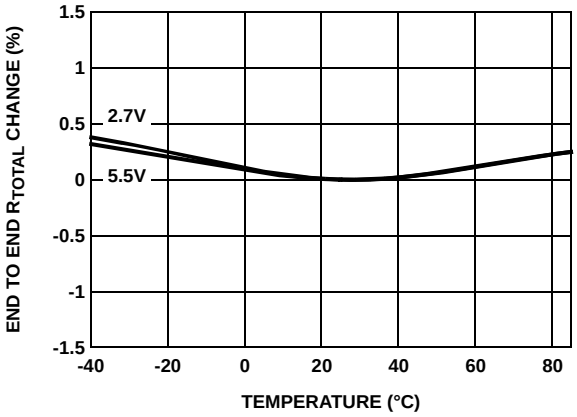


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE FOR 50kΩ (W)

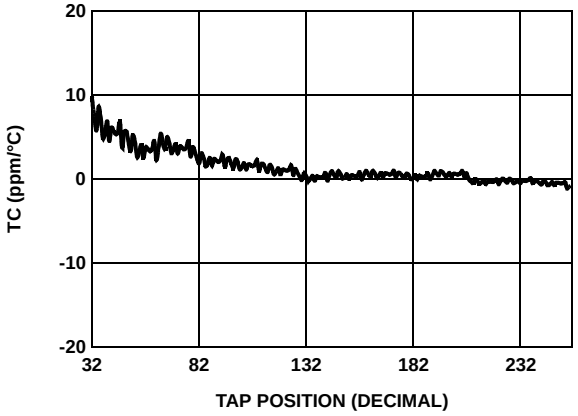


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm FOR 50kΩ (W)

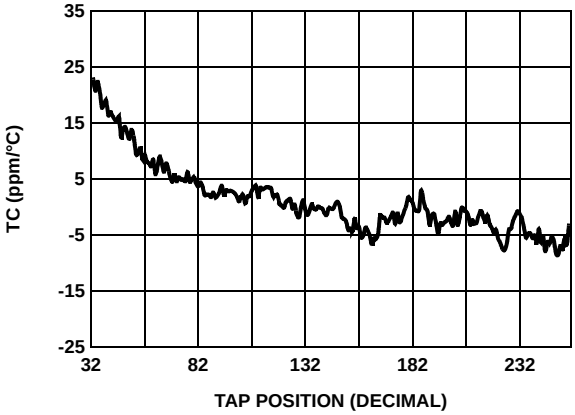


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm FOR 50kΩ (W)

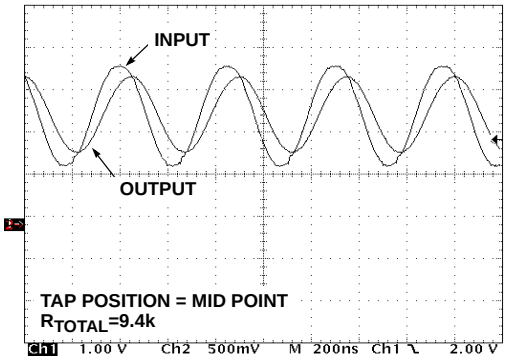


FIGURE 12. FREQUENCY RESPONSE (2.2MHz)

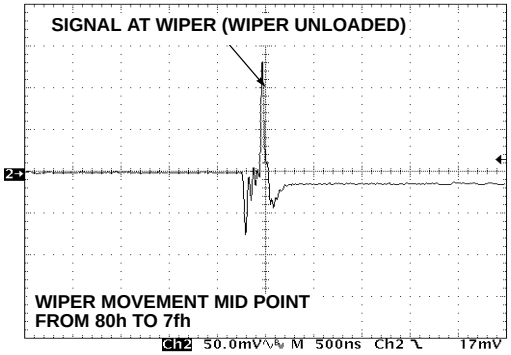


FIGURE 13. MIDSCALE GLITCH, CODE 80h TO 7Fh (WIPER 0)

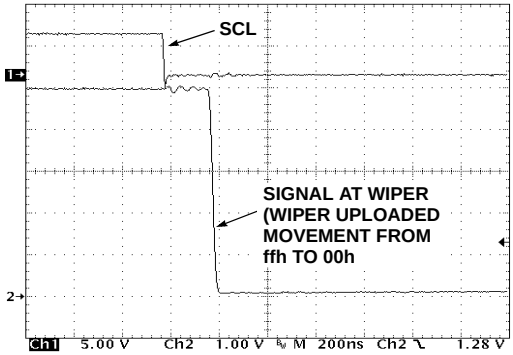
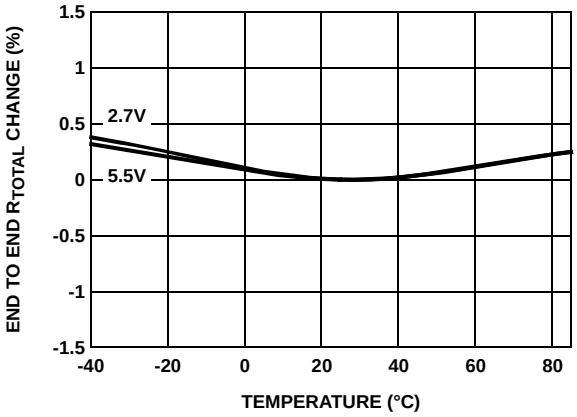


FIGURE 14. LARGE SIGNAL SETTLING TIME

Typical Performance Curves (Continued)



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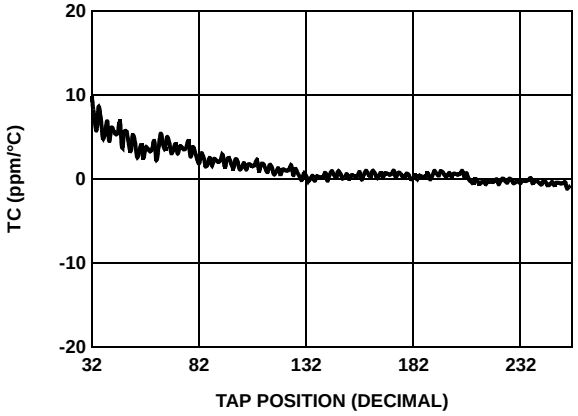

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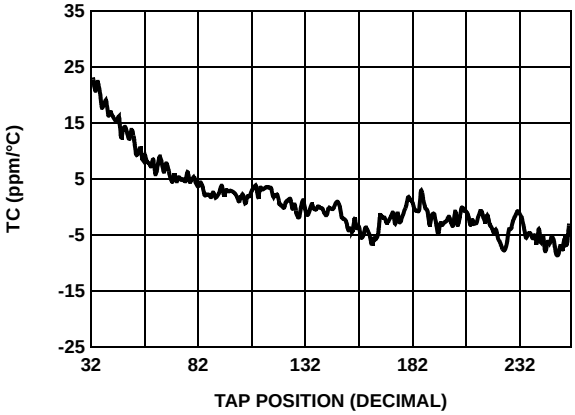

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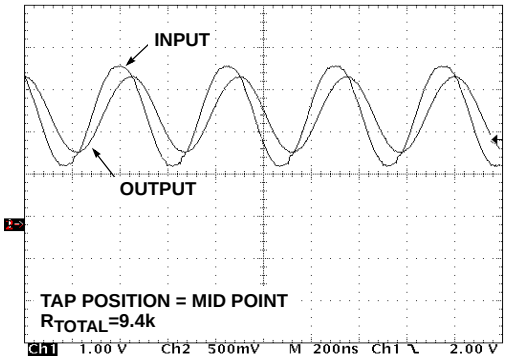

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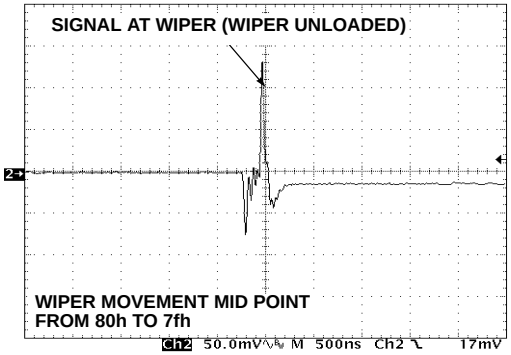

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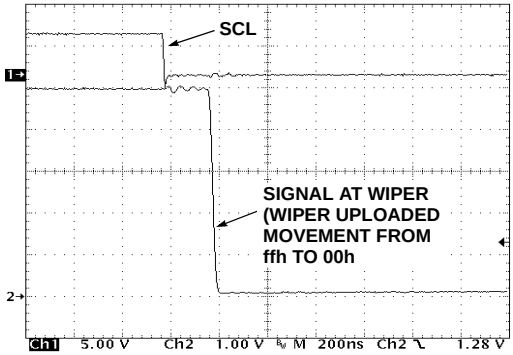

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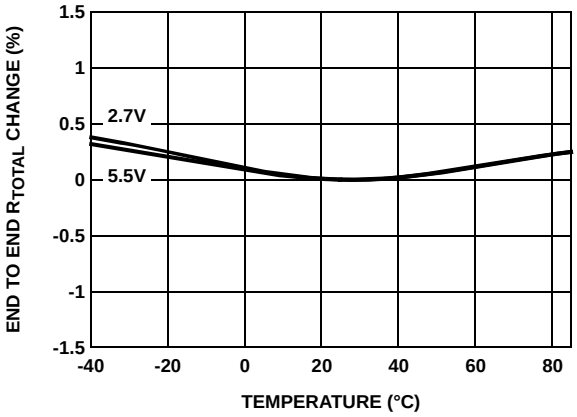

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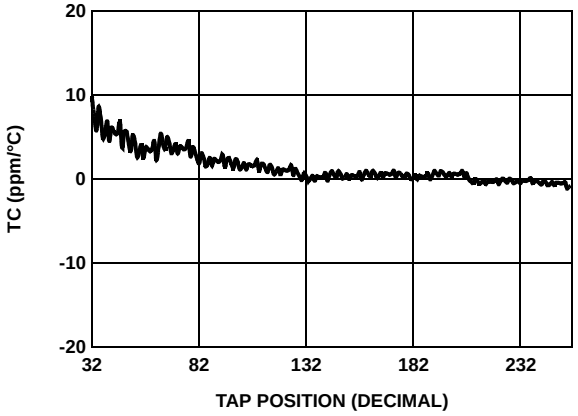

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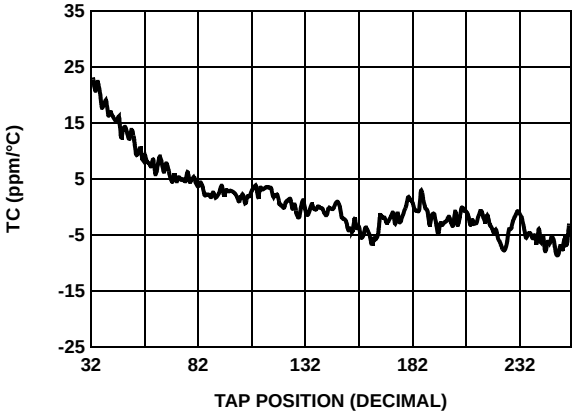

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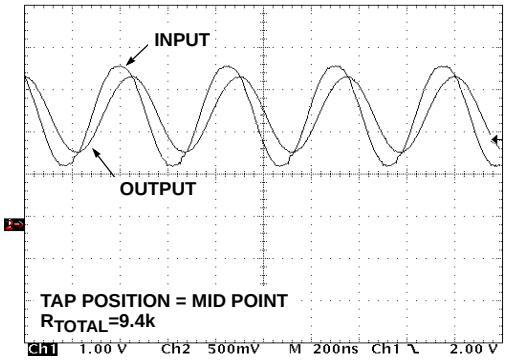

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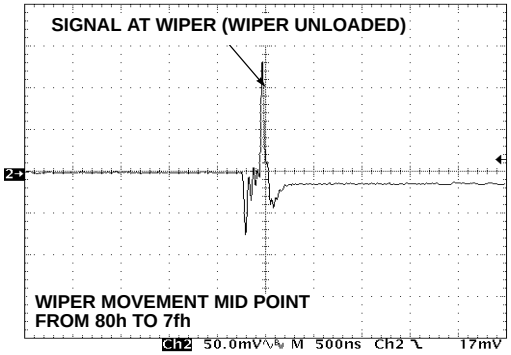

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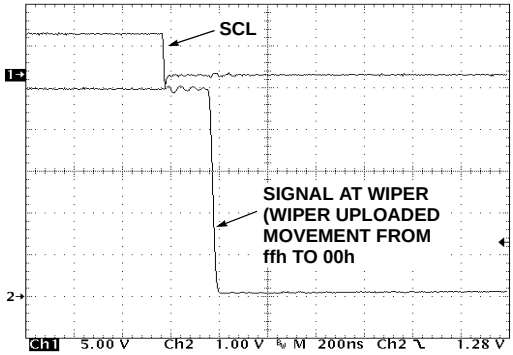

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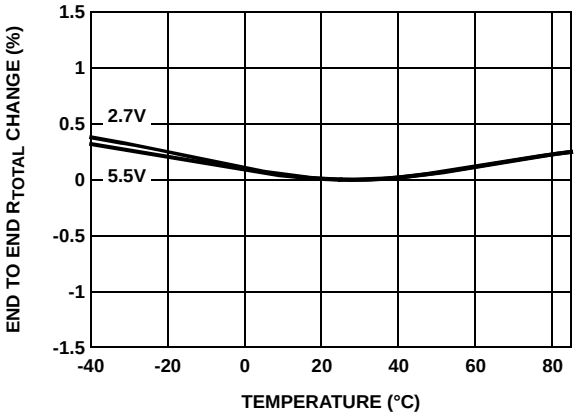
Typical Performance Curves (Continued)



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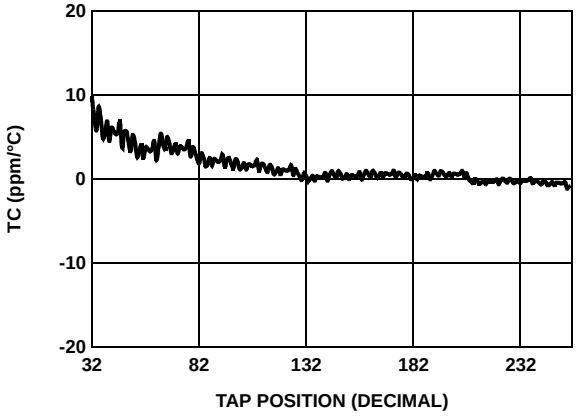

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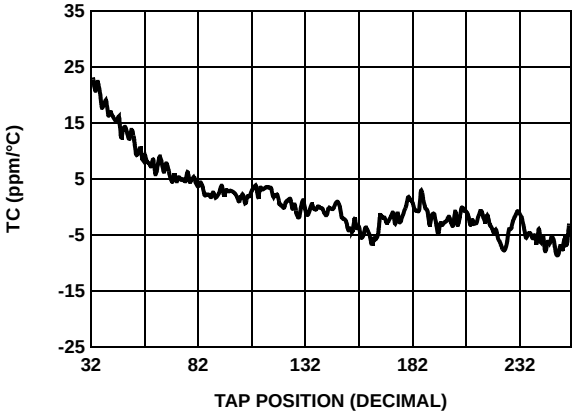

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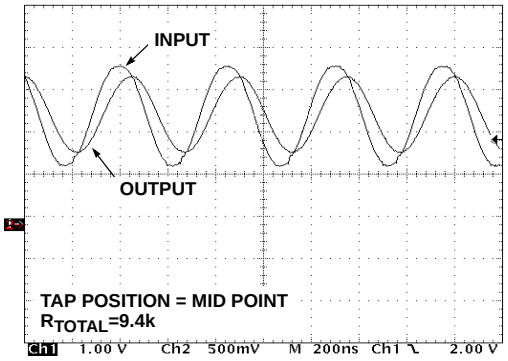

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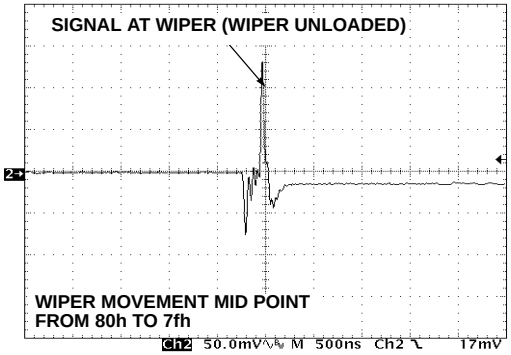

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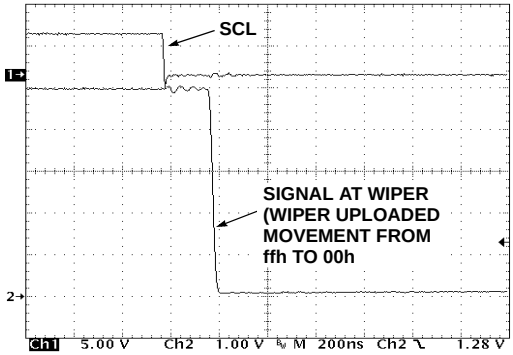

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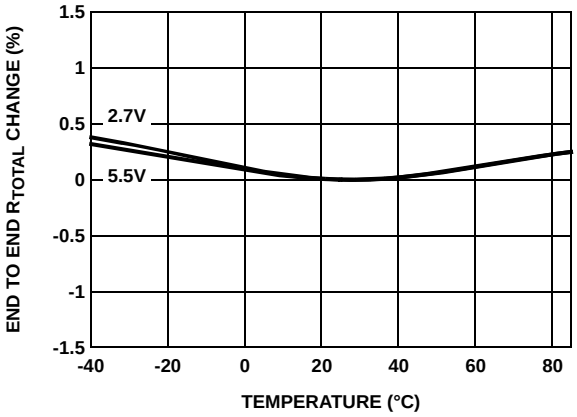

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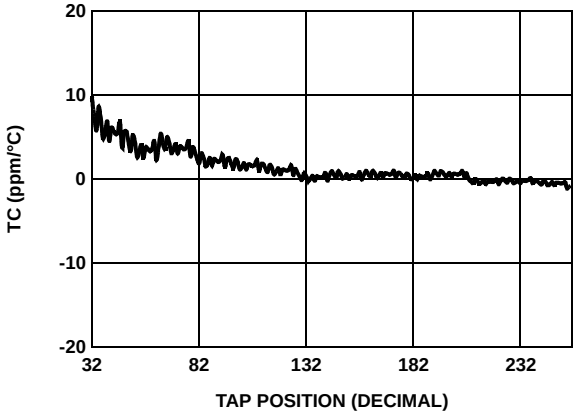

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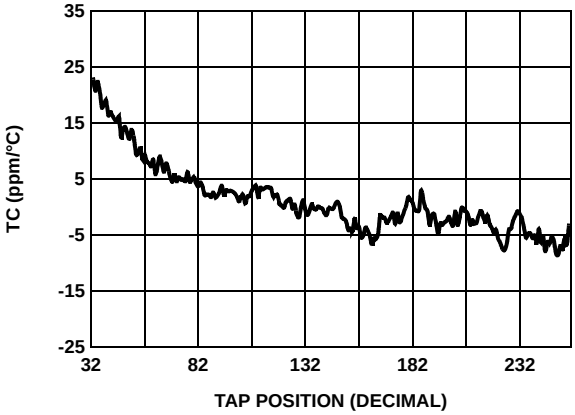

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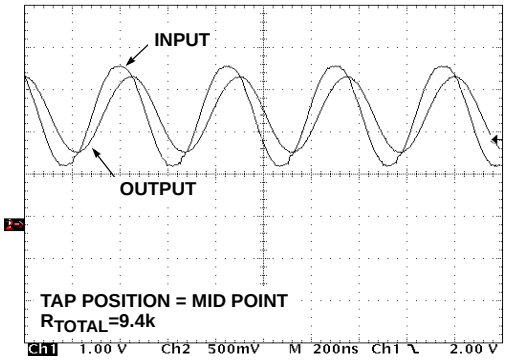

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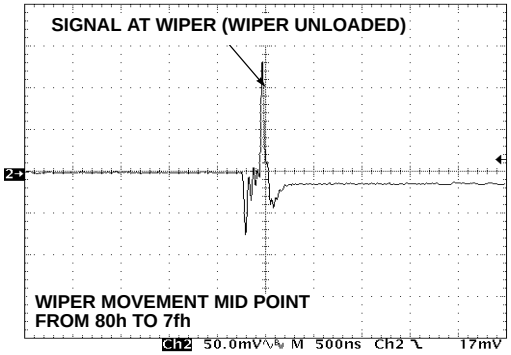

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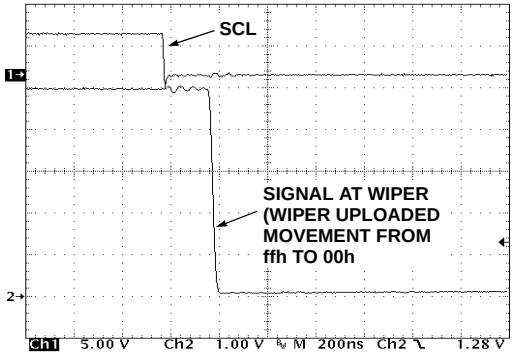


FIGURE 14. LARGE SIGNAL SETTLING TIME

Principles of Operation

The ISL90840 is an integrated circuit incorporating four DCPs with their associated registers, and an I^2C serial interface providing direct communication between a host and the potentiometers.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR[7:0]: 00h), its wiper terminal (R_W) is closest to its “Low” terminal (R_L). When the WR of a DCP contains all ones (WR[7:0]: FFh), its wiper terminal (R_W) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (0 decimal) to all ones (255 decimal), the wiper moves monotonically from the position closest to R_L to the closest to R_H. At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically.

While the ISL90840 is being powered up, all four WRs are reset to 80h (128 decimal), which locates R_W roughly at the center between R_L and R_H.

The WRs can be read or written to directly using the I^2C serial interface as described in the following sections. The I^2C interface Address Byte has to be set to 00h, 01h, 02h, and 03h to access the WR of DCP0, DCP1, DCP2, and DCP3 respectively

I^2C Serial Interface

The ISL90840 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL90840 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 15). On power-up of the ISL90840 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL90840 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 15). A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 15). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 16).

The ISL90840 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL90840 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 0101 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 1).

TABLE 1. IDENTIFICATION BYTE FORMAT

				Logic values at pins A2, A1, and A0 respectively			
0	1	0	1	A2	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

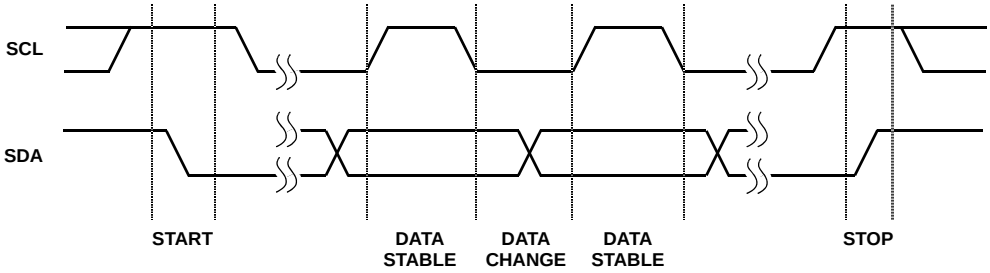


FIGURE 15. VALID DATA CHANGES, START, AND STOP CONDITIONS

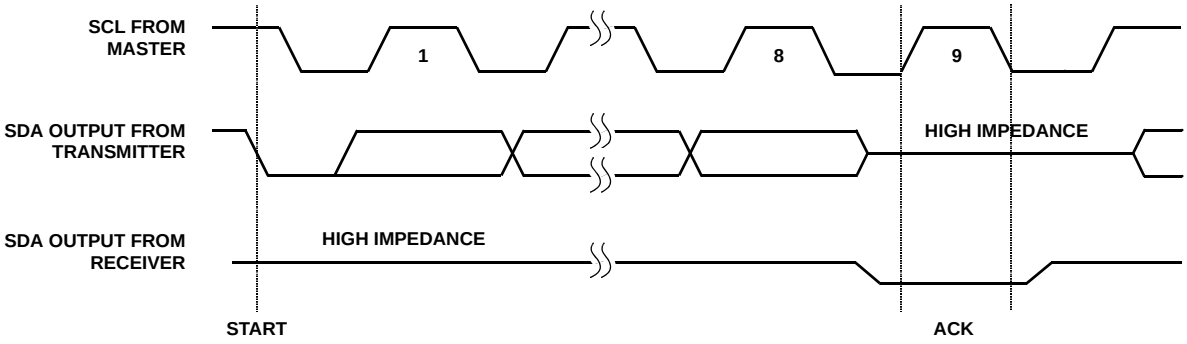


FIGURE 16. ACKNOWLEDGE RESPONSE FROM RECEIVER

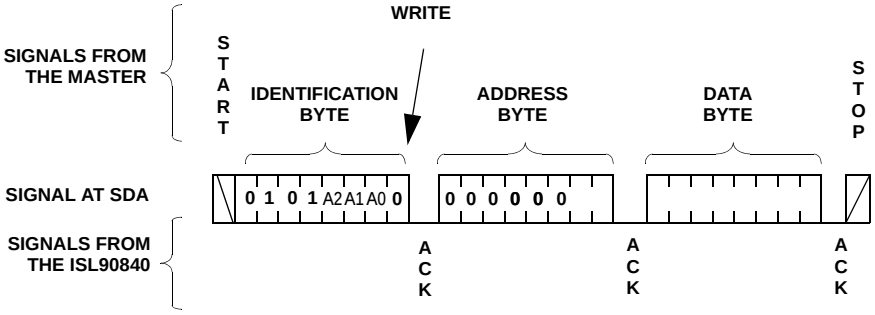


FIGURE 17. BYTE WRITE SEQUENCE

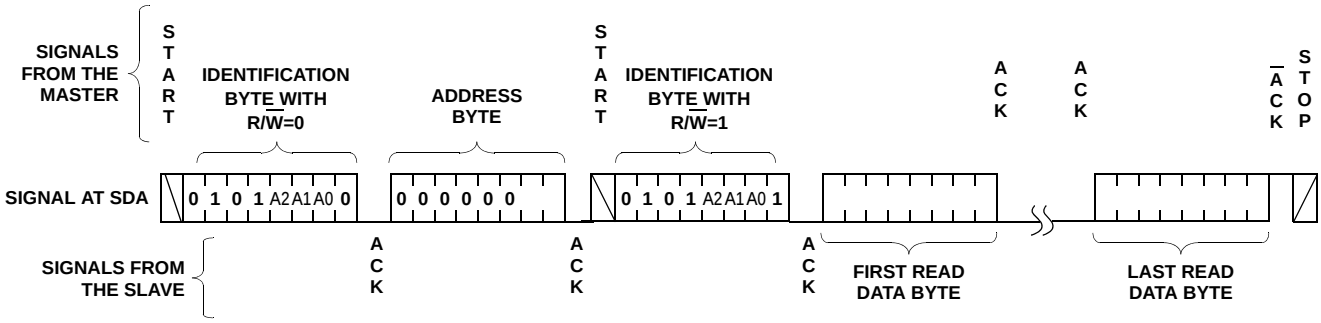


FIGURE 18. READ SEQUENCE

Write Operation

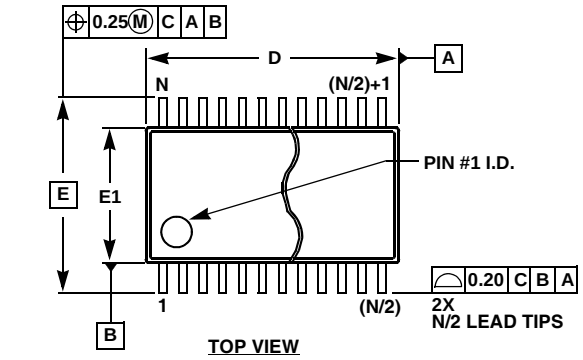
A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL90840 responds with an ACK. At this time, the device enters its standby state (See Figure 17).

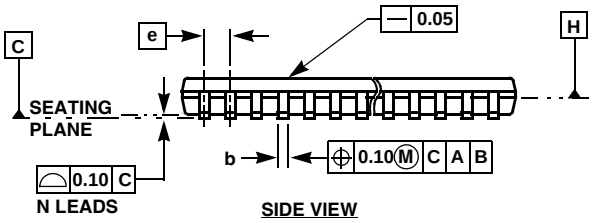
Read Operation

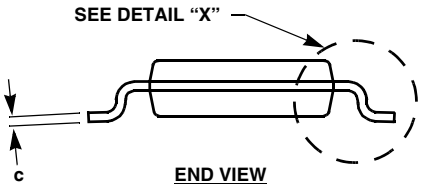
A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL90840 responds with an ACK. Then the ISL90840 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a $\overline{\text{ACK}}$ and STOP condition) following the last bit of the last Data Byte (See Figure 18).

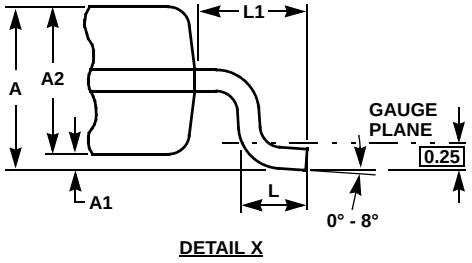
The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 03h, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	14 LD	16 LD	20 LD	24 LD	28 LD	TOLERANCE
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. E 12/02

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.