Data Sheet | August 2004 | FN6042.2

## Low-Voltage, Single Supply, 4 to 1 Multiplexer and DPDT Analog Switches

The Intersil ISL84524 and ISL84525 devices are precision, bidirectional, analog switches configured as a 4 channel multiplexer / demultiplexer (ISL84524) and a double pole / double throw (DPDT) switch (ISL84525) designed to operate from a single +2V to +12V supply. Both have an inhibit pin to simultaneously open all signal paths.

ON resistance is 200Ω with a +5V supply and 500Ω with a +3V supply. Each switch can handle rail to rail analog signals. The off-leakage current is only 1nA at +25°C or 25nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single +5V supply.

The ISL84524 is a 4 to 1 multiplexer device. The ISL84525 is a DPDT, which is perfect for use in 2-to-1 multiplexer applications.

Table 1 summarizes the performance of this family. For higher performance, see the ISL43640 and ISL43410 data sheets.

**TABLE 1. FEATURES AT A GLANCE**

| $R_{ON}$ & $t_{ON}$ / $t_{OFF}$ | ISL84524 4:1 MUX | ISL84525 DPDT |
|---|---|---|
| **3V $R_{ON}$** | 190Ω | 190Ω |
| **3V $t_{ON}$ / $t_{OFF}$** | 170ns / 50ns | 170ns / 50ns |
| **5V $R_{ON}$** | 92Ω | 92Ω |
| **5V $t_{ON}$ / $t_{OFF}$** | 90ns / 40ns | 90ns / 40ns |
| **PACKAGE** | 10 Ld MSOP | |

## Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

## Features

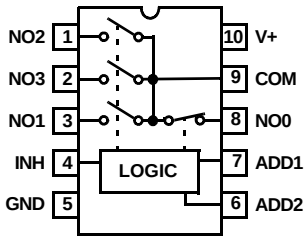
- Drop-in Replacements for MAX4524 and MAX4525
- ON Resistance ($R_{ON}$) Max, $V_S$ = 5V . . . . . 200Ω
- ON Resistance ($R_{ON}$) Max, $V_S$ = 3V . . . . . 500Ω
- $R_{ON}$ Matching Between Channels. . . . . <8Ω
- Low Charge Injection . . . . . 5pC (Max)
- Single Supply Operation. . . . . +2V to +12V
- Low Power Consumption ($P_D$) . . . . . <3µW
- Fast Switching Action ($V_S$ = 5V)
  - $t_{ON}$ . . . . . 90ns
  - $t_{OFF}$ . . . . . 40ns
- Guaranteed Max Off-leakage @ 5V . . . . . 25nA
- Guaranteed Break-Before-Make
- TTL, CMOS Compatible
- Available in 10 Ld MSOP Package
- Pb-free available

## Applications

- Battery Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

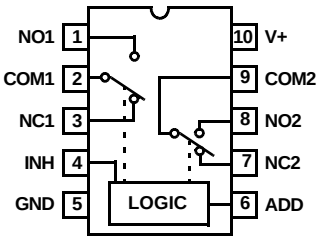
## Pinouts (Note 1)

**ISL84524 (MSOP)**
TOP VIEW




**4:1 MUX**

**ISL84525 (MSOP)**
TOP VIEW




**DPDT**

NOTE:

1. Switches Shown for Logic “0” Inputs.

## Truth Tables

| ISL84524 | | | |
|---|---|---|---|
| **INH** | **ADD2** | **ADD1** | **SWITCH ON** |
| 1 | X | X | NONE |
| 0 | 0 | 0 | NO0 |
| 0 | 0 | 1 | NO1 |
| 0 | 1 | 0 | NO2 |
| 0 | 1 | 1 | NO3 |
| **ISL84525** | | | |
| **INH** | **ADD** | | **SWITCH ON** |
| 1 | X | | NONE |
| 0 | 0 | | NCX |
| 0 | 1 | | NOX |

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V, with $V_S$ between 3V and 11V.

## Pin Descriptions

| PIN | FUNCTION |
|---|---|
| V+ | System Power Supply Input (+2V to +12V) |
| GND | Ground Connection |
| INH | Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off. |
| COM | Analog Switch Common Pin |
| NOX | Analog Switch Normally Open Pin |
| NCX | Analog Switch Normally Closed Pin |
| ADDX | Address Input Pin |

## Ordering Information

| PART NO. (BRAND) | TEMP. RANGE ($^{o}$C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL84524IU (524I) | -40 to 85 | 10 Ld MSOP | M10.118 |
| ISL84524IUZ (524I) (Note) | -40 to 85 | 10 Ld MSOP (Pb-free) | M10.118 |
| ISL84525IU (525I) | -40 to 85 | 10 Ld MSOP | M10.118 |
| ISL84525IUZ (525I) (Note) | -40 to 85 | 10 Ld MSOP (Pb-free) | M10.118 |

*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

## Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to15V
Input Voltages
INH, NO, NC, ADD (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . . 20mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . 40mA

## Operating Conditions

Temperature Range
ISL8452XIU . . . . . -40$^{o}$C to 85$^{o}$C

## Thermal Information

Thermal Resistance (Typical, Note 3) $\theta_{JA}$ ($^{o}$C/W)
10 Ld MSOP Package . . . . . 190
Maximum Junction Temperature (Plastic Package) . . . . . 150$^{o}$C
Moisture Sensitivity (See Technical Brief TB363)
10 Ld MSOP Package . . . . . Level 1
Maximum Storage Temperature Range . . . . . -65$^{o}$C to 150$^{o}$C
Maximum Lead Temperature (Soldering 10s) . . . . . 300$^{o}$C
(Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

2. Signals on NC, NO, COM, ADD, or INH exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications +5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 4), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP ($^{o}$C) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON Resistance, $R_{ON}$ | V+ = 4.5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 3.5V (See Figure 5) | 25 | - | - | 150 | Ω |
| | | Full | - | - | 200 | Ω |
| $R_{ON}$ Matching Between Channels, $\Delta R_{ON}$ | V+ = 4.5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 3.5V (Note 7) | 25 | - | 2 | 8 | Ω |
| | | Full | - | - | 15 | Ω |
| $R_{ON}$ Flatness, $R_{FLAT(ON)}$ | V+ = 5.5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 1.5V, 2.5V, 3.5V (Note 8) | Full | - | - | 15.5 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 1V, 4.5V, $V_{NO}$ or $V_{NC}$ = 4.5V, 1V (Note 6) | 25 | -1 | - | 1 | nA |
| | | Full | -10 | - | 10 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 4.5V, 1V, $V_{NO}$ or $V_{NC}$ = 1V, 4.5V (Note 6) | 25 | -1 | - | 1 | nA |
| | | Full | -25 | - | 25 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 5.5V, $V_{COM}$ = 1V, 4.5V, or $V_{NO}$ or $V_{NC}$ = 1V, 4.5V, or Floating (Note 6) | 25 | -1 | - | 1 | nA |
| | | Full | -25 | - | 25 | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$ | | Full | 2.4 | 1.5 | - | V |
| Input Voltage Low, $V_{INL}$ | | Full | - | 1.5 | 0.8 | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 5.5V, $V_{IN}$ = 0V or V+ | Full | -1 | - | 1 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Inhibit Turn-ON Time, $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ =300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3 (See Figure 1) | 25 | - | 90 | 150 | ns |
| | | Full | - | - | 200 | ns |
| Inhibit Turn-OFF Time, $t_{OFF}$ | $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ =300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3 (See Figure 1) | 25 | - | 40 | 120 | ns |
| | | Full | - | - | 180 | ns |

## Electrical Specifications +5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP ($^oC$) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| Address Transition Time, $t_{TRANS}$ | $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ =300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3 (See Figure 1) | 25 | - | 90 | 150 | ns |
| | | Full | - | - | 200 | ns |
| Break-Before-Make Time Delay, $t_D$ | $R_L$ = 300Ω, $C_L$ = 35pF, $V_{NO}$ = $V_{NC}$ = 3V, $V_{IN}$ = 0 to 3 (See Figure 3) | 25 | 5 | 20 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 0.8 | 5 | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz (See Figure 4) | 25 | - | 75 | - | dB |
| Crosstalk (Channel-to-Channel), (ISL84525) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz (See Figure 6) | 25 | - | -85 | - | dB |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) | 25 | - | 4 | - | pF |
| COM OFF Capacitance, $C_{COM(OFF)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84524 | 25 | - | 14 | - | pF |
| | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84525 | 25 | - | 6 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84524 | 25 | - | 20 | - | pF |
| | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84525 | 25 | - | 12 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | | Full | 2 | - | 12 | V |
| Positive Supply Current, I+ | V+ = 5.5V, $V_{IN}$ = 0V or V+, all channels on or off | 25 | -1 | - | 1 | µA |
| | | Full | -10 | - | 10 | µA |

NOTES:

4. $V_{IN}$ = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25$^o$C.
7. $\Delta R_{ON} = R_{ON}$ (MAX) - $R_{ON}$ (MIN).
8. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.

## Electrical Specifications +3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, $V_{AH}$ = 2.4V, $V_{AL}$= 0.8V (Note 4), Unless Otherwise Specified

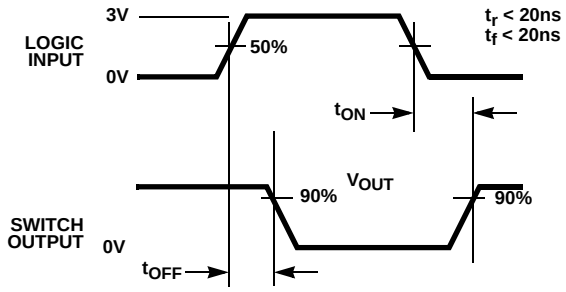
| PARAMETER | TEST CONDITIONS | TEMP ($^oC$) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON Resistance, $R_{ON}$ | V+ = 2.7V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 1.5V (See Figure 5) | 25 | - | - | 400 | Ω |
| | | Full | - | - | 500 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 3.6V, $V_{COM}$ = 1V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 1V (Note 6) | 25 | -1 | - | 1 | nA |
| | | Full | -10 | - | 10 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | V+ = 3.6V, $V_{COM}$ = 3V, 1V, $V_{NO}$ or $V_{NC}$ = 1V, 3V (Note 6) | 25 | -1 | - | 1 | nA |
| | | Full | -25 | - | 25 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 3.6V, $V_{COM}$ = 1V, 3V, or $V_{NO}$ or $V_{NC}$ = 1V, 3V, or floating (Note 6) | 25 | -1 | - | 1 | nA |
| | | Full | -25 | - | 25 | nA |

## Electrical Specifications +3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, $V_{AH}$ = 2.4V, $V_{AL}$= 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

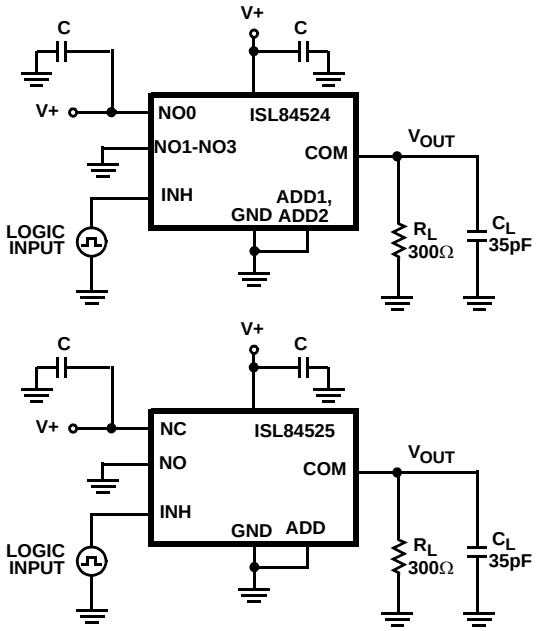
| PARAMETER | TEST CONDITIONS | TEMP ($^{O}$C) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$ | | Full | 2.0 | 1.0 | - | V |
| Input Voltage Low, $V_{INL}$ | | Full | - | 1.0 | 0.5 | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 3.6V, $V_{IN}$ = 0V or V+ | Full | -1 | - | 1 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Inhibit Turn-ON Time, $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ =300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3 (See Figure 1) | 25 | - | 170 | 300 | ns |
| | | Full | - | - | 400 | ns |
| Inhibit Turn-OFF Time, $t_{OFF}$ | $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ =300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3 (See Figure 1) | 25 | - | 50 | 200 | ns |
| | | Full | - | - | 300 | ns |
| Address Transition Time, $t_{TRANS}$ | $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ =300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3 (See Figure 1) | 25 | - | 130 | 300 | ns |
| | | Full | - | - | 400 | ns |
| Break-Before-Make Time Delay, $t_D$ | $R_L$ = 300Ω, $C_L$ = 35pF, $V_{NO}$ or $V_{NC}$ = 1.5V, $V_{IN}$ = 0 to 3 (See Figure 3) | Full | 5 | 40 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 0.8 | 1 | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz (See Figure 4) | 25 | - | 75 | - | dB |
| Crosstalk (Channel-to-Channel) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz (See Figure 6) | 25 | - | -85 | - | dB |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) | 25 | - | 4 | - | pF |
| COM OFF Capacitance, $C_{COM(OFF)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84524 | 25 | - | 14 | - | pF |
| | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84525 | 25 | - | 6 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84524 | 25 | - | 20 | - | pF |
| | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) ISL84525 | 25 | - | 12 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Positive Supply Current, I+ | V+ = 3.6V, $V_{IN}$ = 0V or V+, all channels on or off | 25 | -1 | - | 1 | µA |
| | | Full | -10 | - | 10 | µA |

## Test Circuits and Waveforms




Logic input waveform is inverted for switches that have the opposite logic sense.

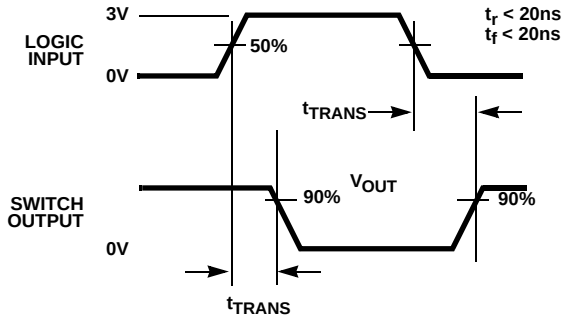
FIGURE 1A. INHIBIT MEASUREMENT POINTS




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

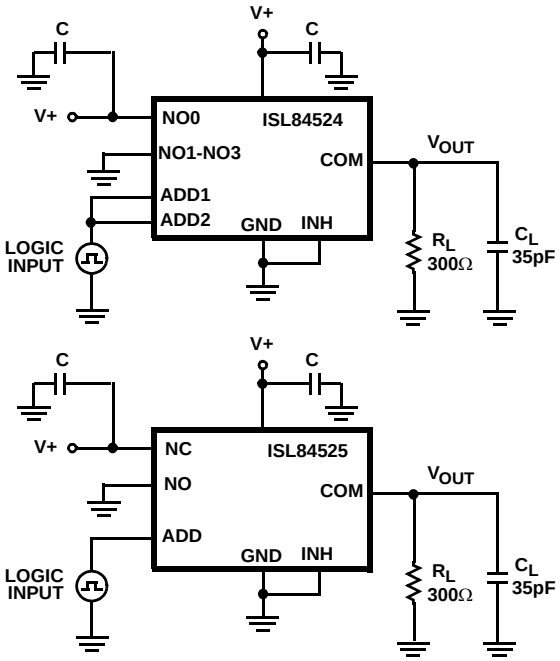
$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. INHIBIT TEST CIRCUIT




Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS MEASUREMENT POINTS




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1D. ADDRESS TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

## Test Circuits and Waveforms (Continued)

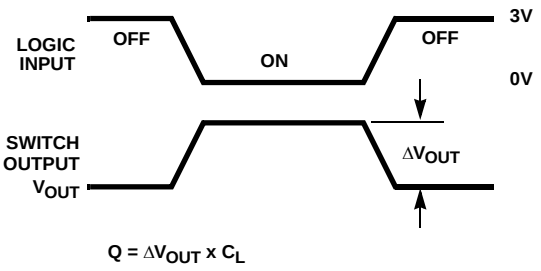



FIGURE 2A. MEASUREMENT POINTS

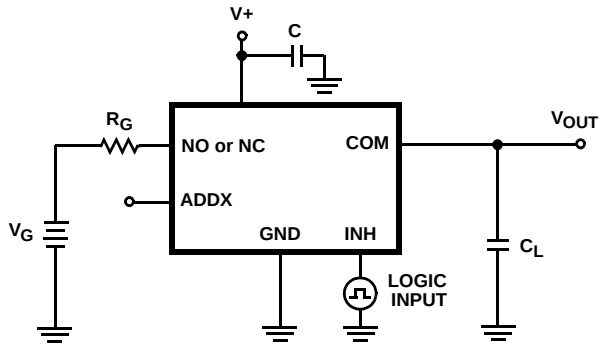



FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

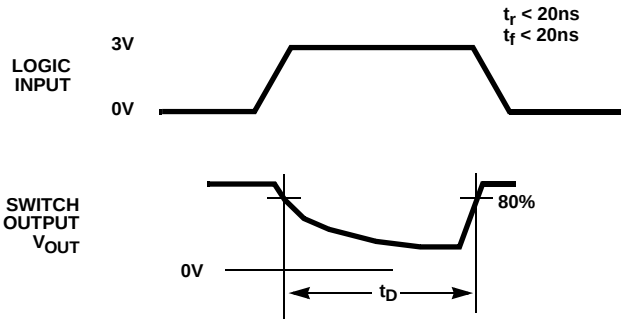
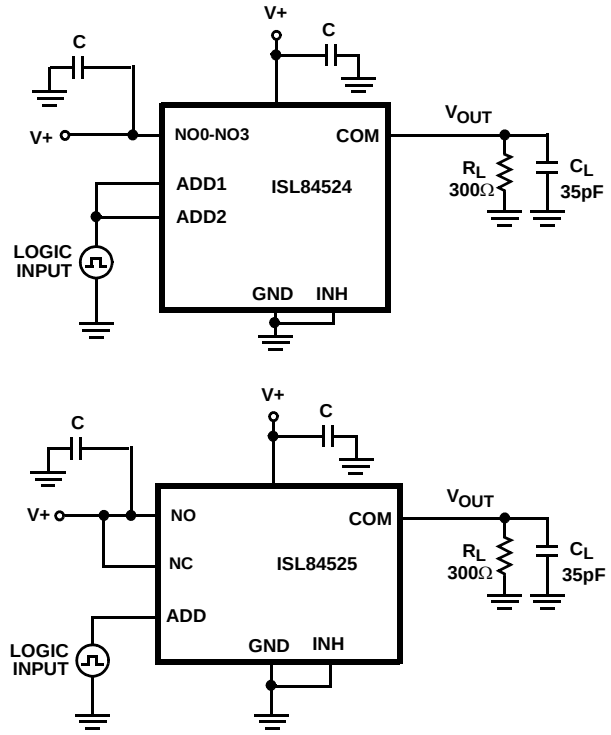



FIGURE 3A. MEASUREMENT POINTS




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

## Test Circuits and Waveforms (Continued)

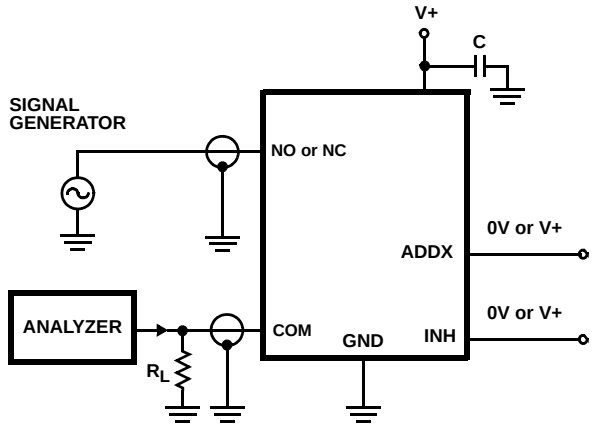



FIGURE 4. OFF ISOLATION TEST CIRCUIT

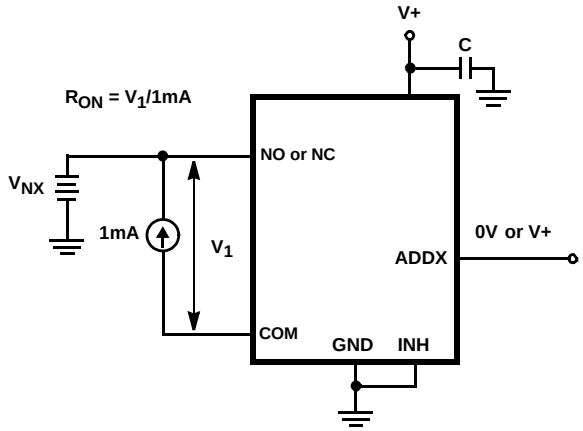



FIGURE 5. $R_{ON}$ TEST CIRCUIT

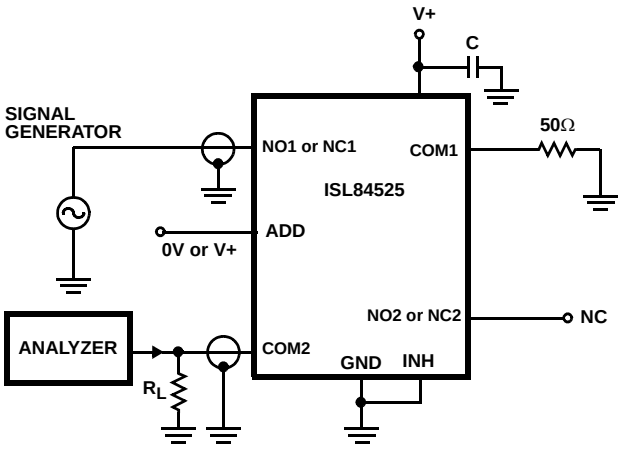



FIGURE 6. CROSSTALK TEST CIRCUIT

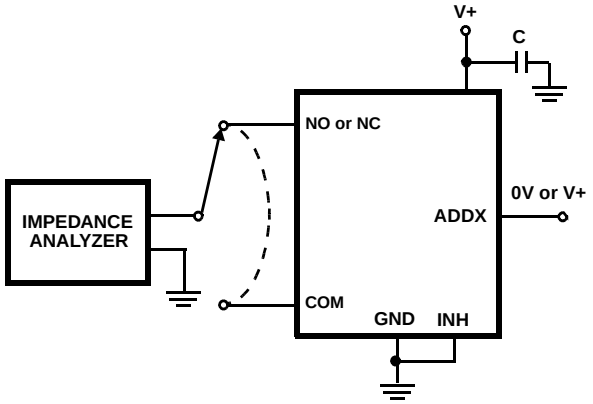



FIGURE 7. CAPACITANCE TEST CIRCUIT

## Detailed Description

The ISL84524 and ISL84525 operate from a single 2V to 12V supply with low on-resistance and high speed operation. The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2.7V), low power consumption (3µW), low leakage currents (25nA max), and the tiny MSOP packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation (75 dB) and crosstalk rejection (-85dB).

### Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low $R_{ON}$ switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

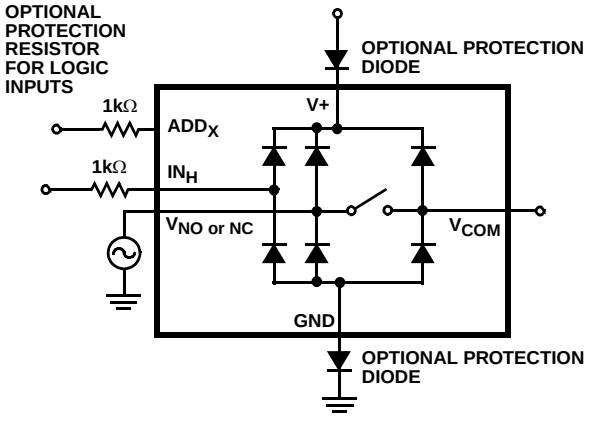



**FIGURE 8. OVERVOLTAGE PROTECTION**

### Power-Supply Considerations

The ISL8452X construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL8452X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and Typical Performance curves for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

### Logic-Level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 2V to 11V. At 12V the $V_{IH}$ level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a $V_{OH}$ greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

### High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figure 13). Figure 13 also illustrates that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 14 details the high Off Isolation and Crosstalk rejection provided by this family. At 10MHz, Off Isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

### Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

## Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

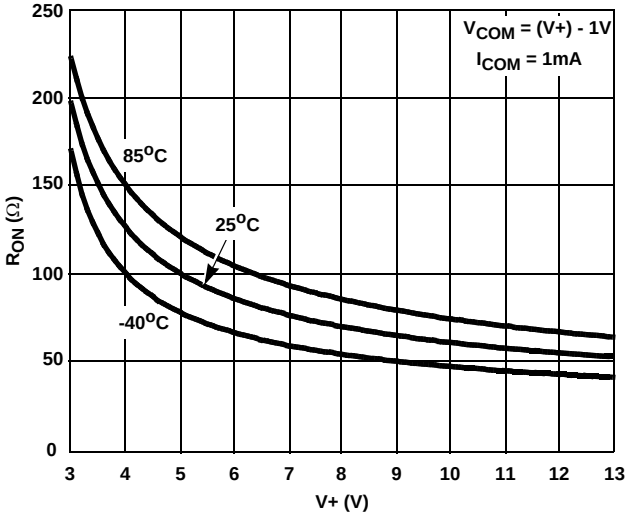



FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE

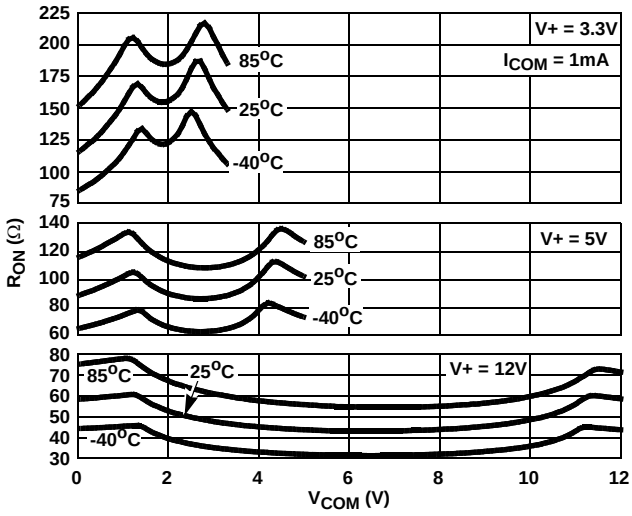



FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

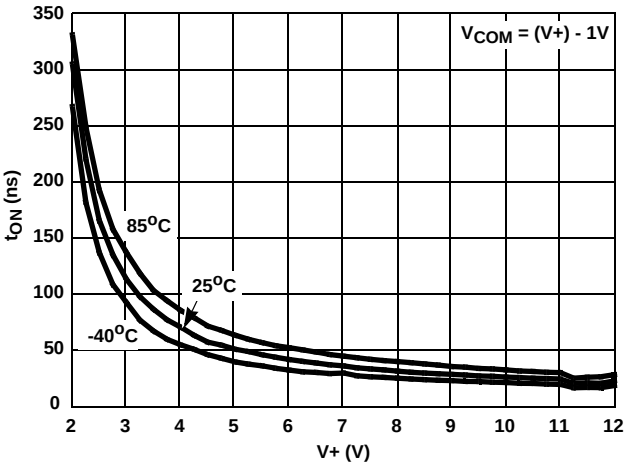



FIGURE 11. TURN - ON TIME vs SUPPLY VOLTAGE

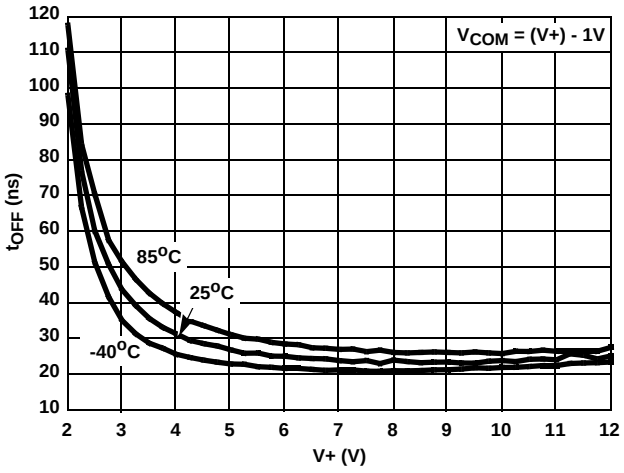



FIGURE 12. TURN - OFF TIME vs SUPPLY VOLTAGE

## Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

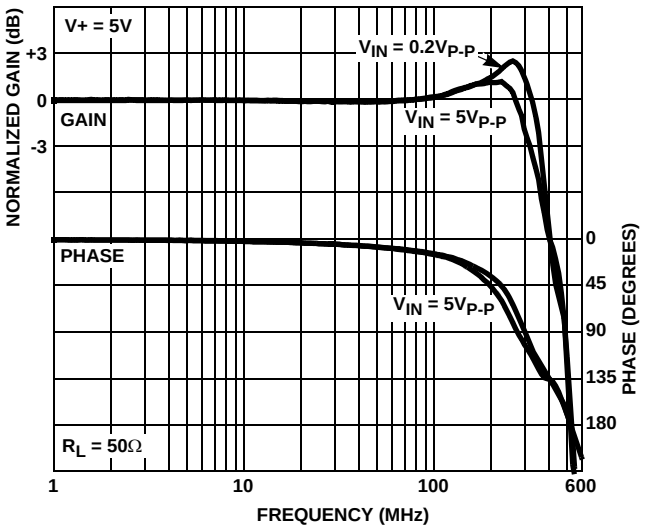



FIGURE 13. FREQUENCY RESPONSE

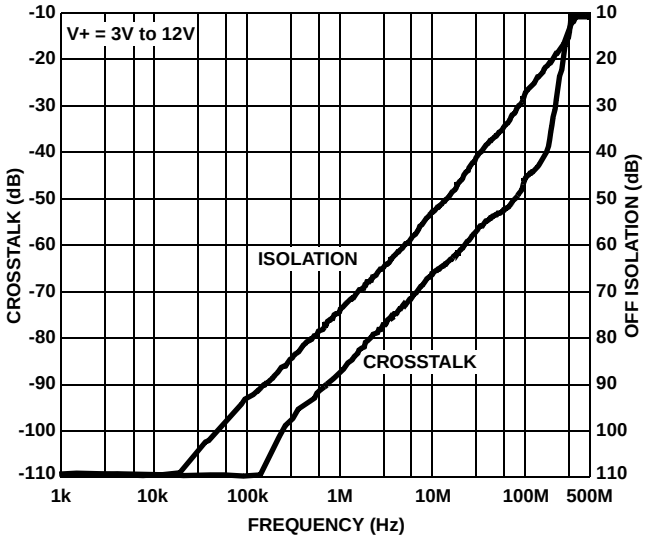



FIGURE 14. CROSSTALK AND OFF ISOLATION

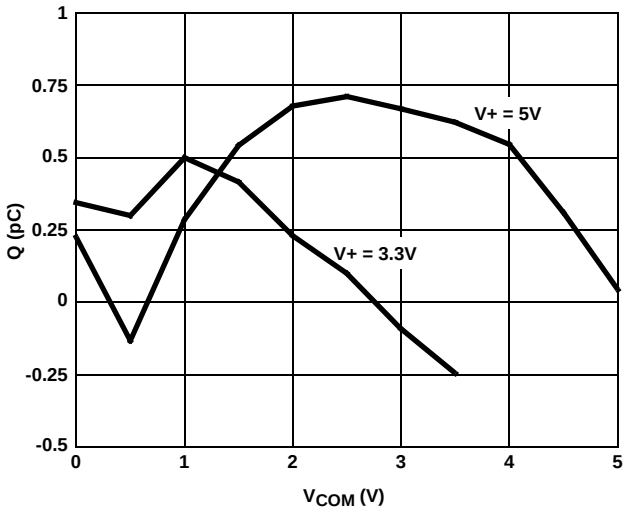



FIGURE 15. CHARGE INJECTION vs SWITCH VOLTAGE

## Die Characteristics

**SUBSTRATE POTENTIAL (POWERED UP):**

GND

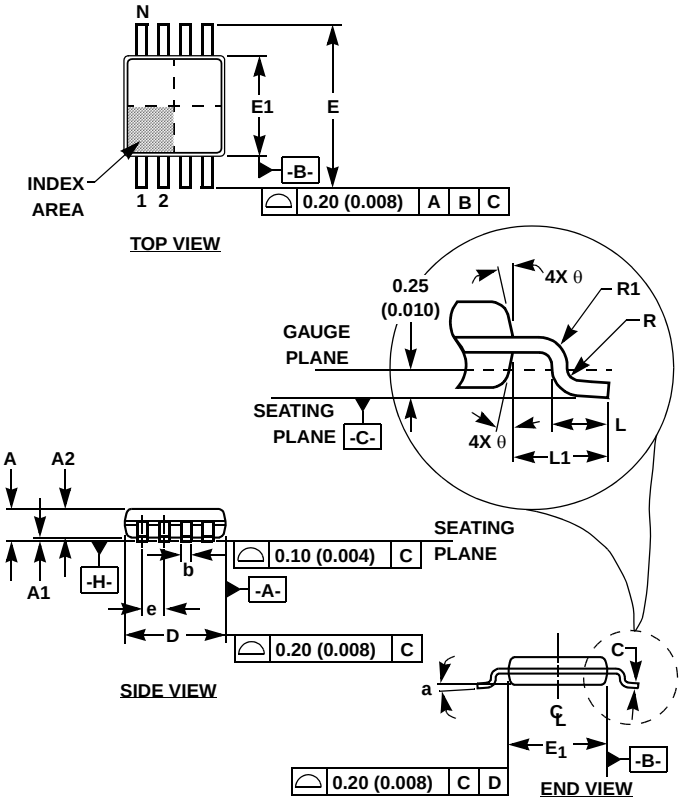
**TRANSISTOR COUNT:**

ISL84524: 193
ISL84525: 193

**PROCESS:**

Si Gate CMOS

## Mini Small Outline Plastic Packages (MSOP)




### M10.118 (JEDEC MO-187BA)

**10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.007 | 0.011 | 0.18 | 0.27 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.020 BSC | | 0.50 BSC | | - |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 REF | | 0.95 REF | | - |
| N | 10 | | 10 | | 7 |
| R | 0.003 | - | 0.07 | - | - |
| R1 | 0.003 | - | 0.07 | - | - |
| θ | $5^o$ | $15^o$ | $5^o$ | $15^o$ | - |
| α | $0^o$ | $6^o$ | $0^o$ | $6^o$ | - |

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [ - H - ] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [ -A - ] and [ - B - ] to be determined at Datum plane [ - H - ].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only