12V Power Distribution Controllers

ISL6115A

This fully featured hot swap power controller targets +12V applications. The ISL6115A with its integrated charge pump has a higher (6.5V vs 5V) gate drive than its sister part the ISL6115 making this part an immediate efficiency improvement replacement.

This IC features programmable overcurrent (OC) detection, current regulation (CR) with time delay to latch-off and soft-start.

The current regulation level is set by 2 external resistors; R_{ISET} sets the CR Vth and the other is a low ohmic sense resistor across, which the CR Vth is developed. The CR duration is set by an external capacitor on the CTIM pin, which is charged with a 20µA current once the CR Vth level is reached. The IC then quickly pulls down the GATE output latching off the pass FET.

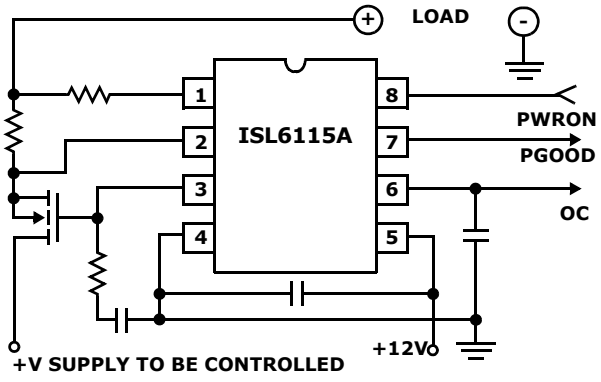
Features

- HOT SWAP Single Power Distribution Control for +12V
- Overcurrent Fault Isolation
- Programmable Current Regulation Level
- Programmable Current Regulation Time to Latch-Off
- Rail-to-Rail Common Mode Input Voltage Range
- Enhanced Internal Charge Pump Drives N-Channel MOSFET gate to 6.5V above IC bias.
- Undervoltage and Overcurrent Latch Indicators
- Adjustable Turn-On Ramp
- Protection During Turn-On
- Two Levels of Overcurrent Detection Provide Fast Response to Varying Fault Conditions
- 1µs Response Time to Dead Short
- Pb-Free (RoHS Compliant)

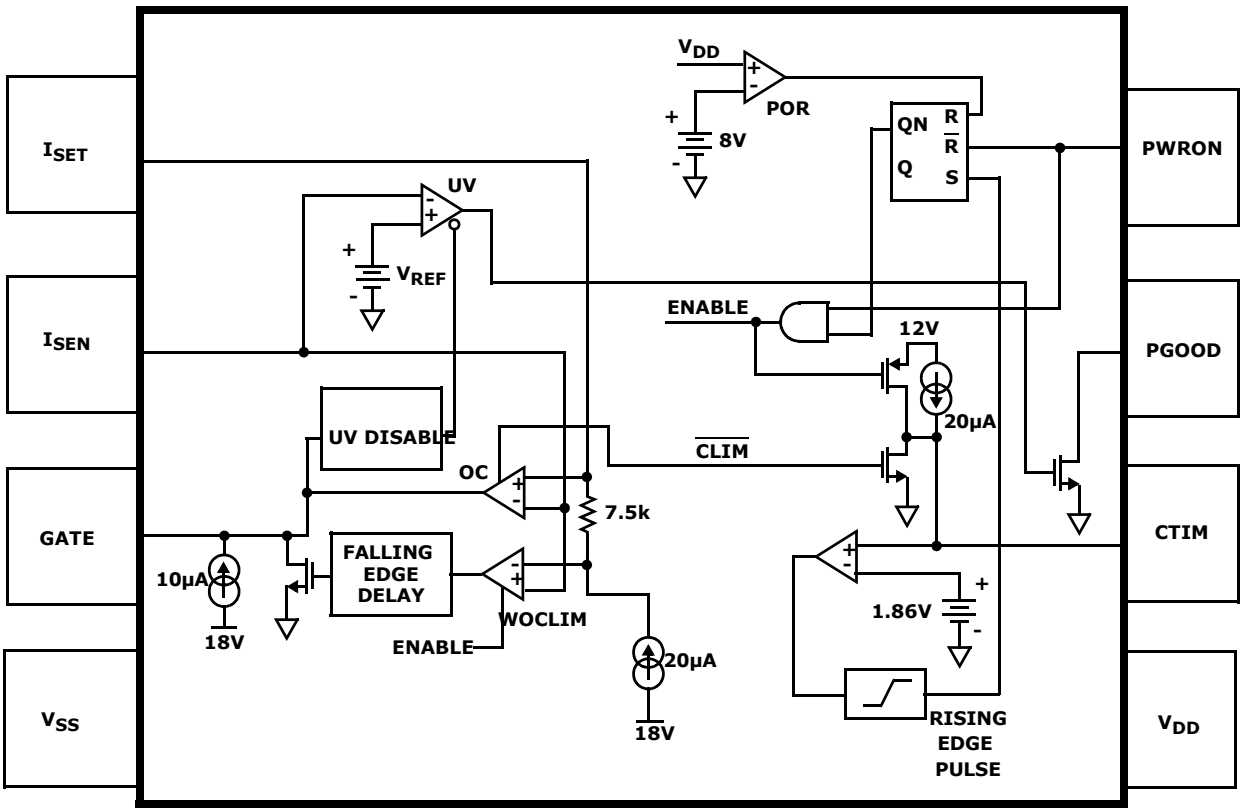
Applications

- Power Distribution Control
- Hot Plug Components and Circuitry

Application Circuits - High Side Controller

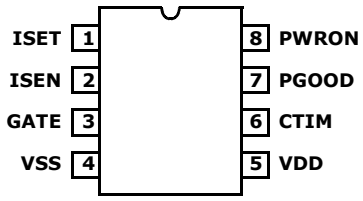


Simplified Block Diagram



Pin Configuration

ISL6115A
(8 LD SOIC)
TOP VIEW



Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6115AIBZ	6115A IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL6115AIBZ-T (Notes 1,)	6115A IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL6115ACBZ	6115A CBZ	0 to +70	8 Ld SOIC	M8.15
ISL6115ACBZ-T (Notes 1,)	6115A CBZ	0 to +70	8 Ld SOIC	M8.15
ISL6115AEVAL1Z	Evaluation Platform			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6115A. For more information on MSL please see techbrief TB363.

Pin Descriptions

PIN NO.	SYMBOL	FUNCTION	DESCRIPTION
1	ISET	Current Set	Connect to the low side of the current sense resistor through the current limiting set resistor. This pin functions as the current limit programming pin.
2	ISEN	Current Sense	Connect to the more positive end of sense resistor to measure the voltage drop across this resistor.
3	GATE	External FET Gate Drive Pin	Connect to the gate of the external N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to V_{DD} +6.5V by an 14µA current source.
4	VSS	Chip Return	
5	VDD	Chip Supply	12V chip supply. This can be either connected directly to the +12V rail supplying the switched load voltage or to a dedicated V_{SS} +12V supply.
6	CTIM	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor determines the time delay between an overcurrent event and chip output shutdown (current limit time-out). The duration of current limit time-out is equal to 93kΩ x C_{TIM}.
7	PGOOD	Power Good Indicator	Indicates that the voltage on the ISEN pin is satisfactory. PGOOD is driven by an open drain N-Channel MOSFET and is pulled low when the output voltage (VISEN) is less than the UV level for the particular IC.
8	PWRON	Power-ON	PWRON is used to control and reset the chip. The chip is enabled when PWRON pin is driven high to a maximum of 5V or is left open. Do not drive this input >5V. After a current limit time-out, the chip is reset by a low level signal applied to this pin. This input has 20µA pull-up capability.

Absolute Maximum Ratings T_A = +25°C

V_{DD} . . . . . -0.3V to +16V
GATE . . . . . -0.3V to V_{DD} + 8V
ISEN, PGOOD, PWRON, CTIM, ISET . . . -0.3V to V_{DD} + 0.3V

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +12V ±15%
Temperature Range (T_A) . . . . . -40°C to +85°C
ESD
Human Body Model 2.5kV
Machine Model 250V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
8 Ld SOIC Package 98
Maximum Junction Temperature (Plastic Package) . . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications V_{DD} = 12V, T_A = T_J = full temperature range, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CURRENT CONTROL						
ISET Current Source	I_{ISET_ft}		**17**	20	**22**	µA
ISET Current Source	I_{ISET_pt}	T_J = +15°C to +55°C	**19**	20	**21**	µA
Current Limit Amp Offset Voltage	Vio_ft	V_{ISET} - V_{ISEN}	**-4.5**	0	**4.5**	mV
Current Limit Amp Offset Voltage	Vio_pt	V_{ISET} - V_{ISEN}, T_J = +15°C to +55°C	**-2**	0	**2**	mV
GATE DRIVE						
GATE Response Time to Severe OC	pd_woc_amp	V_{GATE} to 10.8V	**-**	100	**-**	ns
GATE Response Time to Overcurrent	pd_oc_amp	V_{GATE} to 10.8V	**-**	600	**-**	ns
GATE Turn-On Current	I_{GATE}	V_{GATE} to = 6V	**10.8**	14	**16.7**	µA
GATE Pull-Down Current	OC_GATE_I_4V	Overcurrent	**45**	82	**124**	mA
GATE Pull-Down Current (Note 6)	WOC_GATE_I_4V	Severe Overcurrent	**-**	0.8	**-**	A
Undervoltage Threshold	$12V_{UV\_VTH}$		**8.9**	9.6	**10.2**	V
GATE High Voltage	12VG	GATE Voltage	**V_{DD} + 5.7V**	V_{DD} + 6.5V	**-**	V
BIAS						
V_{DD} Supply Current	I_{VDD}		**-**	3	**3.9**	mA
V_{DD} POR Rising Threshold	$V_{DD\_POR\_L2H}$	VDD Low to High	**7**	8.4	**9**	V
V_{DD} POR Falling Threshold	$V_{DD\_POR\_H2L}$	VDD High to Low	**6.9**	8.1	**8.7**	V
V_{DD} POR Threshold Hysteresis	$V_{DD\_POR\_HYS}$	$V_{DD\_POR\_L2H}$ - $V_{DD\_POR\_H2L}$	**0.1**	0.3	**0.5**	V
Maximum PWRON Pull-Up Voltage	PWRN_PUV	Maximum External Pull-up Voltage	**-**	5	**-**	V
PWRON Pull-Up Voltage	PWRN_V	PWRON Pin Open	**2.5**	3.2	**-**	V
PWRON Rising Threshold	PWR_Vth		**1.1**	1.7	**2.35**	V
PWRON Hysteresis	PWR_hys		**125**	170	**250**	mV
PWRON Pull-Up Current	PWRN_I		**12.6**	17	**24**	µA

Electrical Specifications V_{DD} = 12V, $T_A = T_J$ = full temperature range, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CURRENT REGULATION DURATION/POWER GOOD						
C_{TIM} Charging Current	C_{TIM}_ichg0	V_{CTIM} = 0V	**17.2**	20.5	**25**	µA
C_{TIM} Fault Pull-Up Current (Note 6)			-	20	**-**	mA
Current Limit Time-Out Threshold Voltage	C_{TIM}_Vth	CTIM Voltage	**1.6**	1.8	**2.1**	V
Power Good Pull Down Current	PG_Ipd	V_{OUT} = 0.5V	**-**	8	**-**	mA

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Description and Operation

The ISL6115A is targeted for +12V single power supply distribution control for generic hot swap switching applications.

This ICs features a highly accurate programmable current regulation (CR) level with programmable time delay to latch-off, and programmable soft-start turn-on ramp all set with a minimum of external passive components. It also includes severe OC protection that immediately shuts down the MOSFET switch should a rapid load current transient such as with a dead short cause the CR Vth to exceed the programmed level by 150mV. Additionally, it has an UV indicator and an OC latch indicator. The functionality of the PGOOD feature is enabled once the IC is biased, monitoring and reporting any UV condition on the ISEN pin.

Upon initial power-up, the IC can either isolate the voltage supply from the load by holding the external N-Channel MOSFET switch off or apply the supply rail voltage directly to the load for true hot swap capability. The PWRON pin must be pulled low for the device to isolate the power supply from the load by holding the external N-Channel MOSFET off. With the PWRON pin held high or floating the IC will be in true hot swap mode. In both cases the IC turns on in a soft-start mode protecting the supply rail from sudden inrush current.

At turn-on, the external gate capacitor of the N-Channel MOSFET is charged with a 11µA current source resulting in a programmable ramp (soft-start turn-on). The internal ISL6115A charge pump supplies the gate drive for the 12V supply switch driving that gate to ~V_{DD} +6.5V. Load current passes through the external current sense resistor. When the voltage across the sense resistor exceeds the user programmed CR voltage threshold value, (see Table 1 for R_{ISET} programming resistor value and resulting nominal current regulation threshold voltage, V_{CR}) the controller enters its current regulation mode. At this time, the time-out capacitor, on CTIM pin is charged with a 20µA current source and the controller enters the current limit time to latch-off period. The length of the current limit time to latch-off duration is set by the value of a single external capacitor (see Table 2) for C_{TIM} capacitor value and resulting nominal current limited time-out to latch-off duration placed from the CTIM pin (pin 6) to ground. The programmed current level is held until either the OC event passes or the time-out period expires. If the former is the case then the N-Channel MOSFET is fully enhanced and the C_{TIM} capacitor is discharged. Once C_{TIM} charges to ~1.8V signaling that the time-out period has expired, an internal latch is set whereby the FET gate is quickly pulled to 0V turning off the N-Channel MOSFET switch, isolating the faulty load.

TABLE 1. R_{ISET} PROGRAMMING RESISTOR VALUE

R_{ISET} RESISTOR	NOMINAL CR VTH
10kΩ	200mV
4.99kΩ	100mV
2.5kΩ	50mV
1.25kΩ	25mV

NOTE: Nominal Vth = R_{ISET} x 20µA.

TABLE 2. C_{TIM} CAPACITOR VALUE

C_{TIM} CAPACITOR	NOMINAL CURRENT LIMITED PERIOD
0.022µF	2ms
0.047µF	4.4ms
0.1µF	9.3ms

NOTE: Nominal time-out period = C_{TIM} x 93kΩ.

This IC responds to a severe overcurrent load (defined as a voltage across the sense resistor >150mV over the OC Vth set point) by immediately driving the N-Channel MOSFET gate to 0V in about 10µs. The gate voltage is then slowly ramped up turning on the N-Channel MOSFET to the programmed current regulation level; this is the start of the time-out period.

Upon a UV condition, the PGOOD signal will pull low when connected through a resistor to the logic or VDD supply. This pin is a UV fault indicator. For an OC latch-off indication, monitor CTIM, pin 6. This pin will rise rapidly from 1.8V to VDD once the time-out period expires.

See Figures 2 through 13 for graphs and waveforms related to text.

The IC is reset after an OC latch-off condition by a low level on the PWRON pin and is turned on by the PWRON pin being driven high.

Application Considerations

Design applications where the CR Vth is set extremely low (25mV or less), there is a two-fold risk to consider.

- There is the susceptibility to noise influencing the absolute CR Vth value. This can be addressed with a 100pF capacitor across the R_{SENSE} resistor.
- Due to common mode limitations of the overcurrent comparator, the voltage on the ISET pin must be 20mV above the IC ground either initially (from I_{SET}*R_{SET}) or before C_{TIM} reaches time-out (from gate charge-up). If this does not happen, the IC may incorrectly report overcurrent fault at start-up when there is no fault. Circuits with high load capacitance and initially low load current are susceptible to this type of unexpected behavior.

Do not signal nor pull-up the PWRON input to > 5V. Exceeding 6V on this pin will cause the internal charge pump to malfunction.

During the soft-start and the time-out delay duration with the IC in its current limit mode, the V_{GS} of the external N-Channel MOSFET is reduced driving the MOSFET switch into a (linear region) high $r_{DS(ON)}$ state. Strike a balance between the CR limit and the timing requirements to avoid periods when the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the **MOSFET SOA** information in the manufacturer's data sheet.

When driving particularly large capacitive loads a longer soft-start time to prevent current regulation upon charging and a short CR time may offer the best application solution relative to reliability and FET MTF.

Physical layout of R_{SENSE} resistor is critical to avoid the possibility of false overcurrent occurrences. Ideally, trace routing between the R_{SENSE} resistors and the IC is as direct and as short as possible with zero current in the sense lines (see Figure 1).

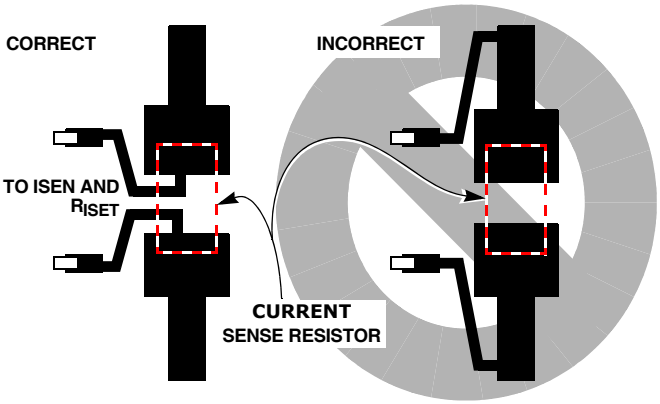


FIGURE 1. SENSE RESISTOR PCB LAYOUT

Typical Performance Curves

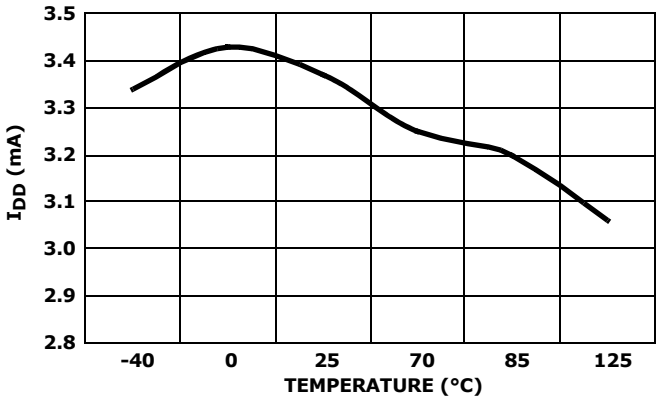


FIGURE 2. V_{DD} BIAS CURRENT

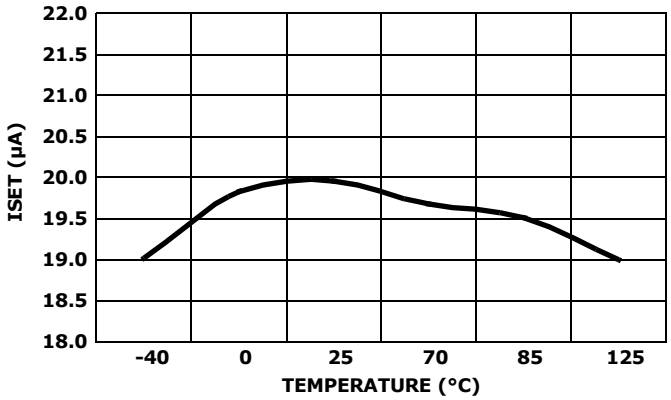


FIGURE 3. I_{SET} SOURCE CURRENT

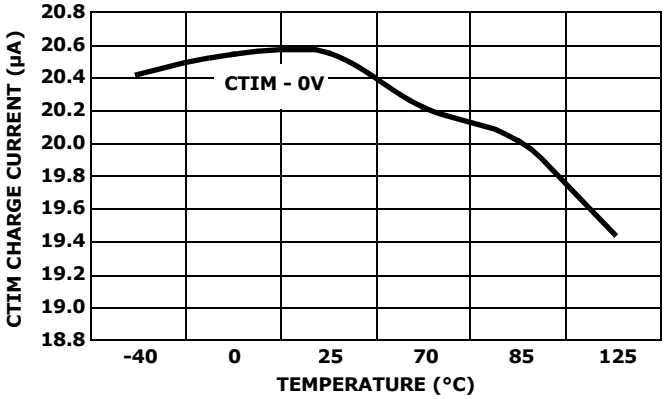


FIGURE 4. C_{TIM} CURRENT SOURCE

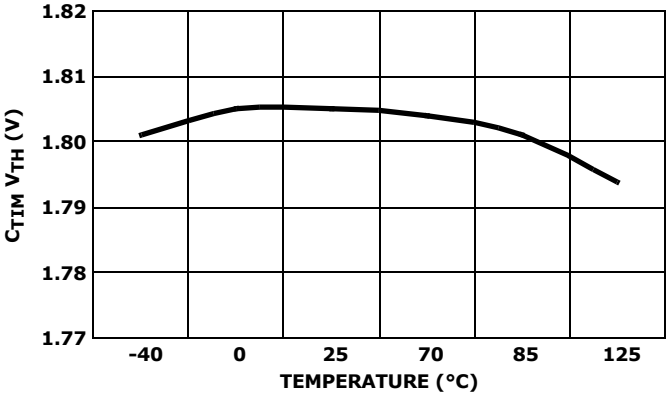


FIGURE 5. C_{TIM} OC VOLTAGE THRESHOLD

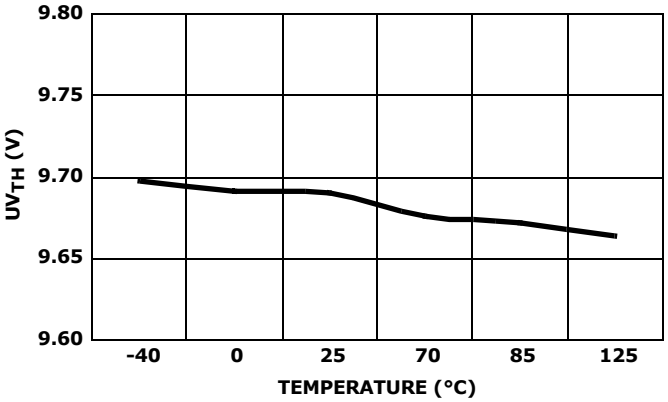


FIGURE 6. UV THRESHOLD

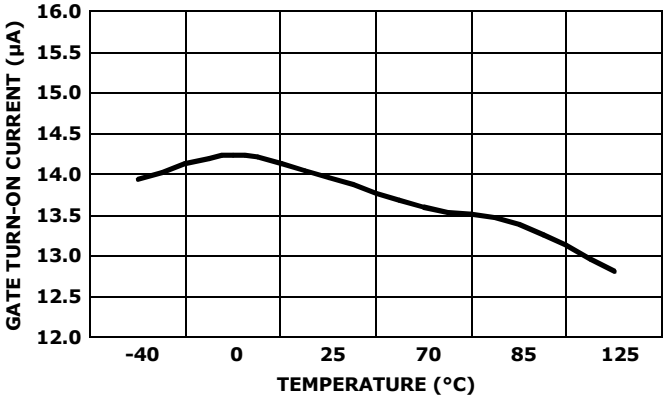


FIGURE 7. GATE CHARGE CURRENT

Typical Performance Curves (Continued)

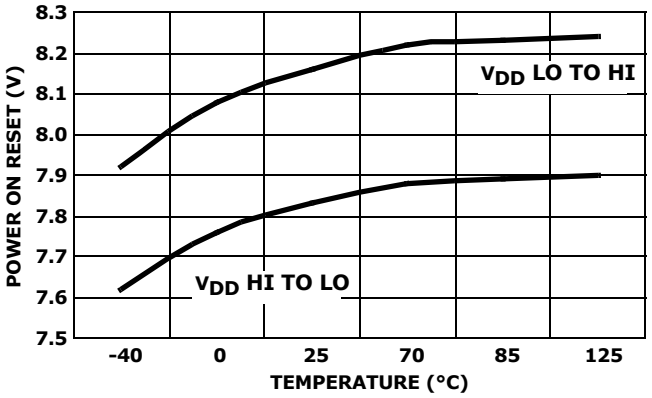


FIGURE 8. POWER-ON RESET VOLTAGE THRESHOLD

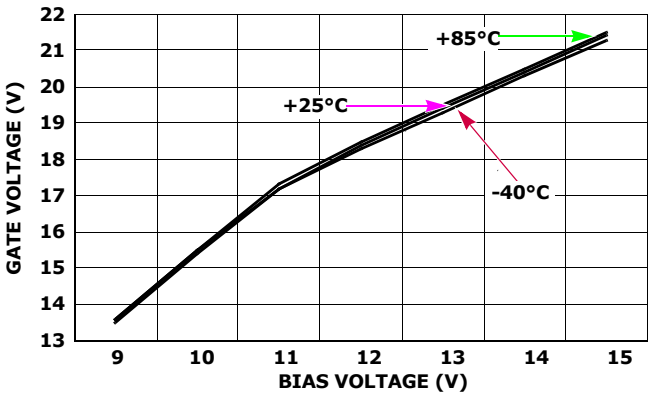


FIGURE 9. GATE VOLTAGE vs BIAS and TEMPERATURE

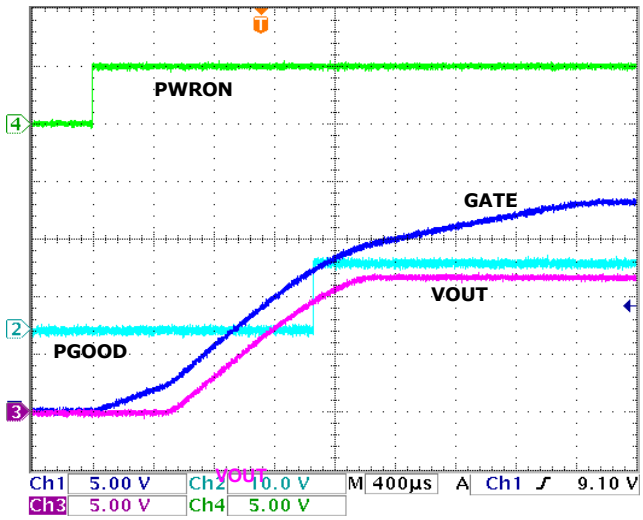


FIGURE 10. ISL6115A TURN-ON

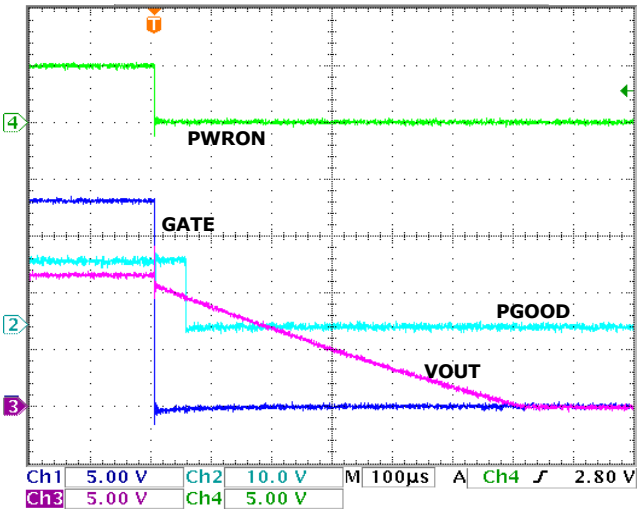


FIGURE 11. ISL6115A TURN-OFF

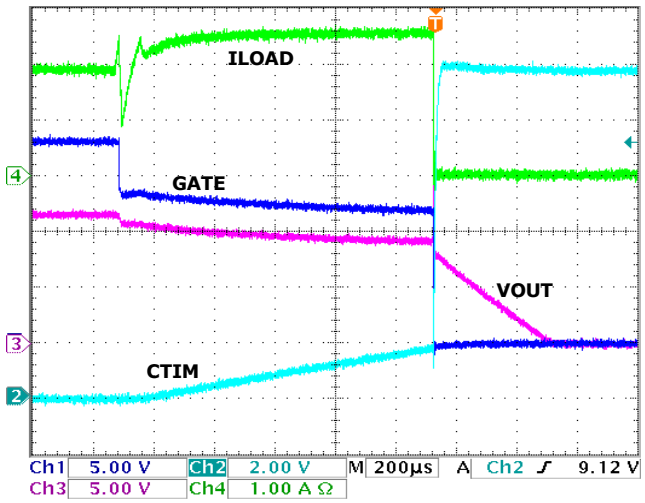


FIGURE 12. IOC REGULATION and TURN-OFF

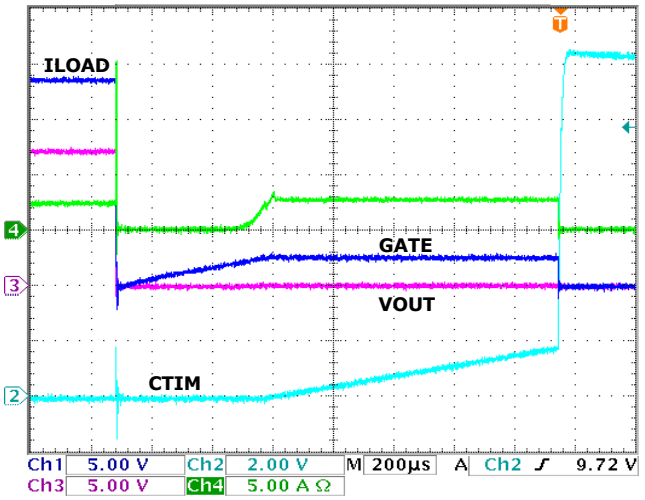


FIGURE 13. WOC TURN-OFF and RESTART

ISL6115AEVAL1Z Board

The ISL6115AEVAL1Z is default provided as a +12V high side switch controller with the CR level set at ~2.5A. See Figure 11 for ISL6115AEVAL1Z schematic and Table 3 for BOM. Bias and load connection points are provided along with test points for each IC pin.

With J1 installed the ISL6115A will be biased from the +12V supply (V_{IN}) being switched. Connect the load to VLOAD+. PWRON pin pulls high internally enabling the ISL6115A if not driven low via PWRON test point or J2.

With R_3 = 1.24kΩ the CR Vth is set to 24.8mV and with the 10mΩ sense resistor (R_1) the ISL6115AEVAL1Z has a nominal CR level of 2.5~A. The 0.01µF delay time to latch-off capacitor results in a nominal 1ms before latch-off of output after an OC event.

Reconfiguring the ISL6115AEVAL1Z board for a higher CR level can be done by changing the R_{SENSE} and/or R_{ISET} resistor values as the provided FET is rated for a much higher current.

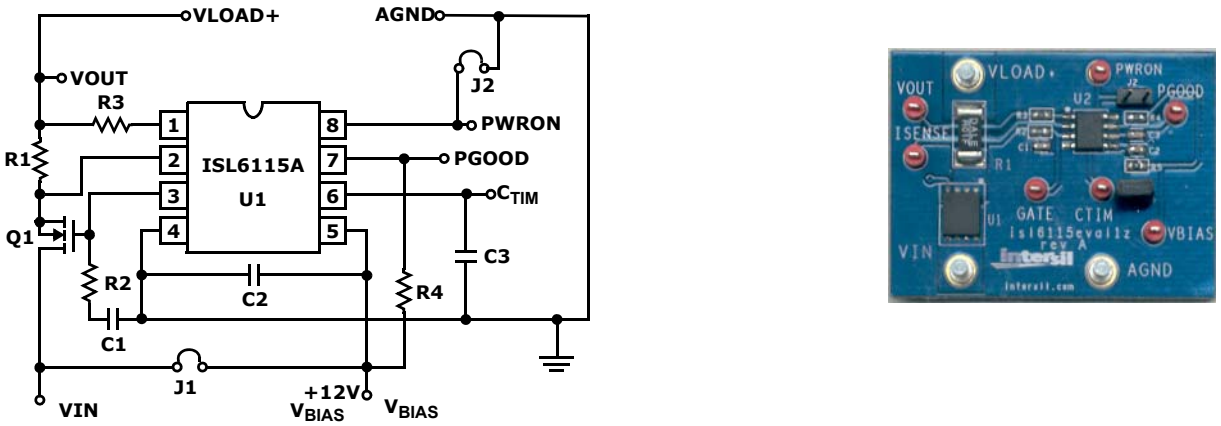
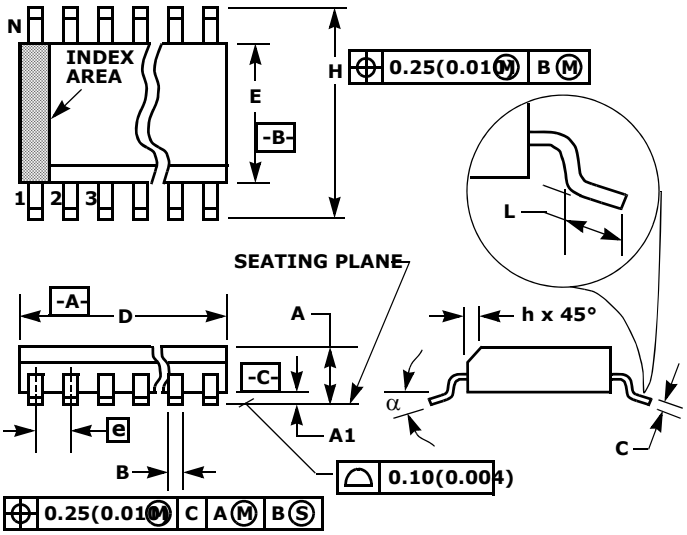


FIGURE 14. ISL6115AEVAL1Z HIGH SIDE SWITCH APPLICATION and PHOTOGRAPH

TABLE 3. BILL OF MATERIALS, ISL6115AEVAL1Z

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
U1	ISL6115A	Intersil
Q1	N-FET	11.5mΩ, 30V, 11.5A Logic Level N-Channel Power MOSFET or equivalent
R1	Load Current Sense Resistor	WSL-2512 10mΩ 1W Metal Strip Resistor
R2	Gate Stability Resistor	20Ω 0603 Chip Resistor
R3	Overcurrent Voltage Threshold Set Resistor	1.24kΩ 0603 Chip Resistor (Vth = 24.8mV)
R4	PGOOD Pull up Resistor	10kΩ 0603 Chip Resistor
C1	Gate Timing Capacitor	0.001µF 0402 Chip Capacitor (<2ms)
C2	IC Decoupling Capacitor	0.1µF 0402 Chip Capacitor
C3	Time Delay Set Capacitor	0.01µF 0402 Chip Capacitor (1ms)
J1	Bias Voltage Selection Jumper	Install if switched rail voltage is = +12V. Remove and provide separate +12V bias voltage to U2 via V_{BIAS} if ISL6116, ISL6117 or ISL6120 is being evaluated.
J2	PWRON Disable	Install J2 to disable U2. Connects PWRON to GND.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
a	0°	8°	0°	8°	-

Rev. 1 6/05

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