High Speed Triple Laser Diode Drivers

ISL58315

The ISL58315 is a high-speed, triple-output laser diode driver (LDD) for laser scanning projector systems, which require three channels modulated at high speed with independent current control.

Each output channel provides laser-independent current control for threshold and color DACs. Separate scale DACs allow independent scaling of both threshold and color DAC output values. This allows control of projector brightness and can be used to simplify automatic power calibration (APC) for laser-based systems.

Pixel data information is transferred through the LDD's high-speed 10-bit or 15-bit parallel video interface. Three parallel interface modes provide flexibility and allow users a trade-off among speed, power and bus width. Pixel data employs a double data rate scheme, allowing video data to be transferred using both clock edges.

Applications

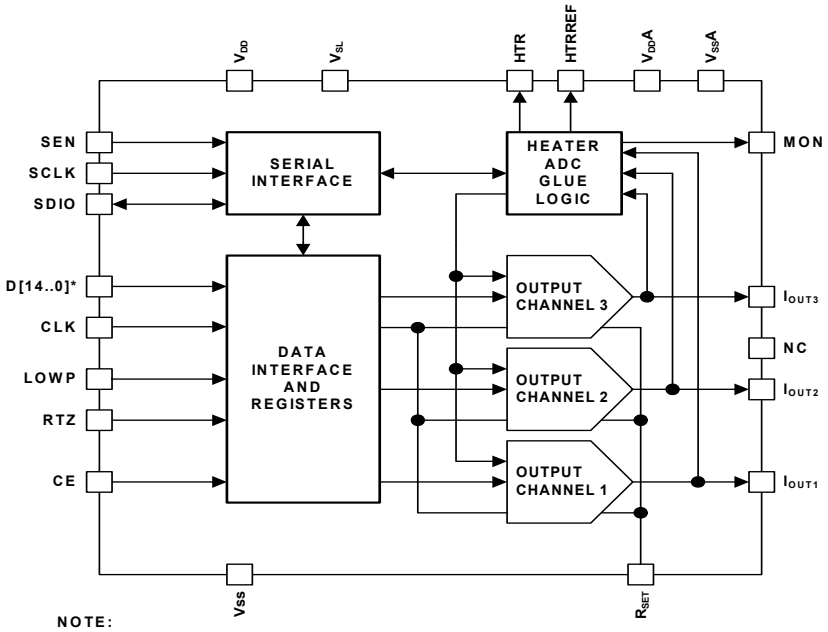
- Laser-based Pico Projectors
- RGB Scanning and Field-based laser projection systems
- Generic laser-based applications requiring multiple, independently controlled lasers

Related Literature

- See application block diagram for Pico Projector (MEMS) at: http://www.intersil.com/applications/PicoProjector%28MEMS%29.asp

Features

- High-speed, triple-output laser diode driver supporting up to 720-pixel HD resolution
- Up to 1A of peak current output
- Fast output switching speeds with pulse rise/fall times of 1ns to 2ns for crisp pixels
- Intersil patented laser voltage sampler function provides dynamic power management capability to dramatically minimize system power
- Intersil patented SmartLinearizer™ DAC feature provides a linear transfer function (input video code to green laser output), eliminating the need for DSP controller processing algorithms required for non-linear green lasers
- Flexible 10-bit or Intersil patented 15-bit RGB pixel input formats supported to reduce speed and power. 300MHz maximum data Input rate supported for 10-bit RGB mode
- Blanking time power reduction reduces LDD current consumption to 3mA typical
- Programmable return-to-zero (RTZ) function provides maximum flexibility
- Integrated heater function for SHG green lasers reduces external components
- Single 3.3V supply and 1.8V video interface compatible for low power



NOTE:
* THE FOLLOWING DATA LINES HAVE ALTERNATIVE USE, DEPENDING ON REGISTER SETTING: D2 = EN3, D4 = EN2, D6 = EN1, AND D10 = SYNC

FIGURE 1. BLOCK DIAGRAM

Typical Application Circuits

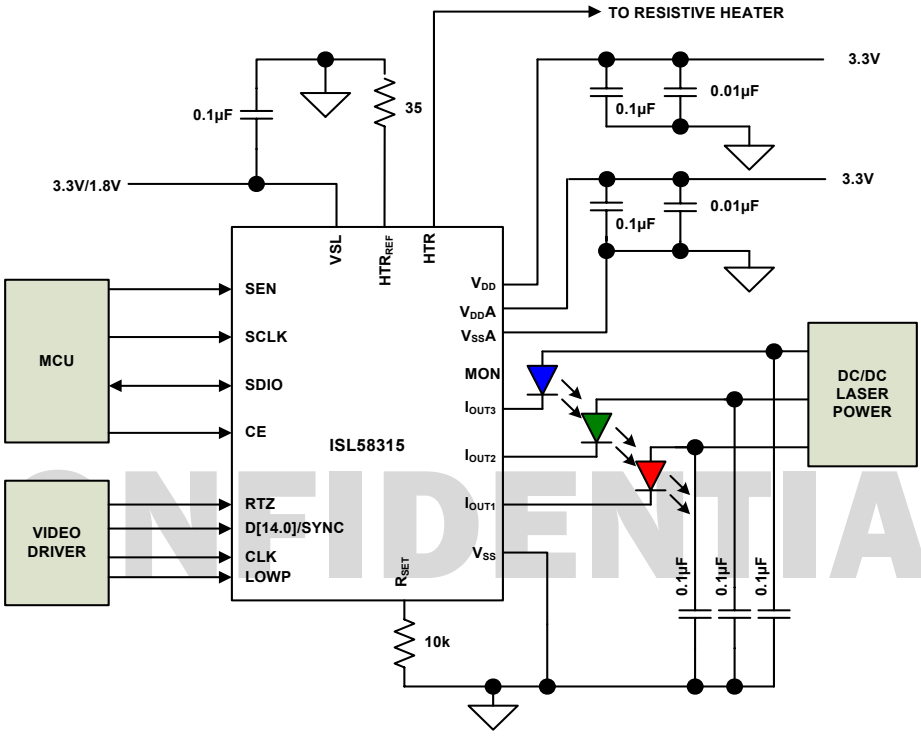
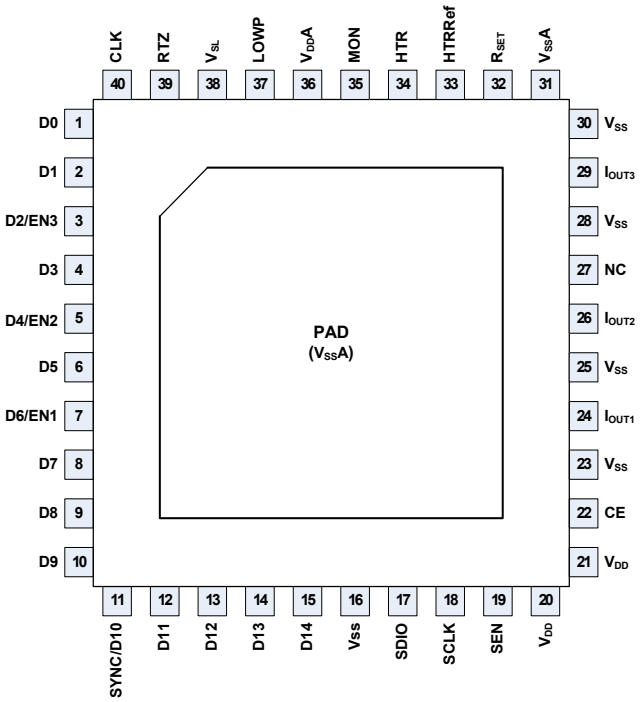


FIGURE 2. ISL58315 TYPICAL APPLICATION

Pin Configurations

ISL58315
(40 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN #	PIN TYPE	PIN DESCRIPTION
CE	22	Digital	CE is an input 3.3V logic signal. When high, it enables the device. Other enables are in the registers.
LOWP	37	Digital	LOWP is a 3.3V signal. When LOWP is asserted (high), the device goes into low-power mode.
RTZ	39	Digital	RTZ signal can be operated with 1.8V or 3.3V. The operating voltage is selected via Reg 0x08 Bits 6 and 7. By default, it is 1.8V. This is a high-speed signal.
D14 to D0	15, 14, 13, 12, 10, 9, 8, 6, 4, 2, 1 (Pins 11, 7, 5, 3 described separately)	Digital	These 15 pins form the Input Pixel Data bus. RGB data enters this bus to drive the laser output channels. See “Functional Description” on page 11 for specific data formats. These signals can be either 1.8V or 3.3V CMOS logic. The operating voltage is selected via Reg 0x08 Bit 6 and 7. By default, it is 1.8V. NOTE: D2, D4, D6 and D10 have alternate functions depending on DATA CONTROL REGISTER - ADDRESS 0x08 Bits 2-0. See description for pins EN1, EN2, EN3 and Sync.
SYNC/D10	11	Digital	Sync signal is shared with D10. Sync has an effect only if input data bus mode 2 is selected. This signal can be operated at 1.8V or 3.3V. The operating voltage is selected via Reg 0x08 Bit 6 and 7. By default, it is 1.8V.
D2/EN3	3	Digital	This signal is available only when the LDD is programmed to use Mode 3 pixel input data format. This signal is shared with D2. EN3 is the output Channel 3 enable signal that allows an external ASIC direct control of enable. It is intended for use with field sequential applications. This signal can be operated at 1.8V or 3.3V. The operating voltage is selected via Reg 0x08 Bit 6 and7. By default, it is 1.8V.
D4/EN2	5	Digital	This signal is available only when the LDD is programmed to use Mode 3 pixel input data format. This signal is shared with D4. EN2 is the output Channel 2 enable signal that allows an external ASIC direct control of enable. It is intended for use with field sequential applications. This signal can be operated at 1.8V or 3.3V. The operating voltage is selected via Reg 0x08 Bit 6 and 7. By default, it is 1.8V.
D6/EN1	7	Digital	This signal is available only when the LDD is programmed to use Mode 3 pixel input data format. This signal is shared with D6. EN1 is the output Channel 1 enable signal that allows an external ASIC direct control of enable. It is intended for use with field sequential applications. This signal can be operated at 1.8V or 3.3V. The operating voltage is selected via Reg 0x08 Bit 6 and 7. By default, it is 1.8V.
CLK	40	Digital	CLK is the input pixel clock. It is used to latch each I_{OUT} channel’s pixel amplitude data. Both clock edges are used. Nominal duty cycle should be 50%. For specific operating modes, see “Input Pixel Data Interface” on page 11. The clock signal can be operated at 1.8V or 3.3V. The operating voltage is selected via Reg 0x08 Bit 6 and 7. By default, it is 1.8V.
SEN	19	Digital	SEN is a 3.3V signal. It is the SPI enable.
SCLK	18	Digital	SCLK is a 3.3V signal. It is the SPI data clock.
SDIO	17	Digital	SDIO is a 3.3V signal. It is the SPI bi-directional serial data.
I_{OUT1}	24	Analog	Current output for the I_{OUT1} laser. Current is sunk from the laser cathode to ground. I_{OUT1} and I_{OUT3} have similar performance capability.
I_{OUT3}	29	Analog	Current output for the I_{OUT3} laser. Current is sunk from the laser cathode to ground. I_{OUT1} and I_{OUT3} have similar performance capability.
I_{OUT2}	26	Analog	Current output for the I_{OUT2} laser. I_{OUT2} can sink high current; up to 1000mA peak.
R_{SET}	32	Reference	R_{SET} pin allows for an external resistor to analog ground that sets the chip bias current level. All other chip reference currents are derived from R_{SET}. A typical resistance is 10kΩ with 1% tolerance, and it should be placed as close to the pin as possible.
V_{DD}	20, 21	Power	Power supply pins for the device (can be applied after V_{DD}A or at the same time). Typical 3.3V. Independent de-coupling capacitors should be tied to each of these pins (Note 1).

Pin Descriptions (Continued)

PIN NAME	PIN #	PIN TYPE	PIN DESCRIPTION
$V_{DD}A$	36	Power	Analog block power supply pin. Analog power de-coupling should use pin pair 36 and 31 ($V_{DD}A$ and $V_{SS}A$), respectively. A de-coupling capacitor should be tied between these two pins. Power-up sequence requires this supply to come up first (Note 1).
V_{SL}	38	Power	Supplies power to the data input circuity. Voltage applied to this pin should be either 1.8V or 3.3V, depending on the data logic levels. Register 0x08 Bit 6 and 7 must be set to correspond to this voltage (can be applied after $V_{DD}A$ or at the same time). This pin should be de-coupled using a pair of 0.01µF and 0.1µF capacitors to ground.
V_{SS}	16, 23, 25, 28, 30	Power	GND connections should be made on the PCB to all GND pins.
$V_{SS}A$	31	Power	Analog ground pin. Pair with Pin 36 V_{DD} for de-coupling.
HTR	34	Analog	This signal connects to the target heater and output currents to drive a 35Ω resistive heater.
HTRRef	33	Analog	This signal connects to an external resistor whose value should closely match the nominal resistance of the target heating element. A current is output to create a voltage reference for the heater circuit. See “Heater Control” on page 17 for a detailed discussion.
MON	35	DNC	Test pin reserved for factory testing use. Do not tie to ground.
NC	27	NA	Not connected internally.
PAD	PAD	Power	Thermal pad of the device; connected to power ground ($V_{SS}A$).

NOTE:
1. Power sequence is as follows: either all supplies must start at the same time or must start in the following order: (1) $V_{DD}A$, (2) V_{DD}, (3) V_{SL}.

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL58315CRTZ	58315 CRTZ	0 to +85	40 Ld TQFN	L40.5x5
ISL58315CRTZ-EVAL	Evaluation Board			
ISL58315LMREF-EVALZ (Note 5)	Evaluation Board			

NOTES:
2. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL58315. For more information on MSL please see Tech Brief TB363.
5. Pico Reference Design Platform. Contact Intersil Marketing for full details.

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Absolute Maximum Ratings T_A = +25°C

Supply Voltage, V_{DD} 4.0V
Voltage at I_{OUT1}, I_{OUT3} 9.5V
Voltage at I_{OUT2} 3.6V
Peak Output Current, I_{OUT1}, I_{OUT3} 1000mA
Peak Output Current, I_{OUT2} 2000mA
Logic Input Voltages . . . . -0.3V to V_{DD} +0.3Vor 4.0V which ever is smaller
Current into R_{SET} 5mA
ESD Rating
  Human Body Model (per JESD22-A114-F) 5000V
  Machine Model (per JESD22-A115-C) 250V
  Charged Device Model (per JESD22-C110-D) 2000V
Latch Up (Tested per JESD-78; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld TQFN (Notes 6, 7)	28.5	0.9

Operating Temperature Range . . . . . 0°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . -0°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests; therefore, $T_J = T_C = T_A$.

DC Electrical Specifications

Unless otherwise indicated, all of the following tables are: $V_{DD}A = V_{DD}$ = 3.3V, R_{SET} = 10kΩ, T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{DD}, V_{DDA}	Chip Supply Voltage	ADC disabled; see registers 0x0C, 0x41, and "ADC DC Specifications" on page 7	3.0	3.3	3.6	V
V_{SL}	Voltage Applied to Digital Bus	(1.8V or 3.3V); see Reg 0x08 Bits 6 and 7	1.6		3.6	V
I_{S-DIS}	Supply Currents	Disable mode			10	µA
I_{S-ENA}	Supply Currents	Total supply current (VDDA, VDD) when chip is enabled, DACs disabled: Reg 0x06,0x07 = 0x01		0.78	0.90	mA
I_{S-ENA}	Supply Currents	Three outputs enabled mode 0; All Reg. set to default value except: Reg. 0x10 = 0x90; Reg. 0x14,0x24,0x34 = 0x18; Reg. 0x11,0x21,0x31 = 0x90; Reg. 0x13,0x23,0x33 = 0xFF		37	48	mA
I_{S-ENA}	Supply Currents No Bias	Three outputs enabled mode 0; All Reg. set to default value except: Reg. 0x10 = 0x90; Reg. 0x14,0x24,0x34 = 0x00; Reg. 0x11,0x21,0x31 = 0x90; Reg. 0x13,0x23,0x33 = 0xFF		12	19	mA
I_{S-ENA}	Supply Currents Low Bias	Three outputs enabled mode 0; All Reg. set to default value except: Reg. 0x10 = 0x90; Reg. 0x14,0x24,0x34 = 0x01; Reg. 0x11,0x21,0x31 = 0x90; Reg. 0x13,0x23,0x33 = 0xFF		14	22	mA
I_{S-ENA}	Supply Currents High Bias	Three outputs enabled mode 0; All Reg. set to default value except: Reg. 0x10 = 0x90; Reg. 0x14,0x24,0x34 = 0x1F; Reg. 0x11,0x21,0x31 = 0x90; Reg. 0x13,0x23,0x33 = 0xFF		60	82	mA

DC Electrical Specifications

Unless otherwise indicated, all of the following tables are: $V_{DD}A = V_{DD} = 3.3V$, $R_{SET} = 10k\Omega$, $T_A = +25°C$. **(Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$V_{DD-GOOD}$	V_{DDA} Voltage Above Which STATUS: Power Good = 1		2.1		2.4	V
V_{SIH}	Input Logic High Level	D[14:0], CLK, RTZ inputs, SYNC	$0.7V_{SL}$			V
V_{SIL}	Input Logic Low Level	D[14:0], CLK, RTZ inputs, SYNC			$0.3V_{SL}$	V
V_{IH}	Input Logic High Level	SPI, LOWP inputs	3.1			V
V_{IL}	Input Logic Low Level	SPI, LOWP inputs			0.2	V
V_{OH}	High Level	$I_L = -5mA$, all logic outputs	3.1			V
V_{OL}	Low Level	$I_L = 5mA$, all logic outputs			0.2	V
I_{IH}	Input Current High Level				1	µA
I_{IL}	Input Current Low Level				1	µA

ADC DC Specifications

Unless otherwise indicated, all of the following tables are: $V_{DD}A = V_{DD} = 3.3V$, $R_{SET} = 10k\Omega$, $T_A = +25°C$.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
FULL-SCALE	Voltage Generating Full-scale Code	$3.0 < V_{DDA} < 3.45$	1.1	1.2	1.3	V
DNL	Differential Non-Linearity	$3.0 < V_{DDA} < 3.45$ (Note 11)	-0.5		0.5	LSB
INL	Integral Non-Linearity	$3.0 < V_{DDA} < 3.45$ (Note 12)		0.5		LSB

I_{OUT1}, I_{OUT2} and I_{OUT3} Code 0x000 Current DC Specifications

$V_{DD} = 3.3V$, $V_{DD}A = 3.3V$, $R_{SET} = 10k\Omega$, Color Scale = 0xFF, $T_A = +25°C$, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT1_{ZERO}$ $IOUT3_{ZERO}$	Code 0x000 Output Current	Input COLOR = 0x000, Threshold = 0x00, $V_{IOUTx} = 7.0V$ (Note 10)			10	µA
$IOUT2_{ZERO}$	Code 0x000 Output Current	Input COLOR = 0x000, Threshold = 0x00, $V_{IOUT2} = 3.6V$ (Note 10)			2	µA

I_{OUT1} and I_{OUT3} COLOR DACs Specifications

$V_{DD} = 3.3V$, $V_{DD}A = 3.3V$, $R_{SET} = 10k\Omega$, $V_{IOUT1} = 1V$, $V_{IOUT3} = 1V$, Color Scale = 0xFF, Bias = 0x1F, $T_A = +25°C$, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT_{MAX}$	Full Scale Output Current	Input COLOR = 0x3FF, $V_{IOUTx} = 500mV$	450	560	700	mA
		Input COLOR = 0x3FF, $V_{IOUTx} = 1V$	500	630	750	mA
t_{RISE}	Rise Time	10% to 90% of zero to 200mA @ 1V headroom; $R_{LOAD} = 4.3\Omega$		2.3		ns
t_{FALL}	Fall Time	90% to 10% of 200mA to zero @ 1V headroom; $R_{LOAD} = 4.3\Omega$		1.0		ns
t_{DELAY}	Time Delay	From CLK falling at 50% to I_{OUT1} and I_{OUT3} at 50% RTZ disabled, mode = 0, CLK = 37.5MHz (Mode 0,1: pipeline on, latency = 8 clock periods; pipeline off, latency = 2 clock periods Mode 2: pipeline on, latency = 10 pixel clock periods)		5.95		ns
DNL	Differential Non-Linearity	(Note 11)	-1		1	LSB
INL	Integral Non-Linearity	(Note 12)		5.2		LSB

I_{OUT2} COLOR DAC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT2} = 1V, Color Scale = 0xFF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT_{MAX}$	Full Scale Output Current	Input COLOR = 0x3FF, V_{IOUT2} = 500mV (Note 10)	650	800	950	mA
		Input COLOR = 0x3FF, V_{IOUT2} = 1V (Note 10)	700	860	1000	mA
t_{RISE}	Rise Time	10% to 90% of zero to max @ 1V headroom; R_{LOAD} = 2Ω		2.0		ns
t_{FALL}	Fall Time	90% to 10% of max to zero @ 1V headroom; R_{LOAD} = 2Ω		2.0		ns
t_{DELAY}	Time Delay	From CLK rising to I_{OUT2} at 50%, RTZ disabled, mode = 0, CLK = 37.5MHz (Mode 0,1: pipeline on, latency = 8 clock periods; pipeline off, latency = 2 clock periods Mode 2: pipeline on, latency = 10 pixel clock periods)		6.37		ns
DNL	Differential Non-Linearity	(Note 11)	-1		1	LSB
INL	Integral Non-Linearity	(Note 12)		8.0		LSB

I_{OUT1} and I_{OUT3} Color Scale DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT1} = 1V, V_{IOUT3} = 1V, Input COLOR = 0x3FF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
SCALER-RANGE	Scaler DAC range		0%		100%	$I_{OUT\ MAX}$
DNL	Differential Non-Linearity	(Note 11)	-1		1	LSB
INL	Integral Non-Linearity	(Note 12)		3.8		LSB

I_{OUT2} Color Scale DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT2} = 1V, Input COLOR = 0x3FF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
SCALER-RANGE	Scaler DAC range		0%		100%	$I_{OUT\ MAX}$
DNL	Differential Non-Linearity	(Note 11)	-1		1	LSB
INL	Integral Non-Linearity	(Note 12)		3.4		LSB

I_{OUT1} and I_{OUT3} THRESHOLD DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT1} = 1V, V_{IOUT3} = 1V, Threshold Scale = 0xFF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT_{MAX}$	Full-scale Output Current	Threshold = 0xFF, V_{IOUTx} = 500mV	240	280	340	mA
$IOUT_{MAX}$	Full-scale Output Current	Threshold = 0xFF, V_{IOUTx} = 1V	270	320	380	mA
DNL	Differential Non-Linearity	(Note 11)	-0.5		0.5	LSB
INL	Integral Non-Linearity	(Note 12)		1.4		LSB

I_{OUT2} THRESHOLD DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT2} = 1V, Threshold Scale = 0xFF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT_{MAX}$	Full-scale Output Current	Threshold = 0xFF, V_{IOUT2} = 500mV	250	290	340	mA
$IOUT_{MAX}$	Full-scale Output Current	Threshold = 0xFF, V_{IOUT2} = 1V	250	310	360	mA
DNL	Differential Non-Linearity	(Note 11)	-0.5		0.5	LSB
INL	Integral Non-Linearity	(Note 12)		1.4		LSB

I_{OUT1} and I_{OUT3} Threshold Scale DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT1} = 1V, V_{IOUT3} = 1V, THRESHOLD = 0xFF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
THRESHOLD-SCALE-RANGE	Threshold scale DAC range	Gain adjustment range over all segments	30%		100%	$I_{OUT\ MAX}$
DNL	Differential Non-Linearity	(Note 11)	-1.5		1.5	LSB
INL	Integral Non-Linearity	(Note 12)		0.5		LSB

I_{OUT2} Color Segment DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT2} = 1V, Color Scale = 0xFF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
GAIN-SEGMENT-RANGE	Gain range for segment DAC		50%		150%	$I_{OUT\ MAX}$
DNL	Differential Non-Linearity	(Note 11)	-2.0		2.0	LSB
INL	Integral Non-Linearity	(Note 12)		0.6		LSB

I_{OUT2} Threshold Scale DAC DC Specifications

V_{DD} = 3.3V, $V_{DD}A$ = 3.3V, R_{SET} = 10kΩ, V_{IOUT2} = 1V, THRESHOLD = 0xFF, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
THRESHOLD-SCALE-RANGE	Threshold scale DAC range	Gain adjustment range over all segments	30%		100%	$I_{OUT\ MAX}$
DNL	Differential Non-Linearity	(Note 11)	-1.0		1.0	LSB
INL	Integral Non-Linearity	(Note 12)		0.5		LSB

Pixel Data Input Interface AC Performance

Unless otherwise indicated, V_{DD} = 3.3V, R_{SET} = 10kΩ, T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
F_{CLK01}	Input Data Clock Frequency	mode 0 and 1 Frequency is input mode dependent. See “Input Pixel Data Interface” on page 11 for details.			100	MHz
F_{CLK2}	Input Data Clock Frequency	mode 2 Frequency is input mode dependent. See “Input Pixel Data Interface” on page 11 for details.			150	MHz
Duty	Input Data Clock “H” Duty Cycle		45	50	55	%
t_{DS}	Data Setup Time to CLK Edge	V_{SL} = 1.8V, Reg. 0x08 : bits[7..6] = 00b, RT,SYNC,CLK,D[14:0]	0.85			ns
t_{DH}	Data Hold Time to CLK Edge	V_{SL} = 1.8V, Reg. 0x08 : bits[7..6] = 00b, RT,SYNC,CLK,D[14:0]	0.95			ns

Pixel Data Input Interface AC Performance

Unless otherwise indicated, V_{DD} = 3.3V, R_{SET} = 10kΩ, T_A = +25°C. **(Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
t_{DS}	Data Setup Time to CLK Edge	V_{SL} = 3.3V, Reg. 0x08 : bits[7..6] = 11b, RT,SYNC,CLK,D[14:0]	1.0			ns
t_{DH}	Data Hold Time to CLK Edge	V_{SL} = 3.3V, Reg. 0x08 : bits[7..6] = 11b, RT,SYNC,CLK,D[14:0]	1.0			ns

Mode 3 Pixel Input Timing Specifications

V_{DD} = 3.3V, R_{SET} = 10kΩ, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
t_{Iout_EN}	Individual Channel Enable Pulse Width		10			ns
t_{Iout_ON}	Time from Channel Enable to I_{OUT} Reaching Maximum Intensity of Programmed Value		10			ns
t_{Iout_OFF}	Time From Channel Disable to I_{OUT} = 0mA, Completely Turned Off				100	ns

SPI Serial Interface AC Performance

V_{DD} = 3.3V, R_{SET} = 10kΩ, T_A = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
F_{SER}	SCLK Operating Range	Static logic not limited at low frequency			40	MHz
t_{EL}	SEN “Low” Time	@ 40MHz (Note 8)	50			ns
t_{ERSR}	SEN Rising Edge to the First SCLK Falling Edge	@ 40MHz (Note 8)	6.25			ns
t_{CDS}	SDIO Set Up Time	@ 40MHz (Note 8)	5			ns
t_{CDH}	SDIO Hold Time	@ 40MHz (Note 8)	5			ns
t_{SREF}	Last SCLK Rising Edge to SEN Falling Edge	@ 40MHz (Note 8)	6.25			ns
t_{CC}	SCLK Cycle Time	@ 40MHz (Note 8)	25			ns
t_{CL}	Clock Low Time	@ 40MHz (Note 8)	13			ns
t_{CH}	Clock High Time	@ 40MHz (Note 8)	6			ns
t_{CDD}	SDIO Output Delay	@ 40MHz (Note 8)		6		ns

NOTES:

8. See Figures 17 and 18 for SPI Read/Write Timing Diagram.
9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. Applied voltage at I_{OUTx} assumes some level of voltage drop across the laser diode
11. Differential non-linearity (DNL) is the difference between the measured and ideal 1 LSB change of any two adjacent codes.
12. Integral Non Linearity (INL) is the maximum deviation between the ideal and actual output levels of a DAC. Ideal output levels are calculated along a line passing through zero and full scale to remove the effects of gain and offset.

Block Diagram

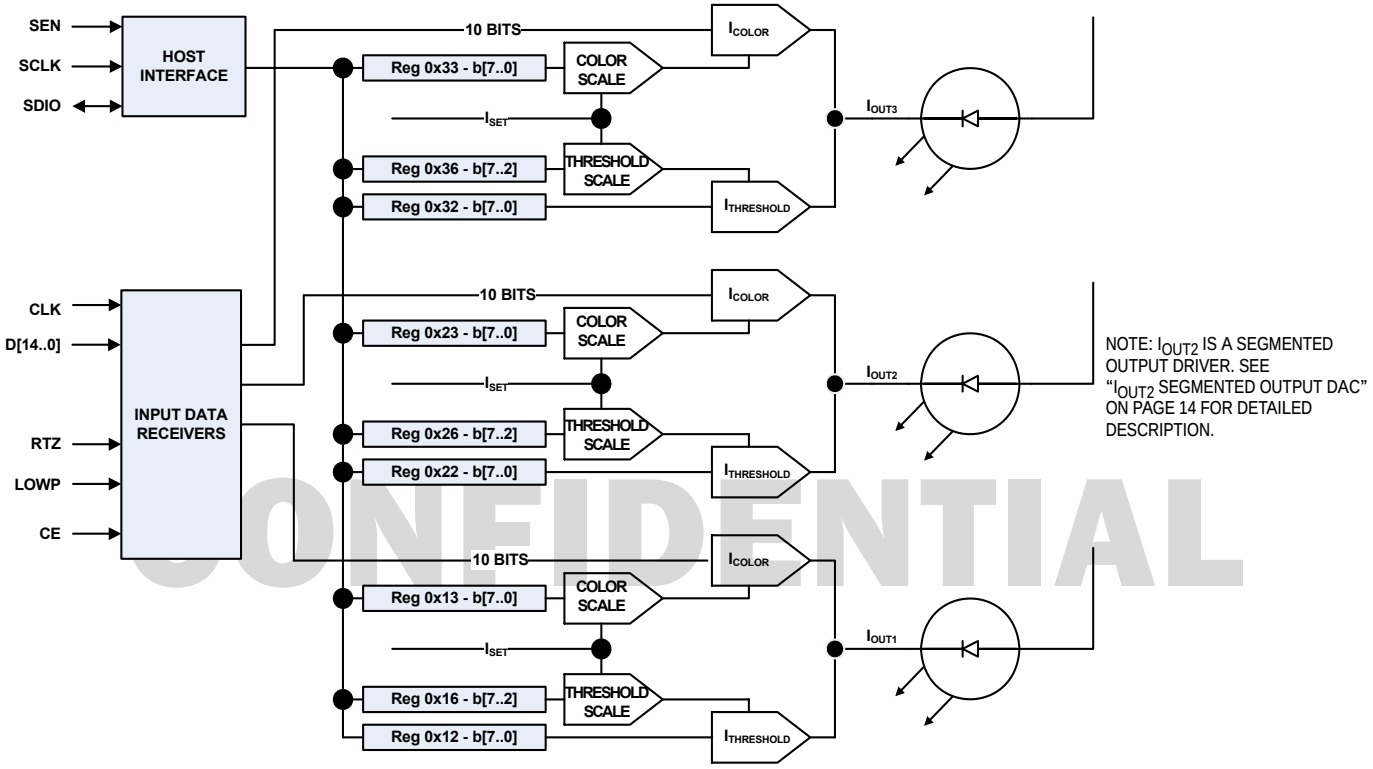


FIGURE 3. ISL58315 BLOCK DIAGRAM

Functional Description

Power-On Reset

Built into ISL58315 is a power-on reset circuit. Once power is applied, the device self-generates an internal reset, and all registers are loaded with their default values. Additionally, a power-good bit in Register 0x0F Bit 0 reports that the device has detected a good operating power supply.

Should the power to the device drop, or should the register state become uncertain for any other reason, then setting Bit 7 of Register 0x07 from low to high will reset all LDD registers to their default states.

Chip Enable

The ISL58315 is enabled when the CE pin is asserted high. When de-asserted, this pin disables the chip. During disable, the SPI interface remains active, thus allowing host access to the internal registers.

This signal is internally ANDed with Reg 0x07 Bit 0 (chip enable bit). Both must be asserted for the chip to operate.

Toggling the chip enable pin (CE) does not reset the register values to their defaults.

Input Pixel Data Interface

The input pixel data interface is a parallel 15-bit-wide bus. It accepts packed RGB pixel data formats, depending on the input mode selected in Register 0x08 Bits[1:0]. There are four data modes.

Upon power-on reset, the laser diode driver defaults to data mode 0. The host must program the data mode select Register 0x08 Bits 1-0 to enable the device to operate in other modes. This can be accomplished during the power-on initialization phase in the total system.

Each I_{OUT} channel takes a 10-bit pixel value. Depending on the mode, the 10-bit pixel data is either packed in 5 bits/rising and 5 bits/falling or 10 bits/clock edge format. See the data mode sections beginning on page 11 for details.

DATA CLOCK

Clock (CLK) is the input data clock used to latch in the RGB pixels. Both edges of the data clock are used. The rising edge is always the first data, followed by the falling edge.

Following are descriptions of each of four data modes, the corresponding RGB data packing order, and the relationship with the input data clock.

DATA MODE 0

Input Data Mode 0 uses all 15 bits (D14 – D0) of the physical data bus (Figure 4). The physical input pixel data interface is separated into three 5-bit buses; one for each of the I_{OUT1}, I_{OUT2} and I_{OUT3} channels.

The 10-bit pixel data is separated into two 5-bit nibble bytes. The MSB nibble byte is latched on the rising edge of clock. The LSB

nibble byte is latched on the falling edge of clock. Thus, in one clock cycle, the full 10-bit pixel data is latched into the LDD.

The alignment of the MSB bit of each nibble byte must align to D4, D9 or D14, depending on which I_{OUT} channel is used. D4 is the MSB of I_{OUT3} nibbles, D9 is the MSB of I_{OUT2} nibbles, and D14 is the MSB of I_{OUT1} nibbles.

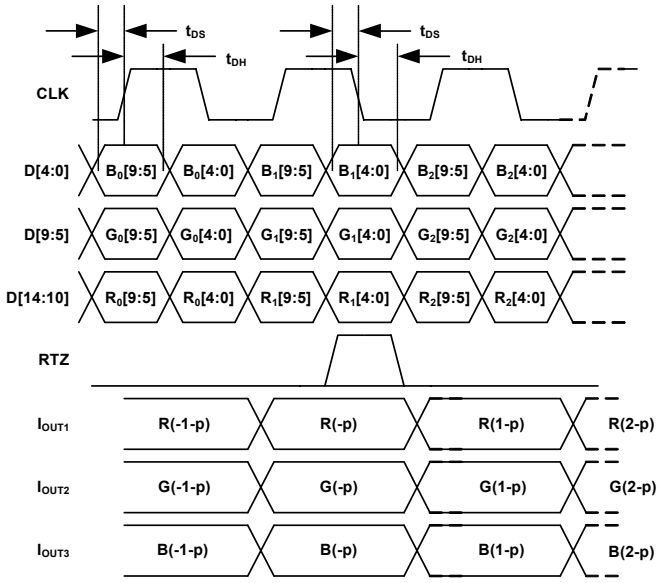


FIGURE 4. DATA MODE 0 TIMING DIAGRAM (p = 2 OR 8 WHEN BIT[3] OF REG. 0X08 IS 1 OR 0, RESPECTIVELY)

DATA MODE 1

Input Data Mode 1 uses all 15 bits (D14 – D0) of the physical data bus (Figure 5). The physical input pixel data interface is separated into three 5-bit buses; one for each of the I_{OUT1}, I_{OUT2} and I_{OUT3} channels. I_{OUT} channel's 10 bits of pixel data is separated into two 5-bit nibble bytes.

On the rising edge of the clock, I_{OUT2} 5-bit MSB nibble and 10-bit of I_{OUT3} are latched by the interface. On the falling edge of the clock, I_{OUT2} 5-bit LSB nibble and 10-bit of I_{OUT1} are latched into the interface. I_{OUT2} MSB and LSB nibble are aligned with D9 – D5 while I_{OUT1} and I_{OUT3} 10-bit data are aligned with D4 – D0 for LSB part and D14 – D10 for the MSB part.

DATA MODE 2

Input Data Mode 2 uses 10 bits (D9 – D0) of the physical data bus (Figure 6). Each I_{OUT} channel's 10 bits of input pixel data is aligned to D9 – D0 and is latched at each edge of the pixel clock. D10 of the pixel bus is used as the SYNC input signal.

The latching order of I_{OUT} channel data is I_{OUT1}, I_{OUT2} and I_{OUT3}. The data is latched beginning with the rising edge of clock.

A SYNC pulse is used to indicate completion of the data transfer for each group of three I_{OUT} channels. During the first rising edge of the clock, a SYNC pulse must be generated, and subsequently, a SYNC pulse is generated on every third clock edge. The SYNC pulse must satisfy the same setup and hold time as I_{OUT3} data relative to the pixel clock.

Internal to the LDD chip, the first SYNC pulse is used to align the internal buffers, and the data in the pile is ignored. The falling edge of the SYNC pulse signifies to the LDD to present the data to the output channels.

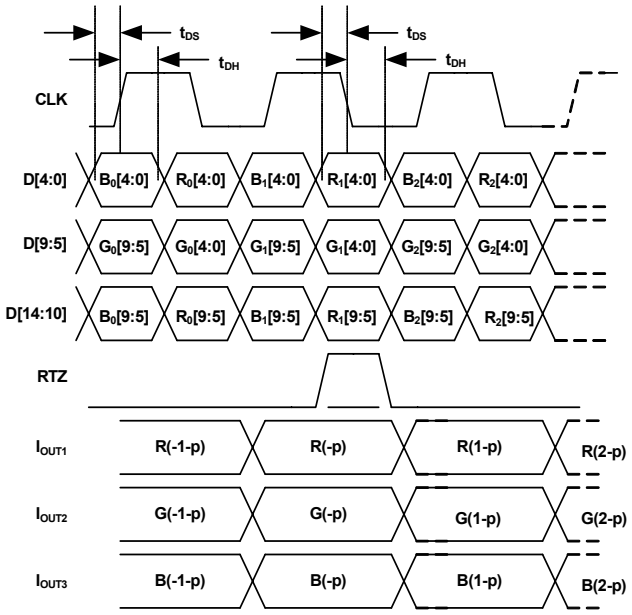


FIGURE 5. DATA MODE 1 TIMING DIAGRAM (p = 2 OR 8 WHEN BIT[3] OF REG. 0X08 IS 1 OR 0, RESPECTIVELY)

DATA MODE 3 (LCOS MODE)

Input Data Mode 3 is designed to support field sequential display imaging devices such as DLP and LCOS (Figure 7). In this mode, each channel's pixel data is written into its corresponding register and is presented when its corresponding enable (ENx) signal is asserted.

To enter this mode, Register 0x08 Bits[1:0] must be set to 11b and Bit[3] must be set to 1b.

Each channel's color DAC data is written to 0x1E/0x1F registers for I_{OUT1}, 0x2E/0x2F registers for I_{OUT2} and 0x3E/0x3F registers for I_{OUT3}.

Pin 7 (D6) is the EN1 signal that enables I_{OUT1} channel output. Pin 5 (D4) is the EN2 signal that enables I_{OUT2} channel output, and Pin 3 (D2) is the EN3 signal that enables I_{OUT3} channel output.

In this mode, there is no input clock. The CLK pin should be tied to ground with a high-impedance resistor of 100K.

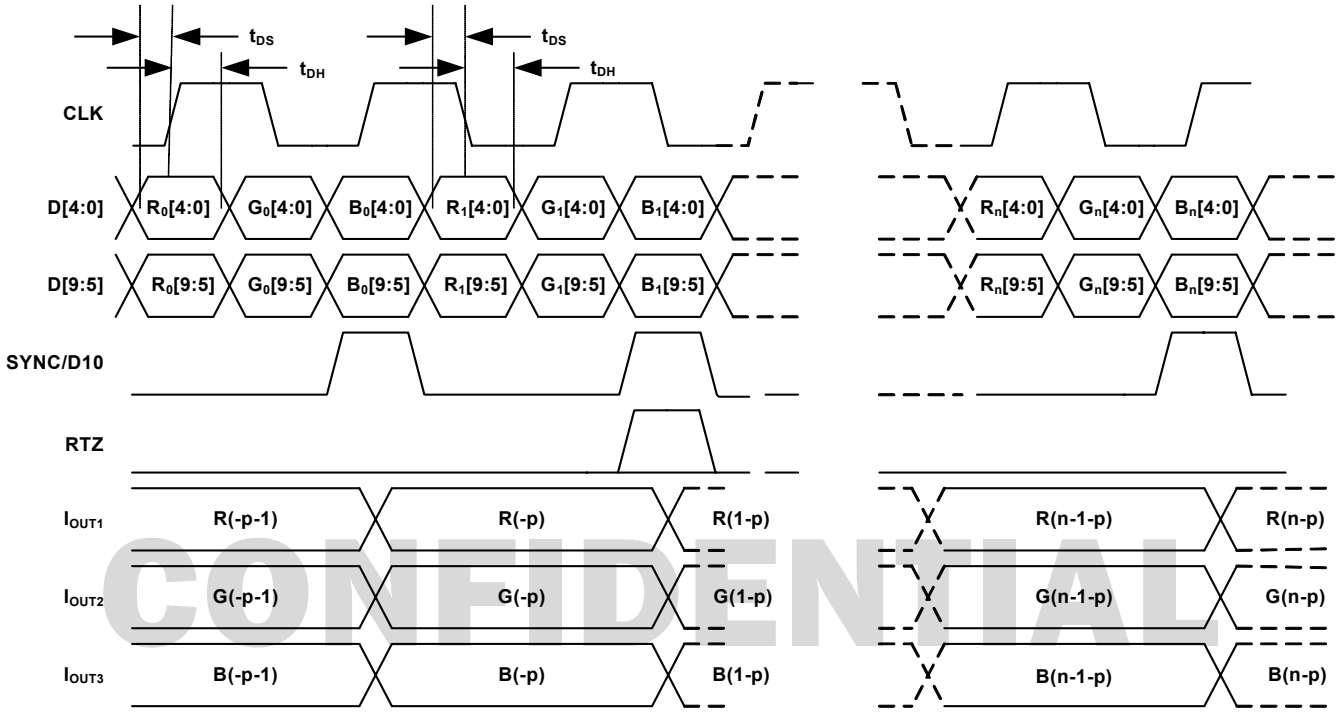


FIGURE 6. DATA MODE 2 TIMING DIAGRAM (p = 2 OR 8 WHEN BIT[3] OF REG. 0X08 IS 1 OR 0, RESPECTIVELY)

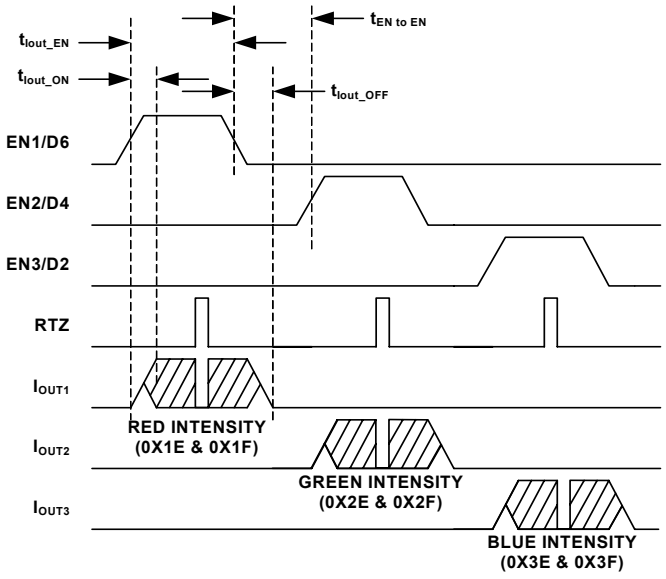


FIGURE 7. DATA MODE 3 TIMING DIAGRAM

I_{OUT} Output Enable

The outputs are enabled by the ENA pin and the Enable register bits. In addition, the LOWP pin, when high, allows the output currents to be turned off, along with some bias currents, to save power at the ends of the horizontal or vertical sweeps. The RTZ pin, when raised, turns off selected colors for a programmable fraction of the CLK interval.

I_{OUT1} and I_{OUT3} Output DAC

Refer to Figures 8 and 9 for block diagrams of the I_{OUT1} and I_{OUT3} N-MOS output DACs. Output Channel 1 and Output Channel 3 DAC structures are identical, but each is programmed by its own registers.

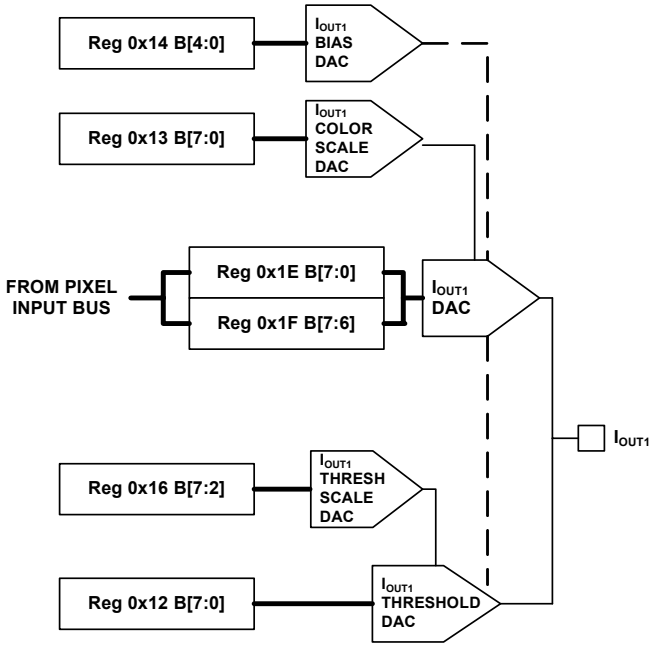


FIGURE 8. I_{OUT1} N-MOS OUTPUT DAC BLOCK DIAGRAM

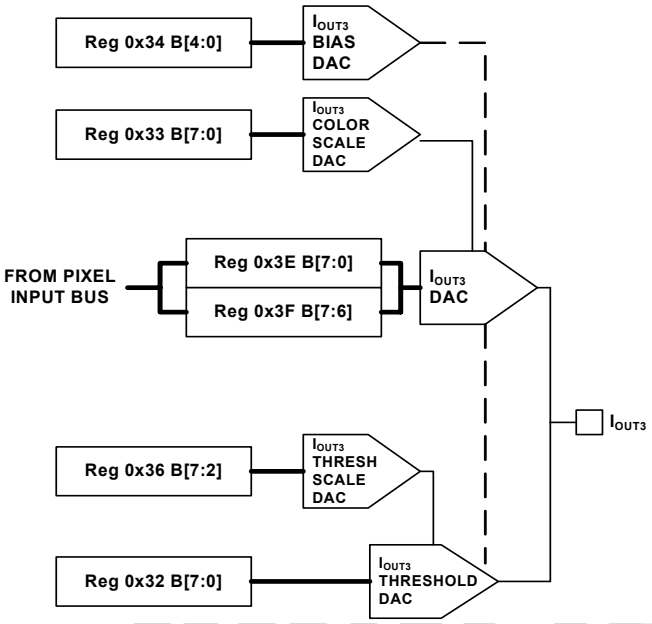


FIGURE 9. I_{OUT3} N-MOS OUTPUT DAC BLOCK DIAGRAM

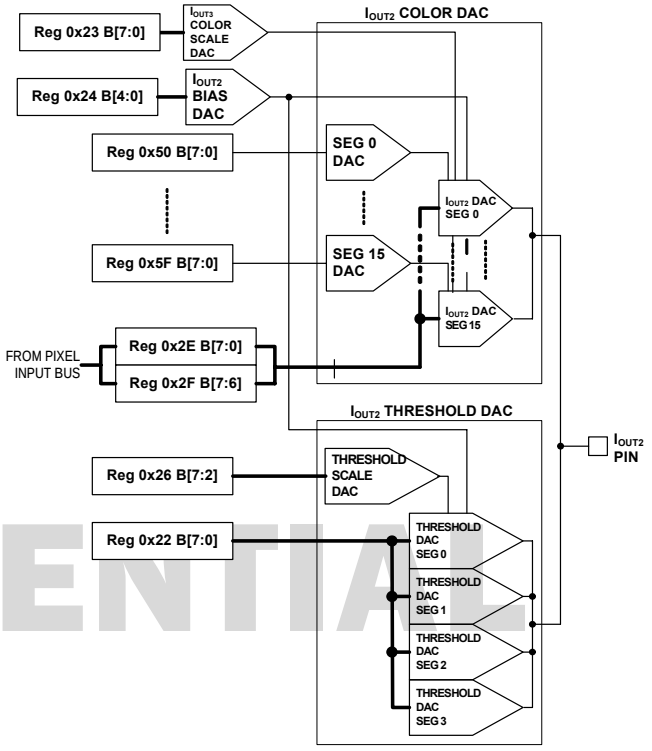


FIGURE 10. I_{OUT2} N-MOS SEGMENT DAC BLOCK DIAGRAM

Threshold DAC

The threshold DAC is made up of two DACs: a threshold DAC and a threshold scale DAC.

Color DAC

The color DAC is made up of two DACs: a color DAC and a color scale DAC. The two DACs set the output current that drives the laser.

Color DAC Output Current

Following is the equation used to calculate the current output on each of the I_{OUT} channels. Equation 1 uses a register setting combined with the parallel interface data:

$$I_{MAX} = [(512b9 + 256b8 + 128b7 + 64b6 + 32b5 + 16b4 + 8b3 + 4b2 + 2b1 + b0)/1023] * \text{Color Scale} \quad \text{(EQ. 1)}$$

where

- b9 to b0 are the parallel interface bits
- Color Scale is each channel's Color scale registers (Registers 0x13, 0x23, and 0x33).

I_{OUT2} Segmented Output DAC

The I_{OUT2} N-MOS output channel has a similar construction to I_{OUT1} and I_{OUT3} (Figure 10). It is made up of a color DAC and a threshold DAC. However, the color and threshold DACs are segmented. The color DAC is divided into 16 segments and the threshold DAC into 4 segments.

The gain of each segment of color DAC is set by linearity registers. In this manner, the color DAC is capable of making a piece-wise linear approximation of the laser sensitivity. In addition, the reference input of all segment gain DACs is set by a slope DAC for each color. Thus, the overall gain of each color can be programmed.

Output Channel Bias Current Programmability

The bias current of each I_{OUT} channel is programmable via a register (0x14, 0x24, 0x34 for I_{OUT1}, I_{OUT2}, I_{OUT3} respectively). Bit[4] of this register adjusts the accuracy vs. power trade-off by setting an internal current mirror ratio. It yields higher accuracy, when it is set to 1, and lower power dissipation, when it is set to 0. Bit[3:0] adjust the power vs. speed trade-off by setting the bias currents that drive the output DACs. 16 binary decoded settings are available, ranging from 0x0 (resulting in lowest power dissipation and slowest response, intended for use in low speed applications such as field sequential ones) to 0xF (resulting in highest power dissipation and fastest response). The "DC Electrical Specifications" on page 6 summarize the effect of the bias current register value on power, while Figure 25 illustrates its effect on speed.

Power Saving Operation (LOWP Signal)

LOWP is an active high signal. When asserted by a host, it places the LDD into sleep mode. During sleep mode, there is no current output. All COLOR DACs, the threshold DAC and the bias DAC are set to zero. All register values are retained during sleep mode.

Recovery from LOWP mode is much quicker than recovery from the disabled state. From de-assertion of LOWP to full recovery, the LDD typically takes 150ns. It is important to conserve power during line-to-line blanking or frame-to-frame blanking transition times.

Look-ahead Pipeline

The look-ahead pipeline is a feature designed to assist power saving based on incoming pixel data. When enabled, the DAC bias current is adjusted based on incoming data. For I_{OUT1} and I_{OUT3}, it reduces the power when the input data is zero. For I_{OUT2}, it turns the segments ON or OFF according to the incoming data.

The look-ahead sleep mode is enabled by setting Register 0x08, Bit 3, to zero (default); when this feature is enabled a latency of 6 cycles is added to the output delay. This feature must be disabled for Mode 3 input to function.

Integrated Sampler Circuit

The purpose of the sampler circuit is to allow the system to sample the voltage level of the desired output DAC at a pre-programmed current. Registers 0x0B and 0x0C are used to configure, control and enable the sampler circuit.

NOTE: If a sampler circuit is used, the VDDA tolerance must be between 3.0V and 3.45V.

Sampler Operation

The target current level is a 10-bit digital value and can be equal to or less than the maximum pixel intensity value. Thus, a maximum of 0x3FF can be programmed into sampler trigger Register 0x0B and 0x0C bit[1:0]. The upper 8 bits are stored in Register 0x0B, and the lower two significant bits are stored in 0x0C bit[1:0]. A sample is made when the selected DAC is driven by the target code in one-shot mode.

Once the target current level is programmed, the target DAC output channel must be selected. The selection is made by programming the sampler control register, 0x0C bit[3:2].

The default gain setting of the sampler circuit is 1/4. If the gain needs to be increased, Register 0x0C bit[5:4] allows additional increments of 1/4, up to a maximum gain of 1.

The last configuration before enabling the sample circuit for operation is to select the sampling mode. There are two modes: continuous or single shot.

Continuous mode is selected when Register 0x0C bit[6] is set to 1. The sampler circuit continuously samples the selected DAC output channel when the sample enable bit Register 0x0C bit[7] is set to 1. The sampler stops when the sample enable bit is reset to 0.

Single-shot mode is selected when Register 0x0C bit[6] is set to 0. The sampler circuit samples the selected DAC output channel once. At the completion of the sample, Register 0x0C bit[7] is automatically reset to zero.

ADC/Peak Detection Circuit

Figure 11 shows the integrated ADC and peak detection block diagram. The ADC and peak detection circuit is part of the sampler circuit. Working together, they enable the sampler circuit to automatically detect the highest or lowest value.

The ADC is controlled via Registers 0x41 and 0x42.

The peak detection circuit is a simple digital comparator. It is used in conjunction with the sampler and the ADC circuit to check the desired DAC output channel's voltage. Knowing the output voltage, a system can externally adjust the supply voltage; for example, to minimize the headroom used, thus enabling power savings.

The peak detection circuit is controlled via Register 0x42.

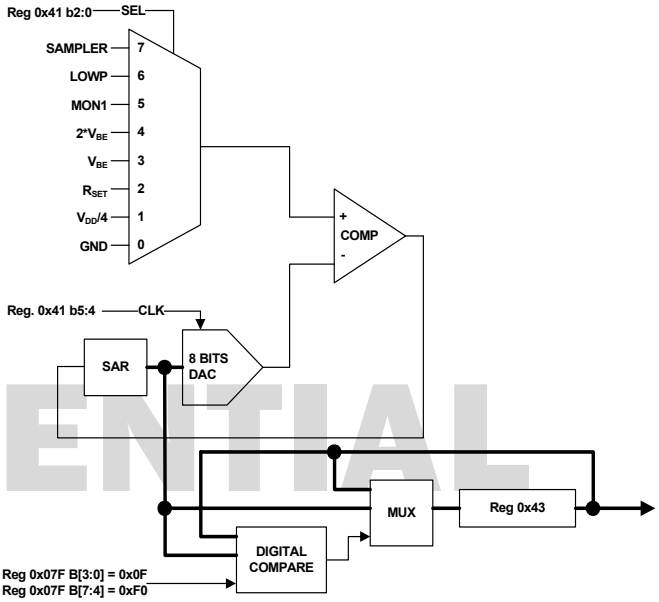


FIGURE 11. ADC AND PEAK DETECTION BLOCK DIAGRAM

Thermal Shutdown

A thermal shutdown circuit is included in the ISL58315 laser diode drivers. Its intent is to prevent the laser diode driver from becoming overheated during normal operation.

A thermal sensor that monitors the die temperature reports the die temperature to the temperature data register, 0x4E. This value can be retrieved by the host controller via the SPI serial interface.

NOTE: An increasing temperature returns a smaller binary value. A decreasing temperature returns a larger binary value.

SHUTDOWN

The thermal shutdown register is 0x4C. The default value represents an equivalent temperature of +150°C. The LDD shuts down if the value of the thermal shutdown register, 0x4C, is greater than the value in the temperature data register, 0x4E.

RECOVERY

After a shutdown event, the LDD recovers automatically. Automatic recovery is achieved via the internal thermal shutdown circuit by comparing the thermal recovery register, 0x4D, to the temperature data register, 0x4E. A default value equivalent to +135°C is programmed into the device. If Register 0x4E is greater than Register 0x4D, then the LDD can resume operation.

WARNING: It is not recommended to override the default value to force the device to operate at a higher temperature. This could lead to possible damage of the device.

Return-to-Zero Function and RTZ Signal

The return-to-zero function allows the LDD to force zero output current to each laser for a short period of time. This function allows projection systems to momentarily destabilize the coherency of the laser. It is an electrical means of assisting projection systems that use laser as a light source. Along with other optical components, return-to-zero enhances, and in some cases, nearly eliminates the speckle effect of the laser light source.

RTZ SIGNAL

RTZ is a physical signal (pin 39) provided by either a host controller or a display system driver. It is an active high signal. If the return-to-zero function is not desired in a system, this pin should be tied to ground via a resistor. It should never be left floating.

Synchronous and asynchronous RTZ operation, including programming and special conditions, is described in the following sections.

SYNCHRONOUS MODE (INPUT DATA MODES 0 AND 1)

In synchronous mode, the return-to-zero function is highly programmable (Figure 12). Pulse width can be programmed to 1/16 of the pixel clock period. Pulse delay can be programmed to 1/16, 3/16, or 5/16 of the clock period. The RTZ pulse can be enabled for each of the I_{OUT} channels. Programming is set in Register 0x44.

Each of the RTZ current pulses is synchronized with the input pixel clock falling edge (Figure 12). Each time the RTZ signal (pin 39) is asserted, the programmed timing in Register 0x44 is executed on each enabled I_{OUT} channel as programmed by Register 0x44 bit[7:5].

Synchronous mode is recommended for use with pixel data input modes 0 and 1 with an input clock frequency of no higher than 100MHz (pixel period of 10ns) and no lower than 50MHz.

Figure 12 shows two ways of using the RTZ signal (pin 39) to enable the return-to-zero function in the synchronous mode. During N^{th} input pixel time, the RTZ signal is high, with the appropriate setup time relative to CLK. This enables the N^{th} pixel to have the return-to-zero function applied. This method allows selective control of the pixel to which the return-to-zero function is applied.

During the input pixel $N^{th}+3$ to $N^{th}+7$ time, the RTZ signal (pin 39) is asserted high. In this case, the return-to-zero function is applied to every pixel beginning with $N^{th}+3$. This method is an easy way to apply the return-to-zero function to a group of pixels or all pixels.

SYNCHRONOUS MODE (INPUT DATA MODE 2)

In synchronous mode, the RTZ signal functions as an enable signal. If active, a pulse to zero is inserted for the current pixel presented on the input interface. Figure 13 shows the synchronous return-to-zero mode pulse timing diagram for input pixel mode 2.

ASYNCHRONOUS MODE

In asynchronous mode, the RTZ signal is the input pin for the asynchronous RTZ waveform generated by an external controller. The state of the RTZ signal determines when and for how long the return-to-zero function is applied (Figure 14). Internally, the RTZ signal is gated with the pixel data.

Asynchronous mode is recommended for use with input pixel mode 3.

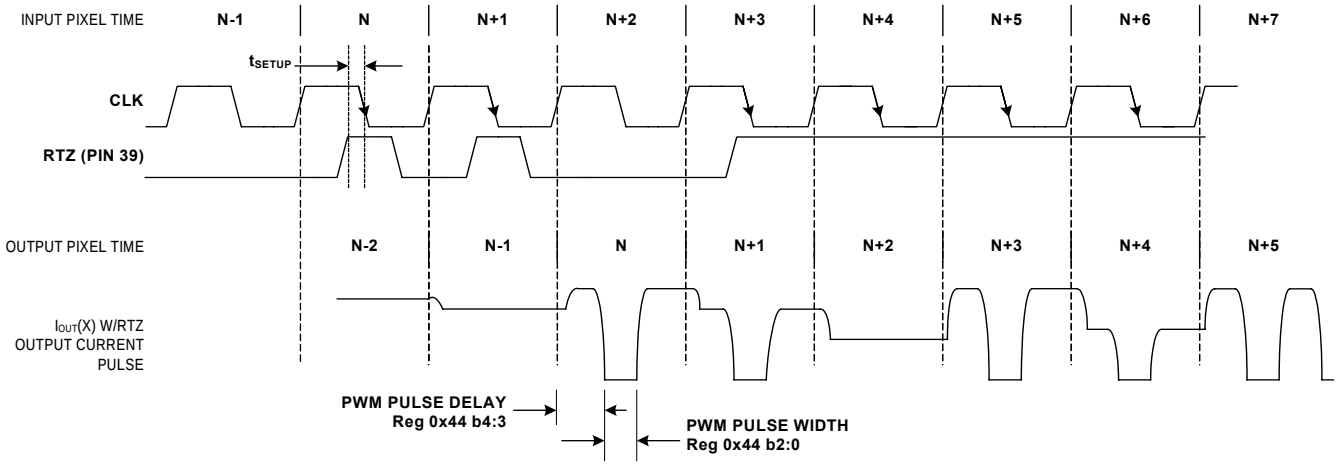


FIGURE 12. SYNCHRONOUS RETURN-TO-ZERO MODE PULSE TIMING DIAGRAM FOR INPUT PIXEL MODES 0 AND 1

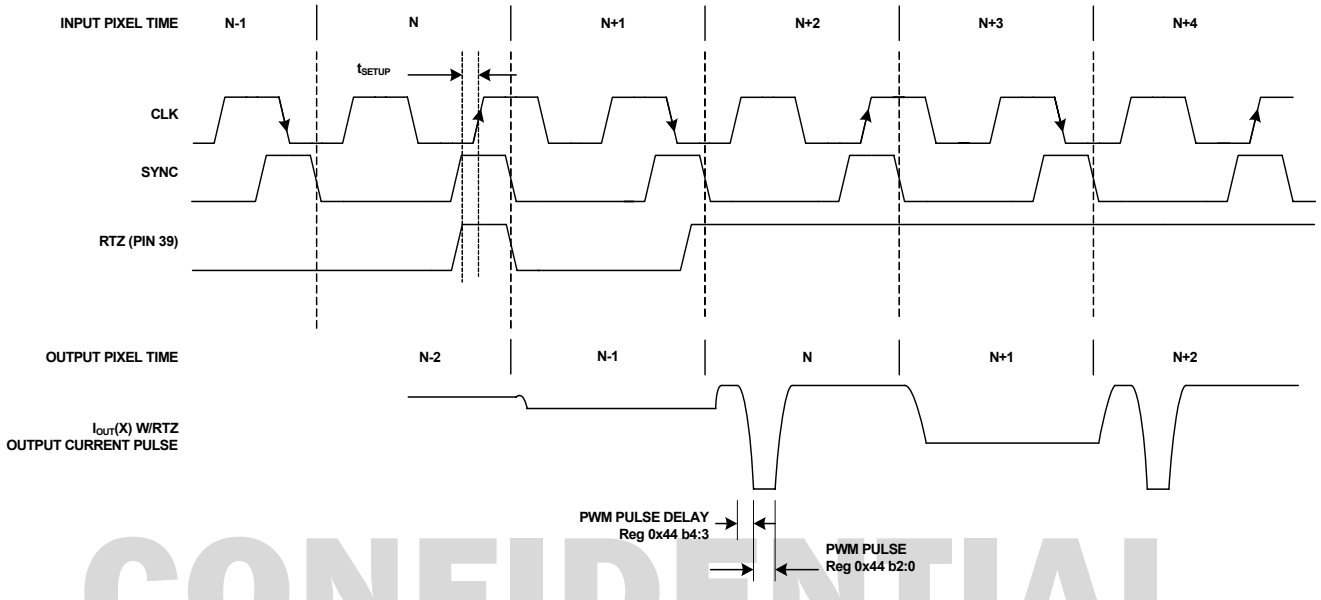


FIGURE 13. SYNCHRONOUS RETURN-TO-ZERO MODE PULSE TIMING DIAGRAM FOR INPUT PIXEL MODE 2

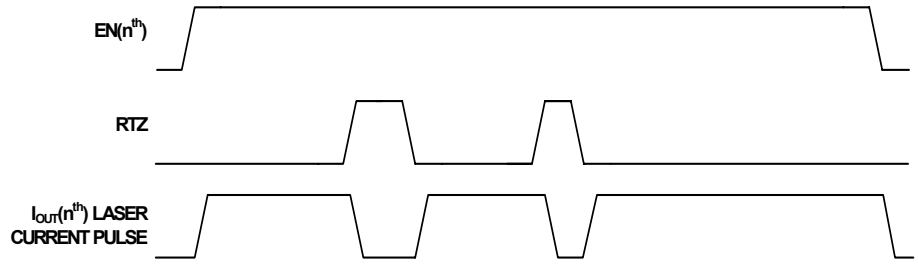


FIGURE 14. ASYNCHRONOUS RETURN-TO-ZERO MODE PULSE TIMING DIAGRAM FOR INPUT PIXEL MODE 3

Heater Control

Some lasers require precise temperature control to obtain optimum optical performance. The ISL58315 LDD integrates a heater circuit that drives a resistive heating control element and monitors temperature by measuring its resistance.

Figure 15 shows the heater control circuit. To measure the resistance of the heating element, a reference current, I_2, is sourced through pin 34 to the heating element. A DAC-controlled current, I_1, is sourced though a reference resistor (pin 33). The voltages on pins 33 and 34 are compared, and the DAC value is adjusted until the voltages are equal.

In steady state, the value in the heater read-back register, 0x4B, varies linearly with the ratio of the heating element resistance over the reference resistor's resistance. A zero code in Register 0x4B occurs when the heating element resistance is half the reference resistance. A maximum code (0xFF) corresponds to a ratio of 1.49. When the heating element resistance is equal to the reference resistance, Register 0x4B reads 0x80.

To achieve maximum range in the resistance measurement, the reference resistor should match the nominal heating element's resistance.

MEASUREMENT ACCURACY VS POWER

Since the heating element's resistance is typically low, large reference currents are needed to accurately measure its resistance. The heater control circuit features a programmable reference current. The reference current is set by Bits 4 and 3 of Register 0x49. Note: a higher current gives higher accuracy in exchange for power consumed.

To further save power, the reference current is periodically pulsed on to measure resistance, and then turned off for a programmable length of time. The off time is controlled by Bits 7 to 5 of Register 0x49, as shown in Table 39. Selecting a higher off time reduces power dissipation at the cost of slower tracking of temperature changes in the heater element.

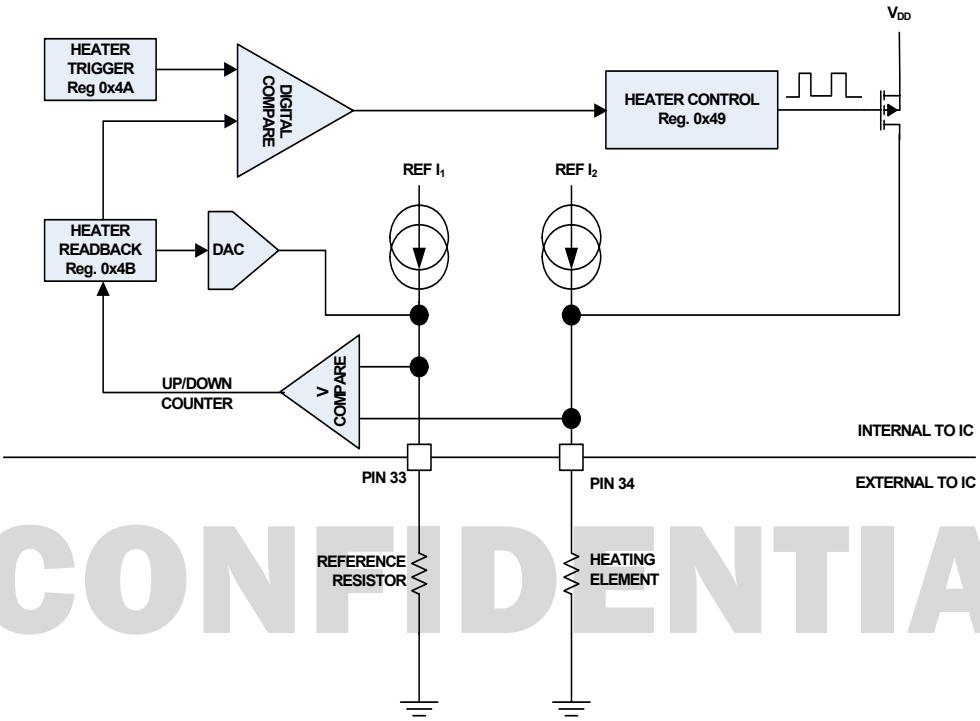


FIGURE 15. HEATER CONTROL CIRCUIT

REGULATING TEMPERATURE

In addition to measuring heater element temperature, the heater control circuit can also regulate the temperature to a desired target. The target heater resistance (and hence temperature) is loaded into Register 0x4A. This target is compared to the actual measured resistance in Register 0x4B. Whenever measured resistance is below target, a switch turns on and forces a current through the heating element, which causes the heating element temperature to increase.

Assuming that the heating element has a positive temperature coefficient, the measured resistance increases until it becomes greater than or equal to the target value. In this state, the heater switch turns off.

The heater circuit turns on and off as the heater temperature ripples around the target value. The magnitude of this ripple can be minimized by selecting shorter off times at the expense of higher power dissipation.

Heating Modes

The heater circuit has five distinct heating modes, which are selected by Bits 2 to 0 of Register 0x49. Table 1 shows all five modes and provides a description of each mode.

MODE 0

In mode 0, the heating circuit is disabled and does not use any power.

MODE 1

In mode 1, the heater control circuit is fully functional. The heating element resistance is constantly monitored. The heater switch is modulated to regulate temperature. The modulated duration and frequency can be programmed in Register 0x49.

MODE 2

In mode 2, the heating element resistance is constantly monitored, but the heating circuit is disabled.

MODE 4

In mode 4, the heating element resistance is constantly monitored, and the heating switch is forced to ON. The heating switch turns off only during pulses, which enables the heater resistance measurement to take place.

TABLE 1. HEATING MODES

BITS 2-0	DESCRIPTION
7	Reserved (not used)
6	Reserved (not used)
5	Heating is fully on
4	Heating cycle is pulsed
3	Reserved (not used)
2	No heating, but ADC is enabled
1	Heating cycle using PWM
0	Disables the heating circuit (default)

MODE 5

In mode 5, the heating element resistance is not monitored, but the heating circuit is continuously on.

MODES 3, 6, AND 7

These modes are reserved. The user should not select these modes.

SPI Serial Interface

The ISL58315 has an SPI serial interface that allows the user access to the internal registers. This interface is a 3-wire, one master/multi-slave protocol.

The three wires are SEN (Serial Enable), which is a high impedance input pin; SCLK (Serial Clock), which is a device high-impedance input pin; and SDIO (Serial Data), which is a bi-directional, tri-state pin.

Multiple SPI devices can share the serial bus (Figure 16). To identify which device is being addressed, a DEN (Device Enable Number) must be sent to enable the target slave.

SERIAL PROGRAMMING

Figures 17 and 18 show the SPI write and read cycle timing diagrams.

NOTE: All host access to the ISL58315 SPI interface must terminate with a read cycle to Reg. 0x03 (this terminates the SPI write access to the device).

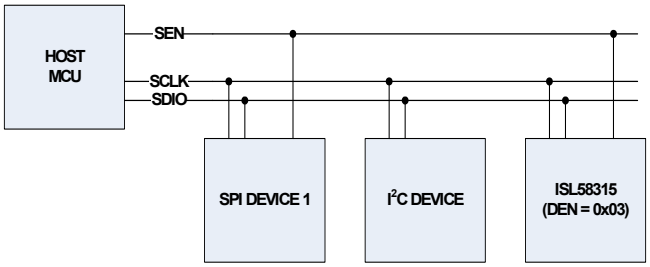


FIGURE 16. SPI INTERFACE TO MULTI-DEVICE SYSTEM

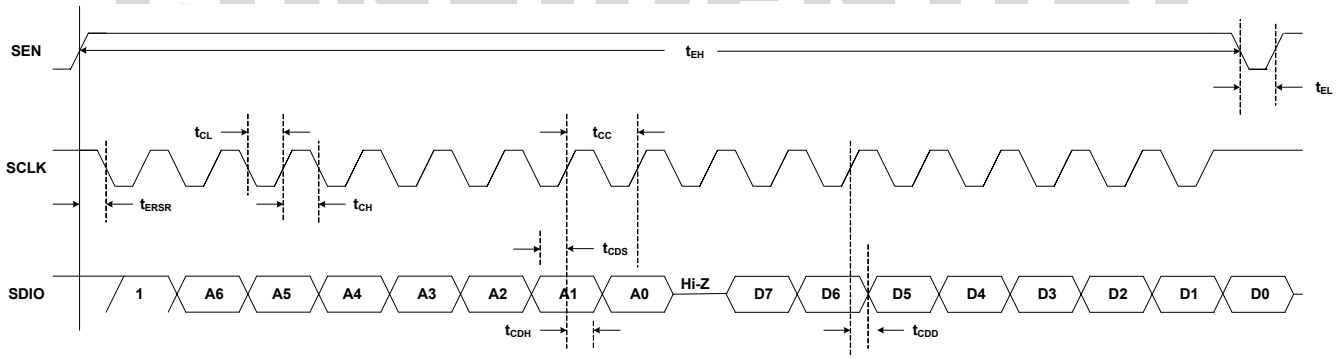


FIGURE 17. SPI SERIAL INTERFACE WRITE CYCLE TIMING DIAGRAM

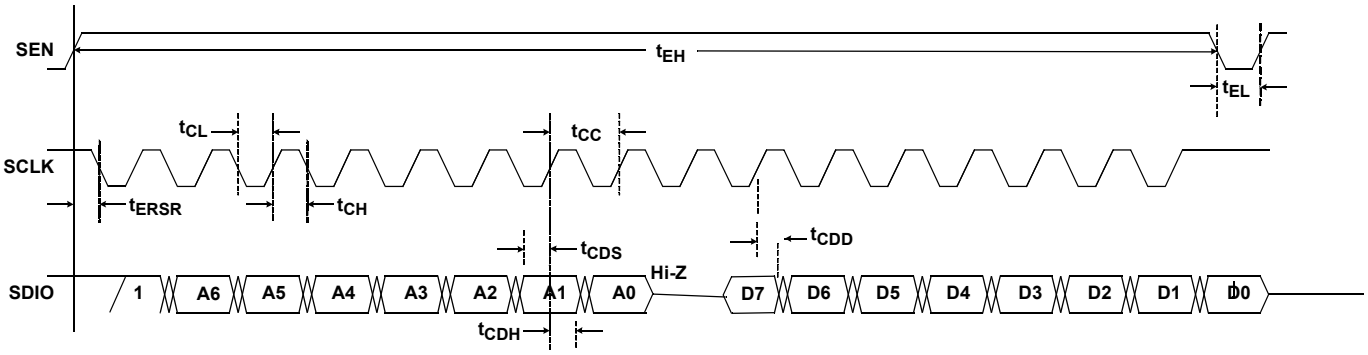


FIGURE 18. SPI SERIAL INTERFACE READ CYCLE TIMING DIAGRAM

Register Map

ADDR	NAME	DESCRIPTION	ACCESS	DEFAULT
0x00	Chip ID	Chip ID	R	0x0F
0x01	Revision ID	Revision ID	R	0x01
0x03	DSR	Device Select Register	R/W	0x00
0x07	Enable Control	Enables various parts of the chip	R/W	0x00
0x08	Data Control	Data Interface Configuration	R/W	0x00
0x0B	Sampler Trigger	Sets the trigger value for sampler circuit	R/W	0x00
0x0C	Sampler Control	Configures and controls the sampler circuit	R/W	0x00
0x0F	Status	Various chip status bits	R	0x00
0x10	I_{OUT1} Control	Configures I_{OUT1} control bits	R/W	0xB0
0x11	I_{OUT1} Threshold Control	I_{OUT1} threshold DAC control	R/W	0x91
0x12	I_{OUT1} I_{THRESH}	I_{OUT1} threshold register	R/W	0x00
0x13	I_{OUT1} Color Scaling	I_{OUT1} color scaling register	R/W	0x00
0x14	I_{OUT1} Bias	I_{OUT1} bias current	R/W	0x18
0x16	I_{OUT1} Threshold Scaling	I_{OUT1} threshold scaling register	R/W	0xFC
0x1E	I_{OUT1} Serial Data MSB	I_{OUT1} serial IO port for MSB	R/W	0x00
0x1F	I_{OUT1} Serial Data LSB	I_{OUT1} serial IO port for LSB	R/W	0x00
0x20	I_{OUT2} Control	Configures I_{OUT2} control bits	R/W	0xB0
0x21	I_{OUT2} Threshold Control	I_{OUT2} threshold DAC control	R/W	0x91
0x22	I_{OUT2} I_{THRESH}	I_{OUT2} threshold register	R/W	0x00
0x23	I_{OUT2} Color Scaling	I_{OUT2} color scaling register	R/W	0x00
0x24	I_{OUT2} Bias	I_{OUT2} bias current	R/W	0x15
0x26	I_{OUT2} Threshold Scaling	I_{OUT2} threshold scaling register	R/W	0xFC
0x2E	I_{OUT2} Serial Data MSB	I_{OUT2} serial IO port for MSB	R/W	0x00
0x2F	I_{OUT2} Serial Data LSB	I_{OUT2} serial IO port for LSB	R/W	0x00
0x30	I_{OUT3} Control	Configures I_{OUT3} control bits	R/W	0xB0
0x31	I_{OUT3} Threshold Control	I_{OUT3} threshold DAC control	R/W	0x91
0x32	I_{OUT3} I_{THRESH}	I_{OUT3} threshold register	R/W	0x00
0x33	I_{OUT3} Color Scaling	I_{OUT3} color scaling register	R/W	0x00
0x34	I_{OUT3} Bias	I_{OUT3} bias current	R/W	0x18
0x36	I_{OUT3} Threshold Scaling	I_{OUT3} threshold scaling register	R/W	0xFC
0x3E	I_{OUT3} Serial Data MSB	I_{OUT3} serial IO port for MSB	R/W	0x00
0x3F	I_{OUT3} Serial Data LSB	I_{OUT3} serial IO port for LSB	R/W	0x00
0x41	ADC Control 0	ADC control 0 register	R/W	0x00
0x42	ADC Control 1	ADC control 1 register	R/W	0x00
0x43	ADC Output (Read Only)	Returns the value of an ADC conversion	R	0x00
0x43	ADC Output (Write Only)	ADC digital data port for writing to various circuits	W	0x00
0x44	RTZ Control	RTZ PWM control register	R/W	0x00
0x49	Heater Control	Configures integrated heater operation modes	R/W	0x00

Register Map (Continued)

ADDR	NAME	DESCRIPTION	ACCESS	DEFAULT
0x4A	Heater Set Point	Sets the heater set point value	R/W	0x00
0x4B	Heater Read Back	Returns a value from the heater circuit	R	0x00
0x4C	High Temp Trip Point	Sets the high temperature trip point limit; default value = +150°C	R/W	0x68
0x4D	Low Temp Trip Point	Sets the low temperature trip point limit; default value = +135°C	R/W	0x6A
0x4E	Temperature	Returns the sensed temperature value	R	0x00
0x50	I_{OUT2} Segment 0	Sets gain adjustment for I_{OUT2} channel segment 0	R/W	0x20
0x51	I_{OUT2} Segment 1	Sets gain adjustment for I_{OUT2} channel segment 1	R/W	0x20
0x52	I_{OUT2} Segment 2	Sets gain adjustment for I_{OUT2} channel segment 2	R/W	0x20
0x53	I_{OUT2} Segment 3	Sets gain adjustment for I_{OUT2} channel segment 3	R/W	0x20
0x54	I_{OUT2} Segment 4	Sets gain adjustment for I_{OUT2} channel segment 4	R/W	0x20
0x55	I_{OUT2} Segment 5	Sets gain adjustment for I_{OUT2} channel segment 5	R/W	0x20
0x56	I_{OUT2} Segment 6	Sets gain adjustment for I_{OUT2} channel segment 6	R/W	0x20
0x57	I_{OUT2} Segment 7	Sets gain adjustment for I_{OUT2} channel segment 7	R/W	0x20
0x58	I_{OUT2} Segment 8	Sets gain adjustment for I_{OUT2} channel segment 8	R/W	0x20
0x59	I_{OUT2} Segment 9	Sets gain adjustment for I_{OUT2} channel segment 9	R/W	0x20
0x5A	I_{OUT2} Segment 10	Sets gain adjustment for I_{OUT2} channel segment 10	R/W	0x20
0x5B	I_{OUT2} Segment 11	Sets gain adjustment for I_{OUT2} channel segment 11	R/W	0x20
0x5C	I_{OUT2} Segment 12	Sets gain adjustment for I_{OUT2} channel segment 12	R/W	0x20
0x5D	I_{OUT2} Segment 13	Sets gain adjustment for I_{OUT2} channel segment 13	R/W	0x20
0x5E	I_{OUT2} Segment 14	Sets gain adjustment for I_{OUT2} channel segment 14	R/W	0x20
0x5F	I_{OUT2} Segment 15	Sets gain adjustment for I_{OUT2} channel segment 15	R/W	0x20

Register Descriptions

This section provides descriptions for each register. The tables are arranged by register address in ascending order.

TABLE 2. CHIP ID REGISTER1 - ADDRESS 0x00

BIT	NAME	BIT DEFINITION
B7-B0	Chip ID	This is a read-only register that contains the chip ID. ISL58315 = 0x0F

TABLE 3. REVISION ID REGISTER1 - ADDRESS 0x01

BIT	NAME	BIT DEFINITION
B7-B0	Revision ID	This is a read-only register that contains the revision identification. Please check the “Revision History” table on page 37 for the latest information on device version ID changes. Note: this value can change depending on the version of the device. ISL58315 = 0x01

TABLE 4. DEVICE SELECT REGISTER - ADDRESS 0x03

BIT	NAME	BIT DEFINITION
B7-B0	DSR	This is the device select register. When a value written into this register matches the Device Enable Number (DEN = 0x03), the serial bus will be active. The SPI bus remains active as long as the DEN value does not change. If the DEN does not match, the SPI interface does not function. When DSR register is not set to the DEN value, the serial bus is inactive except for the ability to write to DSR register. SPI write access must be terminated by a read access in order to complete the write.

TABLE 5. ENABLE CONTROL REGISTER - ADDRESS 0x07

BIT	NAME	BIT DEFINITION
B7	Reset	1 = all internal registers are cleared, and the default values are loaded. 0 = default value. Writing a zero does nothing.
B6	Preload DATA	This register enables a preload of a data read register when a high-speed serial clock is used to clock the ADC. This prevents the serial interface from over-polling the ADC data register, which can prevent the ADC data register from being updated by the ADC. The user should first set this bit to 1, and then read the ADC data register, followed by clearing this bit to retrieve the correct ADC sampled data value. 1 = loads internal read registers 0 = ready state (default)
B5	Over-Temp Shutdown	1 = enables automatic shutdown with over-temperature 0 = disables automatic shutdown (default)
B4	Sampler Enable	1 = enables sampler 0 = disables sampler (default)
B3	ADC Enable	1 = enables ADC 0 = disables ADC (default)
B2	Heater Enable	1 = enables heater 0 = disables heater (default)
B1	LDD Chip Enable	1 = enables LDD 0 = disables LDD (default)
B0	Chip Enable	1 = enables chip. 0 = disables chip (default)

TABLE 6. DATA CONTROL REGISTER - ADDRESS 0x08

BIT	NAME	BIT DEFINITION
B7-B6	IO BUS Rail	This bit sets the compatible IO voltage of the input data bus interface. This bit should match the VSL voltage applied. Both bits must be set; 01 and 10 are invalid selection. 11 = 3.3V 00 = 1.8V (default)
B5	NU	Reserved
B4	Async_RTZ	Return-to-zero configuration 1 = RTZ is asynchronous to input clock (RTZ waveform generated by external circuit). 0 = RTZ is synchronous to input clock (default)
B3	Look Ahead Sleep Mode	Look-ahead sleep mode control 1 = disables look-ahead sleep mode 0 = enables look-ahead sleep mode (default)
B2	NU	Reserved
B1-B0	Data Mode Select	These bits configure the input data bus data format. There are four formats (see “Data Mode 0” on page 11, “Data Mode 1” on page 12, and “Data Mode 3 (LCOS Mode)” on page 12.) 1 1: Mode 3 - parallel input data bus is disabled. Pixel data for each channel is serially transferred via the SPI interface to the corresponding channel. 1 0: Mode 2 - 10 bits/clock edge; 10 bits represents a color that is synchronized with the SYNC signal. 0 1: Mode 1 - 15 bits with color pixel data packed in RG (10/5), BG (10/5) format. Each corresponding data packet clocks into the data port on both edges of the clock. 0 0: Mode 0 - 15 bits with RGB data packed in (5/5/5) format and full pixel (10 bits) clocked in on dual edges of clock (default)

TABLE 7. SAMPLER TRIGGER REGISTER - ADDRESS 0x0B

BIT	NAME	BIT DEFINITION
B7-B0	Upper Sampler Trigger Ptr	Sampler trigger point is a 10-bit value used to compare against the data word currently driving the DAC. This register holds the upper 8 bits (D9..D2) of the 10-bit value. The lower 2 bits are located in 0x0C Bits 1:0.

TABLE 8. SAMPLER CONTROL REGISTER - ADDRESS 0x0C

BIT	NAME	BIT DEFINITION
B7	Sampler Enable	1 = enables the sampler circuit 0 = disables the sampler circuit (default)
B6	Sampling Mode	This register selects which sampling mode the sampler uses to retrieve the target data. 1 = sampler continuously samples the target until 0x0C Bit 7 (Sampler Enable) is reset to zero. 0 = sampler performs a single-shot sampling. When 0x0C Bit 7 is enabled, the sampler takes one sample of the target. Once the sample has been taken, the sampler circuit resets 0x0C Bit 7 to disable (default)
B5-B4	Sample Gain	A 2-bit value changes the sampler circuit gain. 1 1: gain = 1 1 0: gain = 3/4 0 1: gain = 1/2 0 0: gain = 1/4 (default)
B3-B2	Sample Target Select	These 2 bits select which target the sampler circuit retrieves data from. 1 1: selects I_{OUT3} output channel 1 0: selects I_{OUT2} output channel 0 1: selects I_{OUT1} output channel 0 0: selects V_{SO} (default)
B1-B0	Lower Sampler Trigger Ptr	Sampler trigger point is a 10-bit value used to compare against value retrieved by sampler circuit. These 2 bits hold the lower 2 bits (D1-D0) of the 10-bit value. The upper 8 bits are located in 0x0B register.

TABLE 9. STATUS REGISTER - ADDRESS 0x0F

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5	Output Enable	1 = output DACs are enabled. 0 = output DACs are disabled.
B4	Chip Enable Status	1 = indicates hardware and register CE are both enabled. 0 = one or both methods of CE is not set.
B3	Internal Clock Status	1 = internal clock used by ADC and heater circuit is operating. 0 = internal clock powered down.
B2	A ref status	1 = indicates the analog reference and bias circuits are operating. 0 = analog reference and/or bias circuit is powered down.
B1	Thermal Shutdown Status	This bit reports a thermal shutdown event by the thermal shutdown circuit. 1 = device temperature has exceeded the thermal shutdown temperature value. 0 = device temperature trip point has not been exceeded.
B0	Power-Good Status	This bit identifies whether the device is seeing a good power supply rail. 1 = power supply is good. 0 = power supply is below an acceptable operating range.

TABLE 10. I_{OUT1} CONTROL - ADDRESS 0x10

BIT	NAME	BIT DEFINITION
B7	I_{OUT1} Enable	This bit is ANDed with CE and OutDAC enable bits Reg 0x07 Bit 0. It allows for individual disabling of this channel. 1 = I_{OUT1} enabled. 0 = I_{OUT1} disabled (default)
B6	NU	Reserved
B5	Auto Sleep Enable	1 = enables bias current reduction for I_{OUT1} color DAC if the input data is zero. 0 = disables function (default)
B4	Color DAC Enable	1 = enables I_{OUT1} color DAC 0 = disables I_{OUT1} color DAC (default)
B3-B0	NU	Reserved

TABLE 11. I_{OUT1} THRESHOLD DAC CONTROL - ADDRESS 0x11

BIT	NAME	BIT DEFINITION
B7	I_{OUT1} Threshold DAC Enable	1 = enables I_{OUT1} threshold DAC 0 = disables I_{OUT1} threshold DAC (default)
B6-B5	NU	Reserved
B4	I_{OUT1} Threshold Lowp Sleep	1 = I_{OUT1} threshold DAC sleeps on Lowp signal active. 0 = Lowp signal has no effect on I_{OUT1} threshold DAC output (default)
B3	I_{OUT1} Threshold Follow	1 = I_{OUT1} threshold DAC follows I_{OUT1} color DAC with regard to sleep. 0 = I_{OUT1} threshold DAC does not follow I_{OUT1} color DAC with regard to sleep (default)
B2-B1	I_{OUT1} Threshold RTZ Control	B2 - B1 1 1 = reserved. NOTE: Do not select this option as it would place LDD in unknown operational mode. 1 0 = if RTZ signal is active, then I_{OUT1} threshold DAC does not go to sleep, but I_{OUT1} threshold current goes to zero. 0 X = I_{OUT1} threshold DAC does not follow RTZ (default)
B0	I_{OUT1} Threshold Bias Reduction	1 = bias current is reduced depending on I_{OUT1} threshold current. 0 = bias current is independent of I_{OUT1} threshold current (default)

TABLE 12. I_{OUT1} THRESHOLD DAC REGISTER- ADDRESS 0x12

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} I_{THRESH}	These bits are the input data bits of the I_{OUT1} Threshold Current DAC. I_{OUT1} Threshold Current = Gain x (I_{OUT1} Threshold Scale) x (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255.

TABLE 13. I_{OUT1} COLOR SCALE DAC REGISTER- ADDRESS 0x13

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} Color Scale	These bits are the input bits of the I_{OUT1} Color Scale DAC; a.k.a., Color Slope I_{OUT1} Color Scale = K * (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255.

TABLE 14. I_{OUT1} BIAS REGISTER- ADDRESS 0x14

BIT	NAME	BIT DEFINITION
B7-B5	NU	Reserved
B4	I_{OUT1} Reference Current	This bit controls the reference current for I_{OUT1} channel. It adjusts the trade-off between power and accuracy. If set accurate mode is selected (default = 0x1).
B3-B0	I_{OUT1} Bias	These bits control the bias for the I_{OUT1} channel. They adjust the trade-off between power and settling speed of I_{OUT1} (default = 0x8)

TABLE 15. I_{OUT1} THRESHOLD SCALE REGISTER- ADDRESS 0x16

BIT	NAME	BIT DEFINITION
B7-B2	I_{OUT1} Threshold Scale	I_{OUT1} Threshold Scale = (33 + 32B7 + 16B6 + 8B5 + 4B4 + 2B3 + B2)/96 (default = 0xFC)
B1-B0	NU	Reserved

TABLE 16. I_{OUT1} SERIAL DATA MSB REGISTER - ADDRESS 0x1E

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} Serial Data (Upper)	When enabled, these bits correspond to I_{OUT1} data Bits 9 through 2.

TABLE 17. I_{OUT1} SERIAL DATA LSB REGISTER - ADDRESS 0x1F

BIT	NAME	BIT DEFINITION
B7-B6	I_{OUT1} Serial Data Bits	B7 holds Bit 1 and B6 holds Bit 0 of the 10-bit data.
B5-B0	NU	Reserved

TABLE 18. I_{OUT2} CONTROL REGISTER- ADDRESS 0x20

BIT	NAME	BIT DEFINITION
B7	I_{OUT2} Pipeline Enable	This bit is ANDed with CE and OutDAC enable bits Reg 0x07 Bit 0. It allows for individual disabling of this channel. 1 = I_{OUT2} enabled 0 = I_{OUT2} disabled (default)
B6	Deep Sleep at Zero Input	1 = color DAC goes into deep sleep mode when input data is zero. 0 = disabled (default)
B5	Auto Sleep	1 = enables automatic color DAC bias current adjustment according to the input data (default) 0 = disable function.
B4-B0	I_{OUT2} Color DAC Segment Enable	These 5 bits are the enable bits for I_{OUT2} color DAC segments. Each increase in binary value enables the subsequent segment. B4 - B0 1 X X X X: enables all segments (0 - 15) 0 1 1 1 1: enables segment 0 - 14, 0 1 1 1 0: enables segment 0 - 13 0 1 1 0 1: enables segment 0 - 12 0 1 1 0 0: enables segment 0 - 11 0 1 0 1 1: enables segment 0 - 10 0 1 0 1 0: enables segment 0 - 9 0 1 0 0 1: enables segment 0 - 8 0 1 0 0 0: enables segment 0 - 7 0 0 1 1 1: enables segment 0 - 6 0 0 1 1 0: enables segment 0 - 5 0 0 1 0 1: enables segment 0 - 4 0 0 1 0 0: enables segment 0 - 3 0 0 0 1 1: enables segment 0 - 2 0 0 0 1 0: enables segment 0 - 1 0 0 0 0 1: enables segment 0 0 0 0 0 0: all segments are disabled (default)

TABLE 19. I_{OUT2} THRESHOLD DAC CONTROL REGISTER - ADDRESS 0x21

BIT	NAME	BIT DEFINITION
B7-B5	I_{OUT2} Threshold DAC Segment Enable	B7 - B5 1 X X: enables all segments (0 - 3) (default) 0 1 1: enables segment 0 - 2 0 1 0: enables segment 0 - 1 0 0 1: enables segment 0 0 0 0: all segments are disabled
B4	I_{OUT2} Threshold Lowp Sleep	1 = I_{OUT2} threshold DAC sleeps on Lowp signal active (default) 0 = Lowp signal has no effect on I_{OUT2} threshold DAC output.
B3	I_{OUT2} Threshold Follow	1 = I_{OUT2} threshold DAC follows I_{OUT2} color DAC with regard to sleep (default) 0 = I_{OUT2} threshold DAC does not follow I_{OUT2} color DAC with regard to sleep.
B2-B1	I_{OUT2} Threshold RTZ Control	B2 - B1 1 1 = if RTZ signal is active, then I_{OUT2} threshold DAC goes to sleep and the threshold current goes to zero. 1 0 = if RTZ signal is active, then I_{OUT2} threshold DAC does not go to sleep but the threshold current goes to zero. 0 X = I_{OUT2} threshold DAC does not follow RTZ (default)
B0	I_{OUT2} Threshold Bias Reduction	1 = bias current is reduced depending on the I_{OUT2} threshold current (default) 0 = bias current is independent of the I_{OUT2} threshold current.

TABLE 20. I_{OUT2} THRESHOLD DAC REGISTER - ADDRESS 0x22

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} Threshold	These bits are the input data bits of the I_{OUT2} Threshold Current DAC. I_{OUT2} Threshold Current = Gain x (I_{OUT2} Threshold Scale) x (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255.

TABLE 21. I_{OUT2} COLOR SCALE REGISTER - ADDRESS 0x23

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} Color Scale	These bits are the input bits of the I_{OUT2} Color Scale DAC. I_{OUT2} Color Scale = Gain (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255.

TABLE 22. I_{OUT2} BIAS REGISTER- ADDRESS 0x24

BIT	NAME	BIT DEFINITION
B7-B5	NU	Reserved
B4	I_{OUT2} Reference Current	This bit controls the reference current for I_{OUT2} channel. It adjusts the trade-off between power and accuracy. If set accurate mode is selected (default = 0x1).
B3-B0	I_{OUT2} Bias	These bits control the bias for the I_{OUT2} channel. They adjust the trade-off between power and settling speed of I_{OUT2}. A value of 0x0 should be used only for DC mode, (default = 0x8).

TABLE 23. I_{OUT2} THRESHOLD SCALE REGISTER - ADDRESS 0x26

BIT	NAME	BIT DEFINITION
B7-B2	I_{OUT2} Threshold Scale	I_{OUT2} Threshold Scale = (33 + 32B7 + 16B6 + 8B5 + 4B4 + 2B3 + B2)/96 (default = 0xFC)
B1-B0	NU	Reserved

TABLE 24. I_{OUT2} SERIAL DATA MSB REGISTER - ADDRESS 0x2E

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} Serial Data (Upper)	When enabled, these bits correspond to I_{OUT2} data Bits 9 through 2.

TABLE 25. I_{OUT2} SERIAL DATA LSB REGISTER - ADDRESS 0x2F

BIT	NAME	BIT DEFINITION
B7-B6	I_{OUT2} Serial Data Bits	B7 holds Bit 1 and B6 holds Bit 0 of the 10-bit data.
B5-B0	NU	Reserved

TABLE 26. I_{OUT3} CONTROL REGISTER - ADDRESS 0x30

BIT	NAME	BIT DEFINITION
B7	I_{OUT3} Enable	1 = I_{OUT3} enabled (default) 0 = I_{OUT3} disabled
B6	NU	Reserved
B5	Auto Sleep Enable	1 = enables bias current reduction for I_{OUT3} color DAC if the input data is zero (default) 0 = disables function
B4	I_{OUT3} Color DAC Enable	1 = enables I_{OUT3} color DAC output (default) 0 = disables I_{OUT3} color DAC output
B3-B0	NU	Reserved

TABLE 27. I_{OUT3} THRESHOLD DAC CONTROL REGISTER - ADDRESS 0x31

BIT	NAME	BIT DEFINITION
B7	I_{OUT3} Threshold DAC Enable	1 = enables I_{OUT3} threshold DAC (default) 0 = disables I_{OUT3} threshold DAC
B6-B5	NU	Reserved
B4	I_{OUT3} Threshold Lowp Sleep	1 = I_{OUT3} threshold DAC sleeps on Lowp signal active (default). 0 = Lowp signal has no effect on I_{OUT3} threshold DAC output.
B3	I_{OUT3} Threshold Follow	1 = I_{OUT3} threshold DAC follows I_{OUT3} color DAC with regard to sleep. 0 = I_{OUT3} threshold DAC does not follow I_{OUT3} color DAC with regard to sleep (default)
B2-B1	I_{OUT3} Threshold RTZ Control	B2 - B1 1 1 = if RTZ signal is active, then I_{OUT3} threshold DAC goes to sleep and I_{OUT3} threshold current goes to zero. 1 0 = if RTZ signal is active, then I_{OUT3} threshold DAC does not go to sleep but I_{OUT3} threshold current goes to zero. 0 X = I_{OUT3} threshold DAC does not follow RTZ (default)
B0	I_{OUT3} Threshold Bias Reduction	1 = bias current is reduced depending on I_{OUT3} threshold current (default) 0 = bias current is independent of I_{OUT3} threshold current.

TABLE 28. I_{OUT3} THRESHOLD DAC REGISTER - ADDRESS 0x32

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} I_{THRESH}	These bits are the input data bits of the I_{OUT3} Threshold Current DAC. I_{OUT3} Threshold Current = Gain x (I_{OUT3} Threshold Scale) x (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255.

TABLE 29. I_{OUT3} COLOR SCALE REGISTER - ADDRESS 0x33

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} Color Scale	These bits are the input bits of the I_{OUT3} Color Scale DAC. I_{OUT3} Color Scale = Gain (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255.

TABLE 30. I_{OUT3} COLOR DAC BIAS REGISTER - ADDRESS 0x34

BIT	NAME	BIT DEFINITION
B7-B5	NU	Reserved
B4	I_{OUT3} Reference Current	This bit controls the reference current for I_{OUT3} channel. It adjusts the trade-off between power and accuracy. If set accurate mode is selected (default = 0x1)
B3-B0	I_{OUT3} Bias	These bits control the bias for the I_{OUT3} channel. They adjust the trade-off between power and settling speed of I_{OUT3} (default = 0x8)

TABLE 31. I_{OUT3} THRESHOLD SCALE REGISTER - ADDRESS 0x36

BIT	NAME	BIT DEFINITION
B7-B2	I_{OUT3} Threshold Scale	I_{OUT3} Threshold Scale = (33 + 32B7 + 16B6 + 8B5 +4B4 + 2B3 + B2)/96 (default = 0xFC)
B1-B0	NU	Reserved

TABLE 32. I_{OUT3} SERIAL DATA MSB REGISTER - ADDRESS 0x3E

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} Serial Data (Upper)	When enabled, these bits correspond to I_{OUT3} data Bits 9 through 2.

TABLE 33. I_{OUT3} SERIAL DATA LSB REGISTER - ADDRESS 0x3F

BIT	NAME	BIT DEFINITION
B7-B6	I_{OUT3} Serial Data Bits	B7 holds Bit 1 and B6 holds Bit 0 of the 10-bit data.
B5-B0	NU	Reserved

TABLE 34. ADC CONTROL 0 REGISTER - ADDRESS 0x41

BIT	NAME	BIT DEFINITION
B7	Start ADC	1 = begins an ADC conversion cycle. Once that conversion is complete, this bit is automatically reset. This allows for host MCU to poll this bit to retrieve converted data. 0 = ADC conversion is complete and data is available (default)
B6	ADC Enable	1 = ADC circuit enabled 0 = ADC circuit disabled (default)
B5 - B4	ADC Clock	These two bits set the ADC clock. B5 B4 1 1 = 625kHz clock 1 0 = 1.25MHz clock 0 1 = 2.50MHz clock 0 0 = 5.00MHz clock (default)
B3	NU	Reserved
B2 - B0	ADC Source Select	These three bits select the source that the ADC would sample and convert. B2 B1 B0 1 1 1 = sampler (This function enables the ADC to be trigger by the sampler circuit.) 1 1 0 = monitor pin 2 1 0 1 = monitor pin 1 1 0 0 = 2 Vbe (used to monitor temperature) 0 1 1 = Vbe (used to monitor temperature) 0 1 0 = voltage at R_{SET} pin (Nominal 1V) 0 0 1 = $V_{DD}/4$ 0 0 0 = analog ground; (default)

TABLE 35. ADC CONTROL 1 REGISTER - ADDRESS 0x42

BIT	NAME	BIT DEFINITION
B7	DAC Test Mode	This bit is used for factory test. 1 = value written into Register 0x43 is loaded into DAC. 0 = ADC operates normally; default
B6	Initialize Peak Detector	1 = last value written to Register 0x43 is copied into ADC peak detector register; then, this bit is reset to zero. 0 = no action; default
B5 - B2	NU	Reserved
B1 - B0	Peak Detector	Peak detector B1 B0 1 1 = positive peak detect 1 0 = disable 0 1 = negative peak detect 0 0 = disable; (default)

TABLE 36. ADC OUTPUT DATA REGISTER (READ) - ADDRESS 0x43

BIT	NAME	BIT DEFINITION
B7 - B0	ADC Data	Reading this register returns the value of an ADC conversion. Full scale = 1.2V; each LSB = 4.69mV

TABLE 37. ADC OUTPUT DATA REGISTER (WRITE) - ADDRESS 0x43

BIT	NAME	BIT DEFINITION
B7 - B0	ADC Data	Writing to this register places the data into the peak detector or the internal DAC circuit. Target device is selected by the following conditions: Reg 0x42 Bit 1 = 1 for peak detector Reg 0x42 Bit 7 = 1 for internal DAC. The voltage generated by value written can be observed through the monitor pin.

TABLE 38. RTZ PWM CONTROL REGISTER - ADDRESS 0x44

BIT	NAME	BIT DEFINITION
B7	RTZ 3 Enable	Enables RTZ on I_{OUT3} output
B6	RTZ 2 Enable	Enables RTZ on I_{OUT2} output
B5	RTZ 1 Enable	Enables RTZ on I_{OUT1} output
B4 - B3	PWM Pulse Delay	RTZ PWM pulse delay. Delay width is measured as fraction of clock period. This setting is common to all three output channels. B4 B3 1 1 = 5/16 delay 1 0 = 3/16 delay 0 1 = 1/16 delay 0 0 = no delay (default)
B2 - B0	PWM Pulse Width	RTZ PWM pulse width size. Pulse width is measured as fraction of clock period. This setting is common to all three output channels. B2 B1 B0 1 1 1 = 8/16 1 1 0 = 7/16 1 0 1 = 6/16 1 0 0 = 5/16 0 1 1 = 4/16 0 1 0 = 3/16 0 0 1 = 2/16 0 0 0 = 1/16 (default)

TABLE 39. HEATER CONTROL REGISTER - ADDRESS 0x49

BIT	NAME	BIT DEFINITION
B7-B5	Sampling Clock	Selects the number of clock cycles between samples B7 B6 B5 1 1 1 = 512 clocks 1 1 0 = 256 clocks 1 0 1 = 128 clocks 1 0 0 = 64 clocks 0 1 1 = 32 clocks 0 1 0 = 16 clocks 0 0 1 = 8 clocks 0 0 0 = 4 clocks (default)
B4-B3	Heater_Ref_Current	Sets the reference current used by the heater B4 B3 1 1 = 20mA 1 0 = 12mA 0 1 = 6.4mA 0 0 = 1.3mA (default)

TABLE 39. HEATER CONTROL REGISTER - ADDRESS 0x49 (Continued)

BIT	NAME	BIT DEFINITION
B2-B0	Heater Mode Sel	Selects the various heater method. See Tables 1 through 47. B2 B1 B0 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Heater set to 100% 1 0 0 = Heater is pulsed 0 1 1 = Heater is disabled (will be shown as NU) 0 1 0 = ADC enabled 0 0 1 = Heater in PWM mode 0 0 0 = Heater is disabled (default)

TABLE 40. HEATER SET POINT REGISTER - ADDRESS 0x4A

BIT	NAME	BIT DEFINITION
B7-B0	HTR Set Ptr	Sets the target resistance, which corresponds to a temperature value.

TABLE 41. HEATER READ BACK REGISTER - ADDRESS 0x4B

BIT	NAME	BIT DEFINITION
B7-B0	HTR Read	This is a read-only register. The value represents the current heater value.

TABLE 42. THERMAL SHUTDOWN REGISTER - ADDRESS 0x4C

BIT	NAME	BIT DEFINITION
B7-B0	Shutdown Temp	This 8-bit value sets the temperature which, when exceeded, causes a device shutdown. The thermal shutdown circuit compares this register value to the value in the thermal data register (0x4E). If the value of 0x4E is less than 0x4C, the device goes into thermal shutdown. A different thermal shutdown temperature can be programmed into this register during initialization of device. For the temperature sensor to work, the ADC must be enabled by Bit 3 in Register 0x07 and by Bit 6 in Register 41. In addition, the thermal shutdown must be enabled by Bit 5 of Register 07. NOTE: A low binary value represents a high temperature.

TABLE 43. THERMAL RECOVERY REGISTER - ADDRESS 0x4D

BIT	NAME	BIT DEFINITION
B7-B0	Recovery Temp	This 8-bit value sets recovery temperature to re-enable LDD operation after a thermal shutdown. The thermal recovery circuit compares this register value to the value in thermal data register, 0x4E. If the value of 0x4E is greater than 0x4D, the device is re-enabled for operation. A different thermal recovery temperature can be programmed into this register during initialization of device; however, it is not recommended to change this register value to be less than the default. NOTE: An increasing temperature returns a small binary value. A decreasing temperature returns a larger binary value.

TABLE 44. THERMAL DATA REGISTER - ADDRESS 0x4E

BIT	NAME	BIT DEFINITION
B7-B0	Die_Temp	This register returns the current measured temperature value. NOTE: An increasing temperature returns a small binary value. A decreasing temperature returns a larger binary value.

TABLE 45. I_{OUT2} GAIN SEGMENT 0 REGISTER - ADDRESS 0x50

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 0 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 46. I_{OUT2} GAIN SEGMENT 1 REGISTER - ADDRESS 0x51

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 1 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 47. I_{OUT2} GAIN SEGMENT 2 REGISTER - ADDRESS 0x52

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 2 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 48. I_{OUT2} GAIN SEGMENT 3 REGISTER - ADDRESS 0x53

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 3 Gain	Gain = (33 + 32B5 +16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 49. I_{OUT2} GAIN SEGMENT 4 REGISTER - ADDRESS 0x54

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 4 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 50. I_{OUT2} GAIN SEGMENT 5 REGISTER - ADDRESS 0x55

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 5 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 51. I_{OUT2} GAIN SEGMENT 6 REGISTER - ADDRESS 0x56

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 6 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 52. I_{OUT2} GAIN SEGMENT 7 REGISTER - ADDRESS 0x57

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 7 Gain	Gain = (33 + 32B5 + 16B4 + 8B3+ 4B2 + 2B1 + B0)/64.

TABLE 53. I_{OUT2} GAIN SEGMENT 8 REGISTER - ADDRESS 0x58

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 8 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 54. I_{OUT2} GAIN SEGMENT 9 REGISTER - ADDRESS 0x59

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 9 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 55. I_{OUT2} GAIN SEGMENT 10 REGISTER - ADDRESS 0x5A

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 10 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 56. I_{OUT2} GAIN SEGMENT 11 REGISTER - ADDRESS 0x5B

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 11 Gain	Gain = (33 + 32B5 + 16B4 + 8B3+ 4B2 + 2B1 + B0)/64.

TABLE 57. I_{OUT2} GAIN SEGMENT 12 REGISTER - ADDRESS 0x5C

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 12 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 58. I_{OUT2} GAIN SEGMENT 13 REGISTER - ADDRESS 0x5D

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 13 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 +B0)/64.

TABLE 59. I_{OUT2} GAIN SEGMENT 14 REGISTER - ADDRESS 0x5E

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 14 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

TABLE 60. I_{OUT2} GAIN SEGMENT 15 REGISTER - ADDRESS 0x5F

BIT	NAME	BIT DEFINITION
B7-B6	NU	Reserved
B5-B0	Seg 15 Gain	Gain = (33 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0)/64.

Performance Graphs

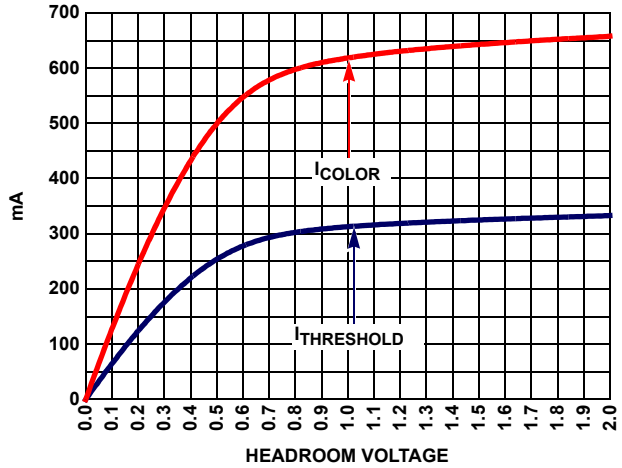


FIGURE 19. I_{OUT1} AND I_{OUT3} NMOS MAXIMUM CURRENT vs HEADROOM VOLTAGE INPUT COLOR DAC = 0x3FF; COLOR SCALE DAC = 0xFF

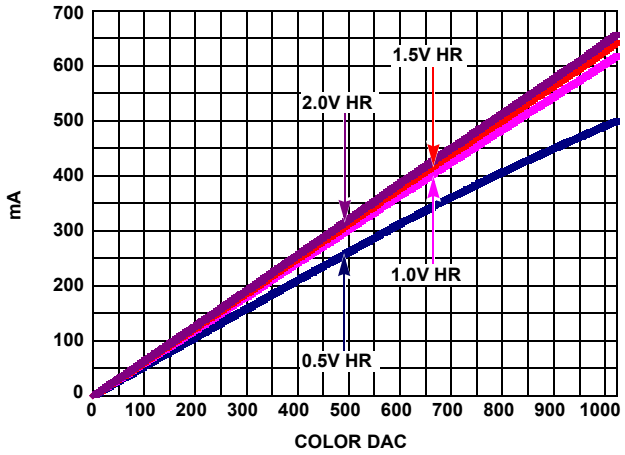


FIGURE 20. I_{OUT1} AND I_{OUT3} NMOS COLOR CURRENT vs INPUT PIXEL VALUE @ DIFFERENT HEADROOM VOLTAGES; COLOR SCALE DAC = 0xFF

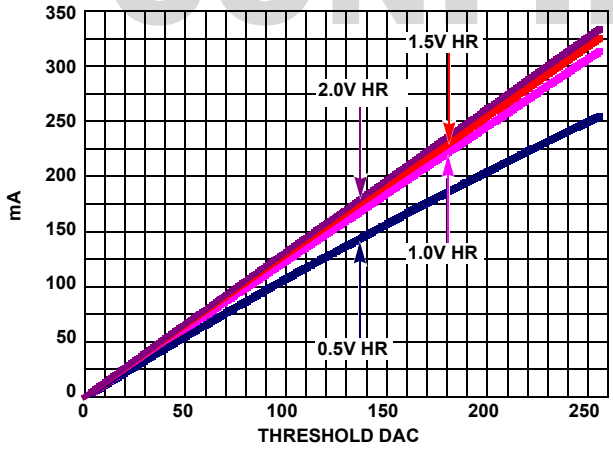


FIGURE 21. I_{OUT1} AND I_{OUT3} NMOS THRESHOLD CURRENT vs THRESHOLD DAC VALUE @ DIFFERENT HEADROOM VOLTAGES; THRESHOLD SCALE DAC = 0XFC

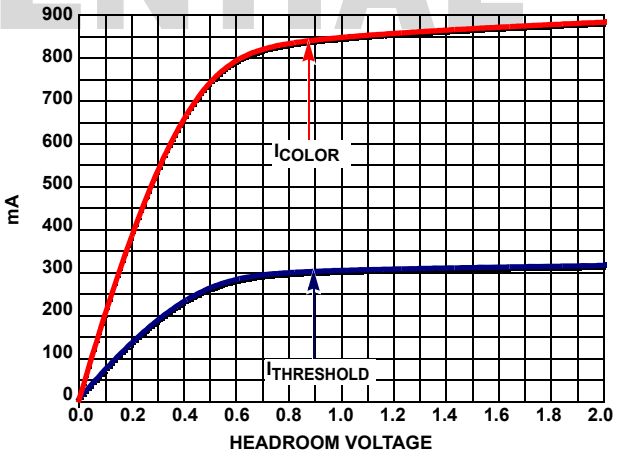


FIGURE 22. I_{OUT2} NMOS DAC MAXIMUM CURRENT vs HEADROOM VOLTAGE, INPUT COLOR DAC = 0x3FF; COLOR SCALE DAC = 0xFF

Performance Graphs

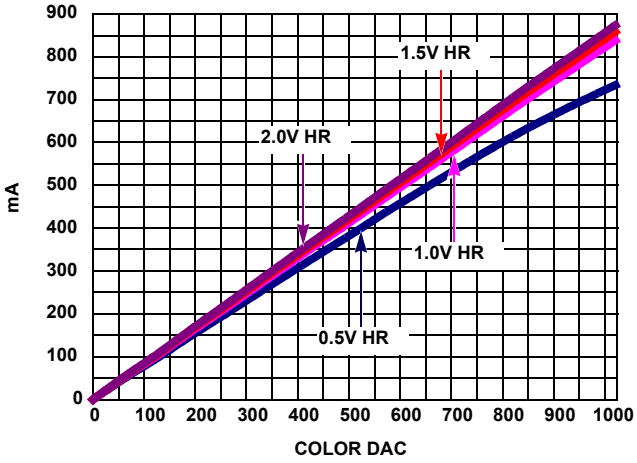


FIGURE 23. I_{OUT2} NMOS COLOR DAC CURRENT vs INPUT PIXEL VALUE @ DIFFERENT HEADROOM VOLTAGES; COLOR SCALE DAC = 0xFF

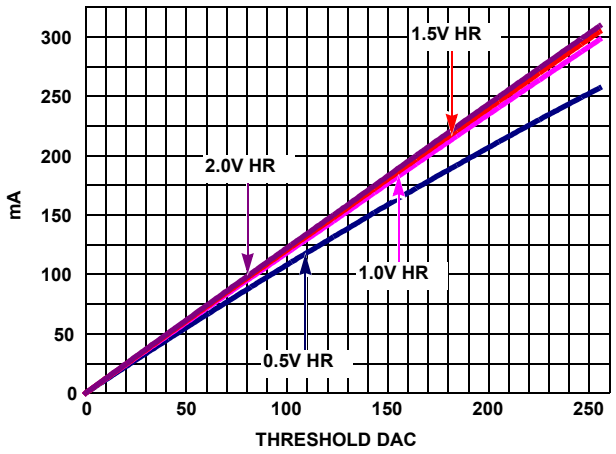


FIGURE 24. I_{OUT2} NMOS THRESHOLD CURRENT vs THRESHOLD DAC VALUE @ DIFFERENT HEADROOM VOLTAGES; COLOR SCALE DAC = 0xFC

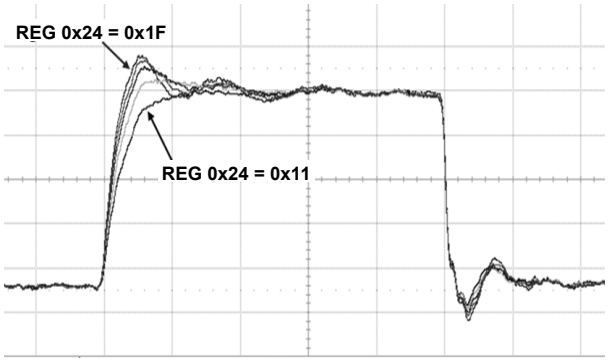


FIGURE 25. I_{OUT2} WAVEFORM AT DIFFERENT BIAS VOLTAGES SCALE: 5ns/DIV, 200mV/DIV

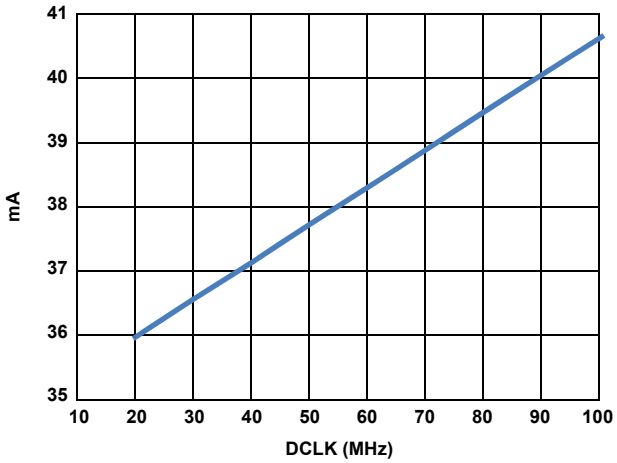


FIGURE 26. TOTAL CURRENT vs. INPUT CLOCK FREQUENCY. DEFAULT SETTINGS EXCEPT REG. 0x07 = 0x03, REG. 0x10, 0x11, 0x20, 0x21, 0x30, 0x31 = 0x90, REG. 0x13, 0x23, 0x33 = 0xFF, MODE 0, CLOCK FREQUENCY: 20MHz TO 100MHz

Packaging Information

Note that in the TQFN package, the die is mounted directly on the thermal pad. This provides a very low thermal resistance junction to the thermal pad of just a few degrees (C) per Watt. The problem is in moving the heat from the thermal pad to some other heat sink.

Figure 27 shows that when mounted well on a 4-layer PCB with three ground plane layers and an area of 10cm x 10cm, θ_{JA} is +28.5°C/W. The typical application does not afford a heat sink that is this efficient.

The device comes with a built-in thermal sensor, but the user must calibrate the sensor.

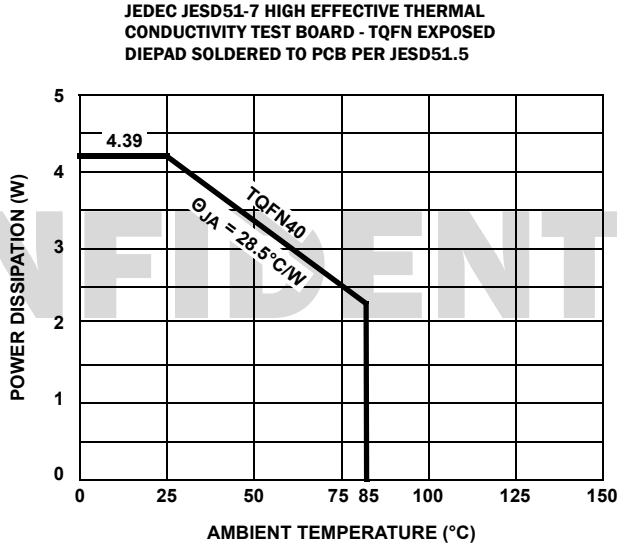


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
9/30/2011	FN7543.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL58315

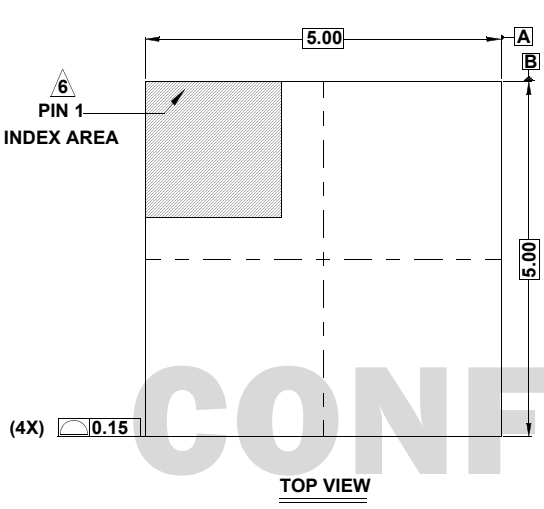
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

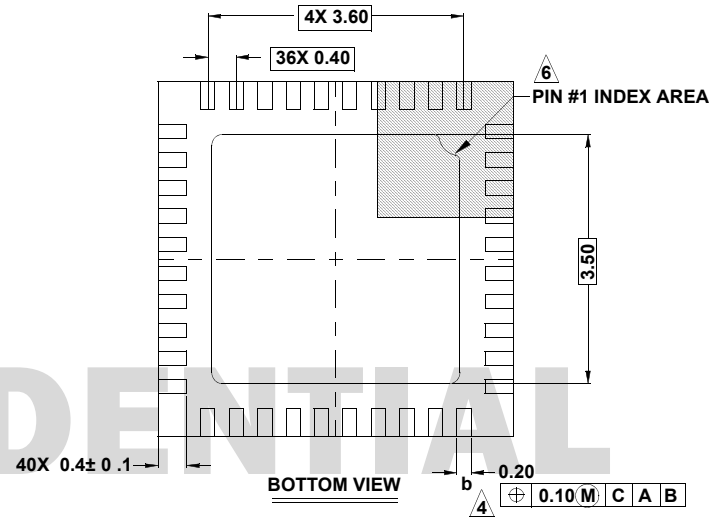
Package Outline Drawing

L40.5x5

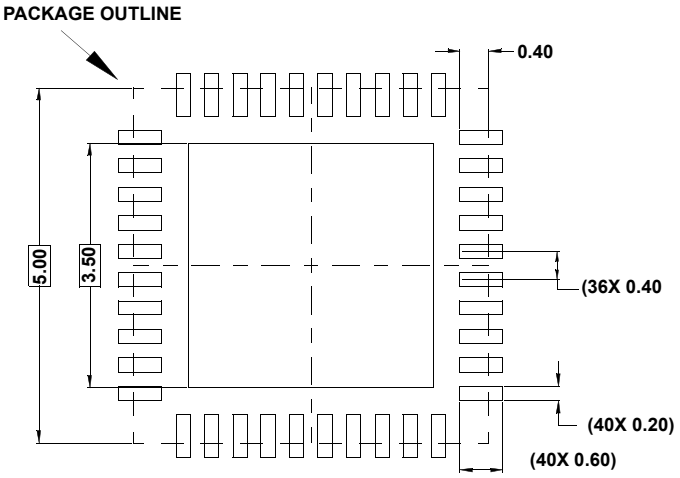
40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 9/10



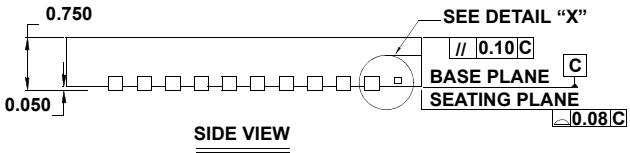
TOP VIEW



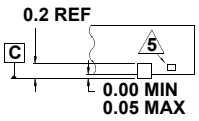
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1