ISL55020

Wideband, Low Distortion, Differential Amplifier

FN6287
Rev 0.00
December 18, 2006

The ISL55020 is fully differential wideband amplifier designed to drive differential ADCs. This device features a high drive capability of 100mA, low operating quiescent current of 21mA and operates with both single and dual supplies over a range of 4.5V (±2.25V) to +12V (±6V). Key features include high impedance, full differential inputs and full differential or DC referenced complementary single-ended outputs A wide bandwidth unity gain common mode (VCM) amplifier input is included to provide DC offset correction or common mode signal injection to the differential output.

The ISL55020 is available in the thermally-enhanced 16 Ld QFN package and is specified for operation over the full -40°C to +85°C temperature range. The ISL55020 has an $\overline{EN}$ pin to disable the outputs.

Features

- Fully differential current feedback amplifier
- High impedance differential inputs
- Differential output drives up to 100mA from a +12V supply
- Separate unity-gain common mode input (VCM)
- 300MHz bandwidth
- 1200V/µs Slewrate
- -73.3dBc typical driver output distortion at $10V_{PP}$; 1MHz
- -64.6dBc typical driver output distortion at $10V_{PP}$; 4MHz
- Low quiescent supply current of 21mA
- Pb-free plus anneal available (RoHS compliant)

Applications

- High Linearity ADC preamplifier
- Differential driver
- Wireless communication receiver
- Differential active filter

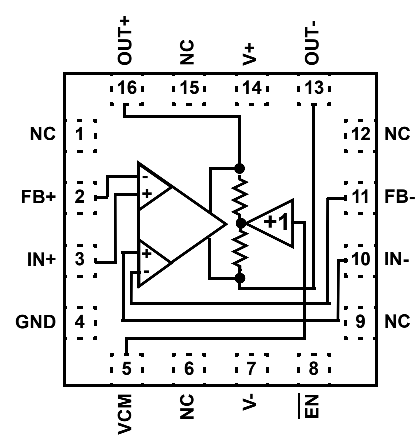
Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55020IRZ	55020IRZ	-	16 Ld QFN	MDP0046
ISL55020IRZ-T13	55020IRZ	13”	16 Ld QFN	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL55020
(16 LD QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

V+ Voltage to Ground or V- . . . . -0.3V to +13.2V
V- Voltage to Ground or V+ . . . . +0.3V to -13.2V
IN+, IN-, FB+, FB-, VCM, EN Voltage . . . . V- -0.3V to V+ +0.3V
Current into any Input 8mA
Continuous Output Current 100mA
ESD Tolerance
  Human Body Model 3kV
  Machine Model 200V

Thermal Information

Thermal Resistance θ_{JA} (°C/W)
  16 Ld QFN Package 40
Ambient Operating Temperature Range . . . .-40°C to +85°C
Storage Temperature Range . . . .-60°C to +150°C
Operating Junction Temperature . . . . +150°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 12V, R_F = 750Ω, R_G = 1.5kΩ, R_L = 1kΩ connected to mid supply, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
V_{OS}	Common Mode Offset Voltage		-38	15	38	mV
ΔV_{OS}	V_{OS} Mismatch		-7	0.7	7	mV
INPUT CHARACTERISTICS						
I_B+, I_B-	Non-Inverting Input Bias Current		-7		7	µA
F_B+, F_B-	Inverting Input Bias Current		-125	25	125	µA
ΔI_B-	I_B- Mismatch		-75	0	75	µA
e_N	Input Noise Voltage	f_O = 1kHz		9.8		nV/√Hz
		f_O = 10kHz		6.9		nV/√Hz
i_N	Input Noise Current	f_O = 1kHz		6.6		pA/√Hz
		f_O = 10kHz		2.7		pA/√Hz
CMIR	Common Mode Input Range IN+, IN-		2		10	V
VCM						
I_B **VCM**	**VCM** Input Bias Current	VCM = 5V to 6V	-7		7	µA
VOS VCM	((VOUT+) + (VOUT -))/2	VCM, IN +, IN- = 0V, R_L = 1kΩ	-150		150	mV
VCM Av	Close Loop Gain	ΔVCM = 1V, VCM = 5V to 6V	0.87	0.95	1.03	V/V
CMIR	Common Mode Input Range VCM		2.3		9.7	V
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing (differential)	V_S = ±6V, R_L = 1kΩ differential load	±4.8	±5.0		V
		V_S = 4.5V, R_L = 1kΩ differential load	±1.05			V
I_{OUT}	Output Current	R_L = 0Ω differential load		±150		mA
		R_L = 50Ω differential load	±1.45			mA
SUPPLY						
V_S	Supply Voltage	Single supply	4.5		12	V
I_S+ ENABLE	Positive Supply Current	All outputs at 0V, EN = 0V	14	21	28	mA
IS- ENABLE	Negative Supply	All outputs at 0V, EN = 0V	-28	-21	-14	mA
I_S+ DISABLE	Positive Supply Current	All outputs at 0V, EN = 5V	0.5	1.4	2.5	mA
IS- DISABLE	Negative Supply	All outputs at 0V, EN = 5V	-2.5	-1.6	0.5	mA
Ts	Thermal Shutdown Temperature	IC Junction Temperature		185		°C
Ts-hys	Thermal Shutdown Hysteresis	IC Junction Shutdown Hysteresis		15		°C

Electrical Specifications V_S = 12V, R_F = 750Ω, R_G = 1.5kΩ, R_L = 1kΩ connected to mid supply, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC						
V_{INH}, $\overline{EN}$	ENABLE High Level		2			V
V_{INL}, $\overline{EN}$	ENABLE Low Level				0.8	V
I_{INH}, $\overline{EN}$	Input Current, High	$\overline{ENABLE}$ = 5V	180	250	320	µA
I_{INL}, $\overline{EN}$	Input Current, Low	$\overline{ENABLE}$ = 0V	-5		+5	µA
$t_{\overline{EN}}$ ON	Enable time, off to on	$\overline{ENABLE}$ = 5V to 0V		12		nS
t$\overline{EN}$ OFF	Disable time, on to off	$\overline{ENABLE}$ = 0V to 5V		250		nS
R_{IN}	IN+, IN- Input resistance disables state	V+ = 12V, Vin = 2V to 10V, $\overline{ENABLE}$ = 5V	1			MΩ
		V+ = 4.5V,Vin = 2V to 4V, $\overline{ENABLE}$ = 5V	1			MΩ
AC PERFORMANCE						
BW	-3dB Bandwidth, single-ended output to GND (Figure 3)	A_{VS} = +2.5, R_F = 750Ω, R_G = 374Ω, RL=100Ω		300		MHz
		A_{VS} = 5, R_F = 750Ω, R_G = 169Ω, RL=100Ω		200		MHz
THD, HD2, HD3	THD, A = 2; Differential	f = 1MHz, V_O = 1V_{P-P}, R_L = 1kΩ		-63.8		dBc
		f = 1MHz, V_O = 10V_{P-P}, R_L = 1kΩ		-73.3		dBc
		f = 4MHz, V_O = 1V_{P-P}, R_L = 1kΩ		-57.4		dBc
		f = 4MHz, V_O = 10V_{P-P}, R_L = 1kΩ		-62.4		dBc
	HD2, A_V = 2; Differential	f = 1MHz, V_O = 1V_{P-P}, R_L = 1kΩ		-82.3		dBc
		f = 1MHz, V_O = 10V_{P-P}, R_L = 1kΩ		77.6		dBc
		f = 4MHz, V_O = 1V_{P-P}, R_L = 1kΩ		-62.3		dBc
		f = 4MHz, V_O = 10V_{P-P}, R_L = 1kΩ		-64.6		dBc
	HD3, A_V = 2; Differential	f = 1MHz, V_O = 1V_{P-P}, R_L = 1kΩ		-68.5		dBc
		f = 1MHz, V_O = 10V_{P-P}, R_L = 1kΩ		-83.5		dBc
		f = 4MHz, V_O = 1V_{P-P}, R_L = 1kΩ		-60.3		dBc
		f = 4MHz, V_O = 10V_{P-P}, R_L = 1kΩ		-67.7		dBc
SR	Slew Rate, Single-ended	V_{OUT} from -3V to +3V, R_L = 1kΩ	600	1200		V/µs

Typical Performance Curves

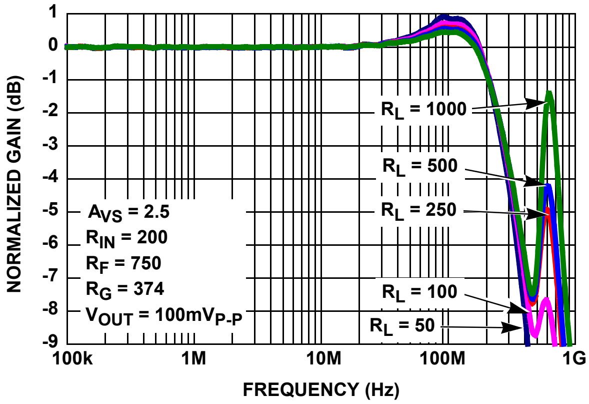


FIGURE 1. SINGLE-ENDED GAIN vs FREQUENCY vs R_L

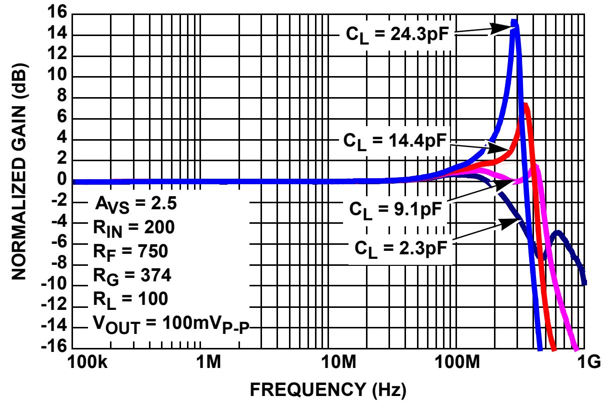


FIGURE 2. SINGLE-ENDED GAIN vs FREQUENCY vs C_L

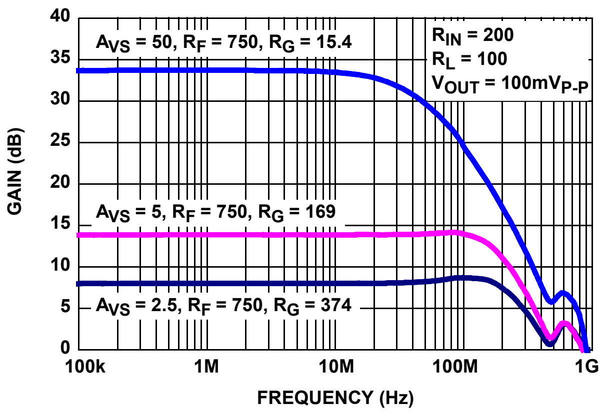


FIGURE 3. CLOSED LOOP GAIN vs FREQUENCY

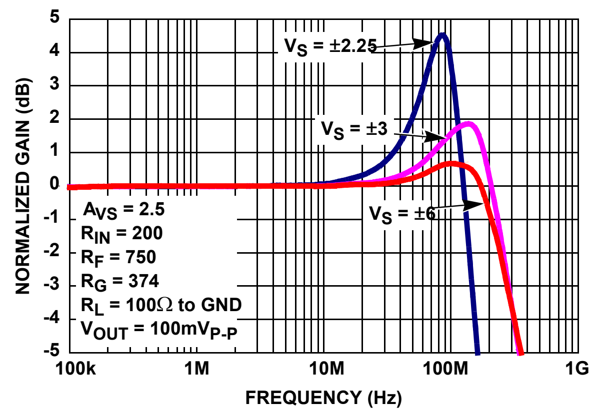


FIGURE 4. SINGLE-ENDED GAIN vs FREQUENCY vs V_S

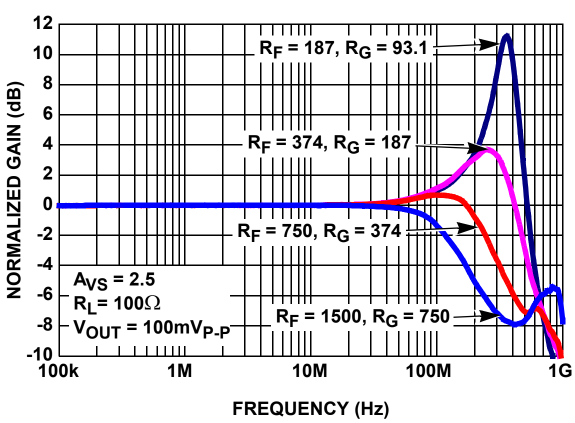


FIGURE 5. SINGLE-ENDED GAIN vs FREQUENCY vs R_F/R_G

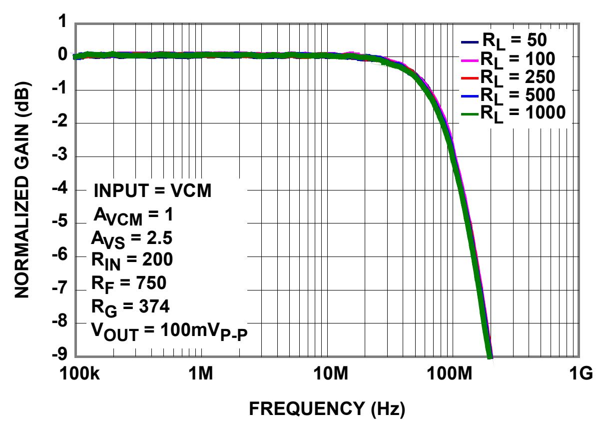


FIGURE 6. VCM GAIN vs FREQUENCY vs R_L

Typical Performance Curves (Continued)

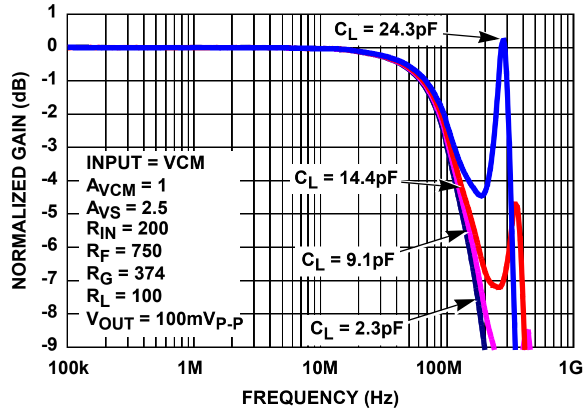


FIGURE 7. VCM GAIN vs FREQUENCY vs CL

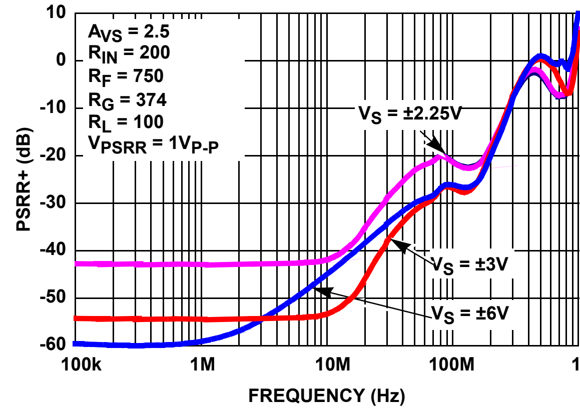


FIGURE 8. PSRR+ vs FREQUENCY vs V_S (DUAL SUPPLIES)

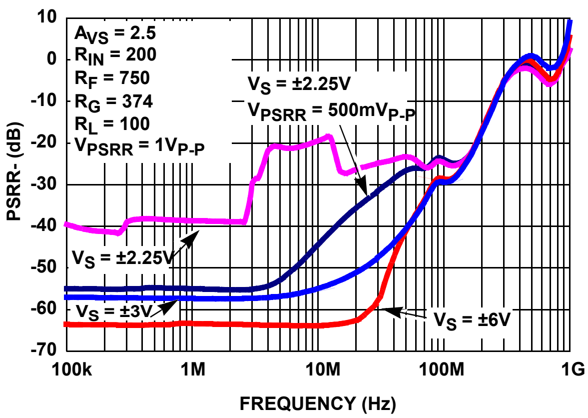


FIGURE 9. PSRR- vs FREQUENCY vs V_S

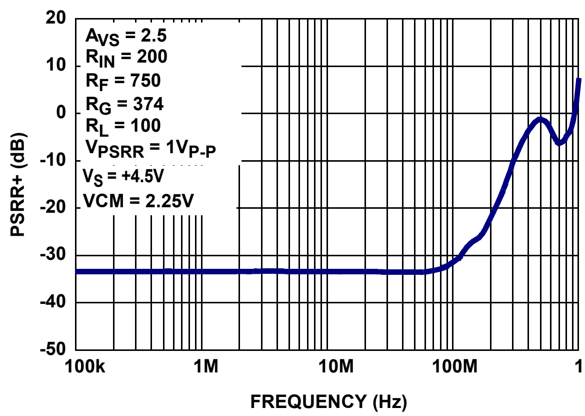


FIGURE 10. PSRR+ vs FREQUENCY vs V_S (SINGLE SUPPLY)

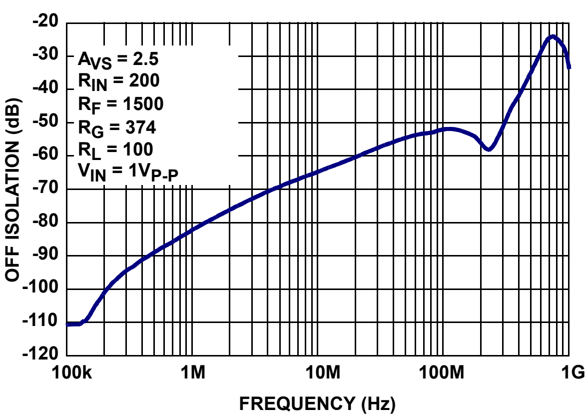


FIGURE 11. INPUT OFF ISOLATION GAIN vs FREQUENCY SINGLE-ENDED

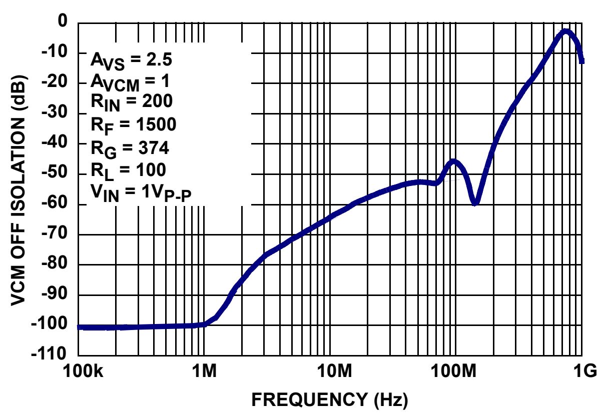


FIGURE 12. VCM OFF ISOLATION vs FREQUENCY - SINGLE-ENDED

Typical Performance Curves (Continued)

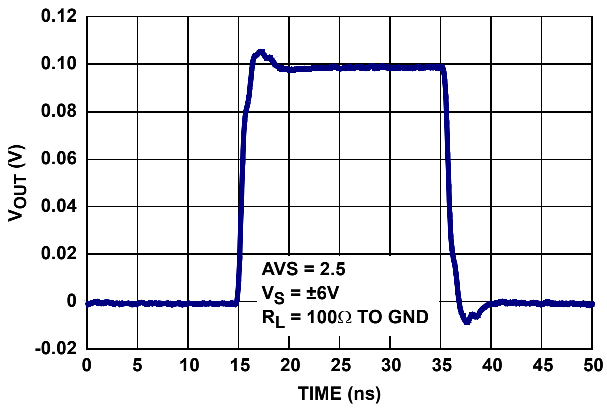


FIGURE 13. SMALL SIGNAL STEP RESPONSE

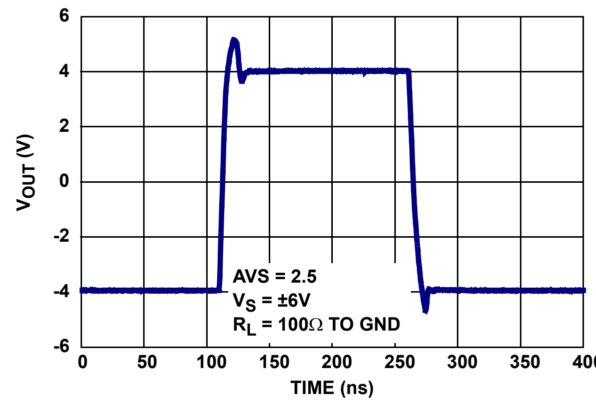


FIGURE 14. LARGE SIGNAL STEP RESPONSE

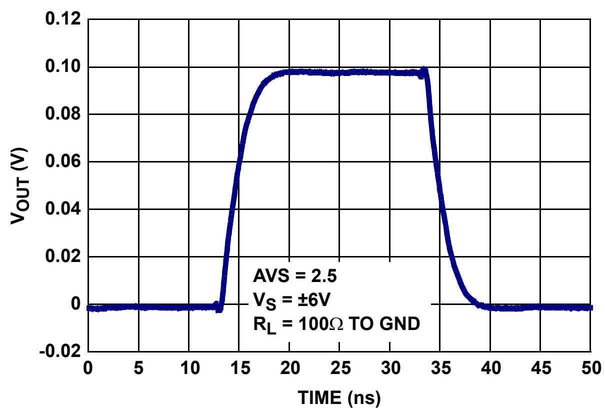


FIGURE 15. SMALL SIGNAL STEP RESPONSE - VCM TO V_{OUT}

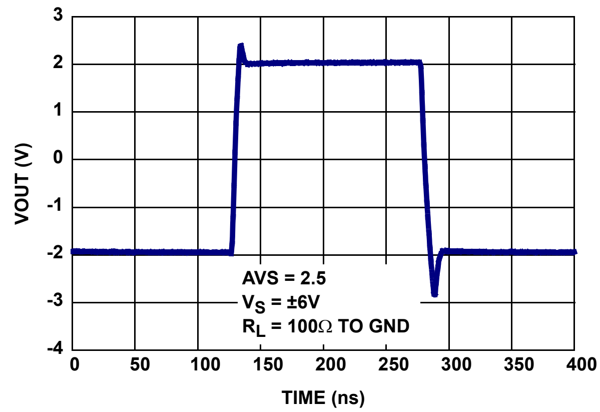


FIGURE 16. LARGE SIGNAL STEP RESPONSE - VCM TO V_{OUT}

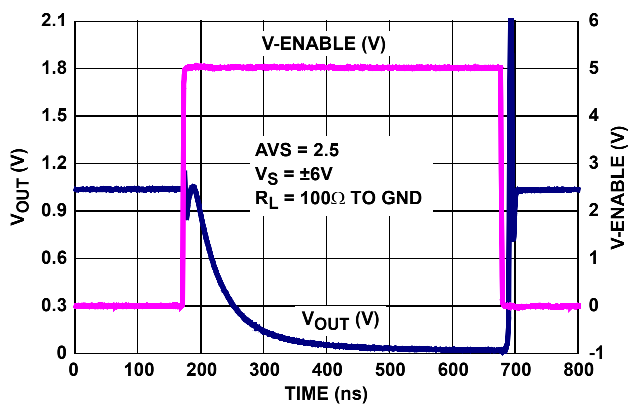
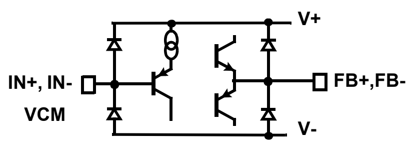


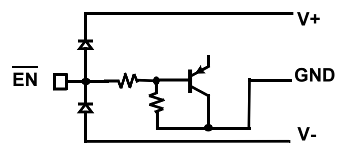
FIGURE 17. ENABLE TO OUTPUT DELAY

Pin Descriptions

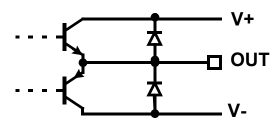
PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	PIN FUNCTION
1, 6, 9, 12, 15	NC		No connect; grounded for best AC performance
2	FB+	Circuit1	Feedback from non-inverting output
3	IN+	Circuit 1	Non-inverting input
4	GND	Circuit 4	Ground
5	VCM	Circuit 1	Reference input, sets common-mode output voltage with AV = 1. Must be st to V+/2 for single supply applications
7	V-	Circuit 4	Negative supply. Must be connected to GND for single supply operation
8	$\overline{EN}$	Circuit 2	Enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state
10	IN-	Circuit 1	Inverting input
11	FB-	Circuit 1	Feedback from inverting output
13	OUT-	Circuit 3	Inverting output
14	V+	Circuit 4	Positive supply
16	OUT+	Circuit 3	Non-inverting output
Thermal Pad		Circuit 5	Pack thermal pad electrically connected to IC substrate - must be connected to most negative voltage applied to the IC



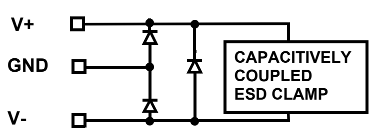
CIRCUIT 1



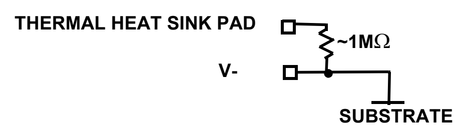
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4.



CIRCUIT 5

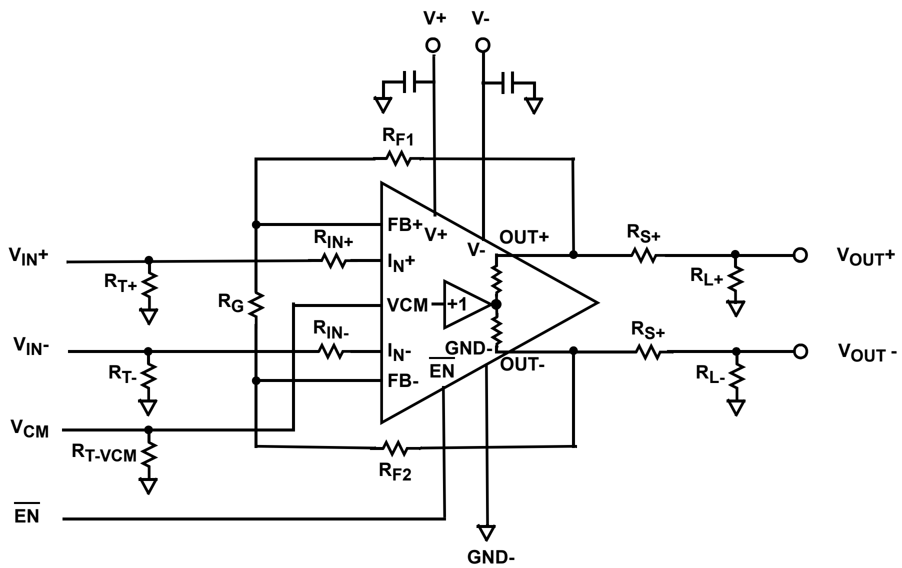


FIGURE 18. BASIC APPLICATION CIRCUIT

Description of Operation and Application Information

Product Description

The ISL55020 is a full differential Current Feedback Amplifier (CFA) featuring wide bandwidth and low power. The device contains a pair of high impedance differential inputs and a pair of differential outputs. It can be used in any combination of single/differential ended input/output configurations. A wide bandwidth unity gain, common mode amplifier with a 100MHz -3dB bandwidth (Figure 6) is included to provide DC offset correction or common mode signal injection to the differential output. The ISL55020 is internally compensated for single-ended closed loop gain (A_{VS}), differential closed gain (A_{VD}) of 2, or greater. Connected in differential gain of 5 (single ended gain of ±2.5 and driving a 200Ω differential load, the ISL55020 has a -3dB bandwidth of 300MHz. Driving a 200Ω differential load at gain of 10, the bandwidth is about 200MHz (Figure 3). The ISL55020 is available with a power down feature ($\overline{EN}$) to reduce the power while the amplifier is disabled.

Input, Output, and Supply Voltage Range

The ISL55020 is designed to operate with dual supplies over a range of +/-2.25V to +/-6V and can also operate with a single supply over the range of 4.5V to 12V. For single supply operation, the V- and GND pins must be connected together as close to the device as possible. The amplifiers have an input common mode voltage range from -4.3V to 3.4V when operated from ±5V supplies. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the VCM pin is from -3.3V to 3.7V. If the input common mode or differential mode signal is outside the above-specified ranges, the output signal will be distorted.

The output of the ISL55020 can swing from -3.8V to +3.8V at 100Ω differential load at ±5V supply. As the load resistance becomes lower, the output swing is reduced.

Single-ended, Differential and Common Mode Gain Settings

The ISL55020 can be used as a single/differential ended to differential/single converter. The voltage applied at VCM pin sets the output common mode voltage and the common mode gain is fixed at gain is one (A_{VCM} = 1).

The output differential voltage is given by the following:

$$V_{OD} = (V_{IN+} - V_{IN-}) \times (1 + 2R_F/R_G) \quad \text{(EQ. 1)}$$

Where:

$R_{F1} = R_{F2} = R_F$

The differential output gain (A_{VD}) is defined by the feedback resistors according to the following

$$A_{VD} = 1 + 2R_F/R_G \quad \text{(EQ. 2)}$$

The single ended output voltage (V_{OS}) contains a common mode component (V_{CM}) and a differential mode component equal to one-half the differential output (V_{OD}/2)., and is given by the following:

$$V_{OS} = V_{OD}/2 + V_{CM} = V_{CM} + (V_{IN+} - V_{IN-}) \times (0.5 + R_F/R_G) \quad \text{(EQ. 3)}$$

and the single-ended gain becomes:

$$A_{VS} = 0.5 + R_F/R_G \quad \text{(EQ. 4)}$$

Feedback Resistor, Gain Bandwidth Product and Stability Considerations *(See Figure 18 - Basic Application Schematic)*

For gains greater than 1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes lower in frequency, the amplifier's phase margin is reduced. Excessive parasitic capacitance at the input will cause excessive ringing in the time domain and peaking in the frequency domain. High feedback resistor values have the same effect, and therefore should be kept as low as possible. Figure 5 shows the gain-peaking effect of using higher feedback resistor values. Feedback resistor R_F has some maximum value that should not be exceeded for optimum performance.

Unlike voltage feedback (VFA) amplifier topologies that exhibit constant gain-bandwidth product, CFA amplifiers maintain high bandwidth at gains high greater than 1. Figure 3 illustrates the nearly constant bandwidth from a single-ended gain (A_{VS}) of 2.5 to 5, and only a slight reduction out to a A_{VS} of 50. For the gains other than 1, optimum response is obtained with R_F between 500Ω to 1kΩ.

The high impedance inputs IN+ and IN- are sensitive parasitic capacitance and inductance. To ensure input stability, a small value resistor (200Ω recommended) should be placed as close to the device IN+ and IN- pins as possible.

Driving Capacitive Loads and Cables

Excessive output capacitance also contributes to gain peaking (Figure 2) and high overshoot in pulse applications. For PC board layouts requiring long traces at the output, a small series resistor (Figure 17 - R_{S+}, R_{S-} usually between 5Ω to 50Ω) should be inserted as close to the device output pin as possible to each to minimize peaking,. The resultant gain error should be compensated with an appropriate adjustment of R_G.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor (R_S) at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The ISL55020 can be disabled with it's outputs in a high impedance state. The turn off time is about 250nS and the turn on time is about 12nS (Figure 17). When disabled, the amplifier's supply current is reduced to 1.4mA for I_S+ and -1.6mA for I_S- typically. The amplifier's power down can be controlled by standard ground-referenced CMOS signal levels at the $\overline{EN}$ pin. V.

Output Drive Capability

The ISL55020 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.internal short circuit protection.

Power Dissipation

With the high output drive capability of the ISL55020, It is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

A thermal shutdown circuit is included that implements a thermal shutdown if the junction temperature exceeds ~+185°C. The thermal shutdown includes thermal hysteresis of ~+15°C. The thermal shutdown feature is designed to protect the device during accidental overload conditions and continuous operation at junction temperatures greater than +150°C should never be allowed.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = V_S \times I_{SMAX} + V_S \times \frac{\Delta V_O}{R_{LD}}$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current per channel

ΔV_O = Maximum differential output voltage of the application

R_{LD} = Differential load resistance

I_{LOAD} = Load current

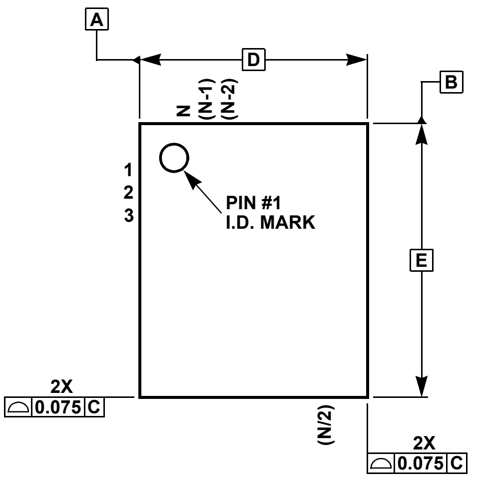
By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

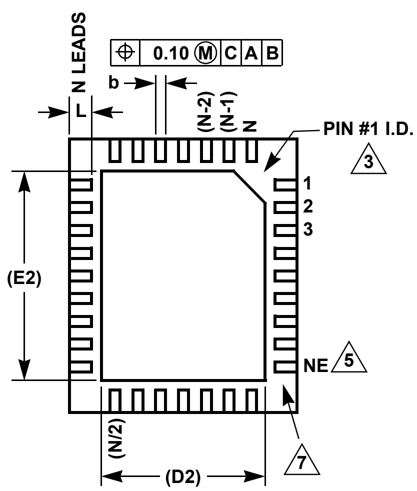
As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as sort as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

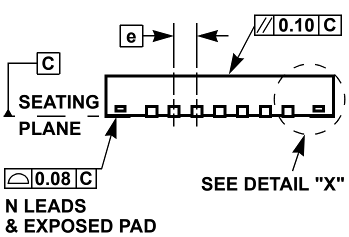
QFN (Quad Flat No-Lead) Package Family



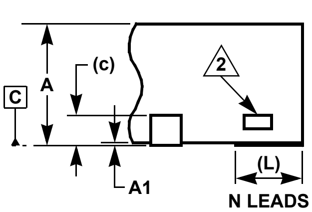
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	QFN44	QFN38	QFN32		TOLERANCE	NOTES
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	QFN28	QFN24	QFN20		QFN16	TOLER-ANCE	NOTES
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

Rev 10 12/04

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

RENESAS

NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

DATASHEET

ISL55020

Wideband, Low Distortion, Differential Amplifier

FN6287
Rev 0.00
December 18, 2006

The ISL55020 is fully differential wideband amplifier designed to drive differential ADCs. This device features a high drive capability of 100mA, low operating quiescent current of 21mA and operates with both single and dual supplies over a range of 4.5V (±2.25V) to +12V (±6V). Key features include high impedance, full differential inputs and full differential or DC referenced complementary single-ended outputs A wide bandwidth unity gain common mode (VCM) amplifier input is included to provide DC offset correction or common mode signal injection to the differential output.

The ISL55020 is available in the thermally-enhanced 16 Ld QFN package and is specified for operation over the full -40°C to +85°C temperature range. The ISL55020 has an $\overline{EN}$ pin to disable the outputs.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55020IRZ	55020IRZ	-	16 Ld QFN	MDP0046
ISL55020IRZ-T13	55020IRZ	13"	16 Ld QFN	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

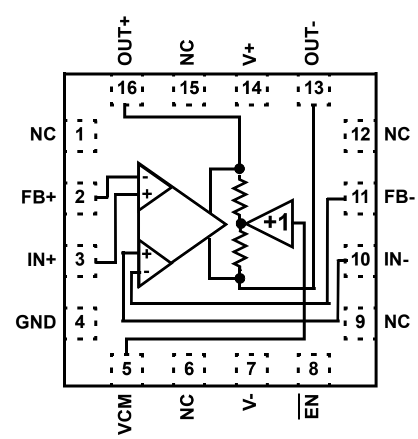
- Fully differential current feedback amplifier
- High impedance differential inputs
- Differential output drives up to 100mA from a +12V supply
- Separate unity-gain common mode input (VCM)
- 300MHz bandwidth
- 1200V/µs Slewrate
- -73.3dBc typical driver output distortion at $10V_{PP}$; 1MHz
- -64.6dBc typical driver output distortion at $10V_{PP}$; 4MHz
- Low quiescent supply current of 21mA
- Pb-free plus anneal available (RoHS compliant)

Applications

- High Linearity ADC preamplifier
- Differential driver
- Wireless communication receiver
- Differential active filter

Pinout

ISL55020
(16 LD QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

V+ Voltage to Ground or V- . . . . -0.3V to +13.2V
V- Voltage to Ground or V+ . . . . +0.3V to -13.2V
IN+, IN-, FB+, FB-, VCM, EN Voltage . . . . V- -0.3V to V+ +0.3V
Current into any Input 8mA
Continuous Output Current 100mA
ESD Tolerance
Human Body Model 3kV
Machine Model. 200V

Thermal Information

Thermal Resistance θ_{JA} (°C/W)
16 Ld QFN Package 40
Ambient Operating Temperature Range . . . .-40°C to +85°C
Storage Temperature Range . . . .-60°C to +150°C
Operating Junction Temperature . . . . +150°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 12V, R_F = 750Ω, R_G = 1.5kΩ, R_L = 1kΩ connected to mid supply, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
V_{OS}	Common Mode Offset Voltage		-38	15	38	mV
ΔV_{OS}	V_{OS} Mismatch		-7	0.7	7	mV
INPUT CHARACTERISTICS						
I_B+, I_B-	Non-Inverting Input Bias Current		-7		7	µA
F_B+, F_B-	Inverting Input Bias Current		-125	25	125	µA
ΔI_B-	I_B- Mismatch		-75	0	75	µA
e_N	Input Noise Voltage	f_O = 1kHz		9.8		nV/√Hz
		f_O = 10kHz		6.9		nV/√Hz
i_N	Input Noise Current	f_O = 1kHz		6.6		pA/√Hz
		f_O = 10kHz		2.7		pA/√Hz
CMIR	Common Mode Input Range IN+, IN-		2		10	V
VCM						
I_B **VCM**	**VCM** Input Bias Current	VCM = 5V to 6V	-7		7	µA
VOS VCM	((VOUT+) + (VOUT -))/2	VCM, IN +, IN- = 0V, R_L = 1kΩ	-150		150	mV
VCM Av	Close Loop Gain	ΔVCM = 1V, VCM = 5V to 6V	0.87	0.95	1.03	V/V
CMIR	Common Mode Input Range VCM		2.3		9.7	V
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing (differential)	V_S = ±6V, R_L = 1kΩ differential load	±4.8	±5.0		V
		V_S = 4.5V, R_L = 1kΩ differential load	±1.05			V
I_{OUT}	Output Current	R_L = 0Ω differential load		±150		mA
		R_L = 50Ω differential load	±1.45			mA
SUPPLY						
V_S	Supply Voltage	Single supply	4.5		12	V
I_S+ ENABLE	Positive Supply Current	All outputs at 0V, EN = 0V	14	21	28	mA
IS- ENABLE	Negative Supply	All outputs at 0V, EN = 0V	-28	-21	-14	mA
I_S+ DISABLE	Positive Supply Current	All outputs at 0V, EN = 5V	0.5	1.4	2.5	mA
IS- DISABLE	Negative Supply	All outputs at 0V, EN = 5V	-2.5	-1.6	0.5	mA
Ts	Thermal Shutdown Temperature	IC Junction Temperature		185		°C
Ts-hys	Thermal Shutdown Hysteresis	IC Junction Shutdown Hysteresis		15		°C

Electrical Specifications V_S = 12V, R_F = 750Ω, R_G = 1.5kΩ, R_L = 1kΩ connected to mid supply, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC						
V_{INH}, $\overline{EN}$	ENABLE High Level		2			V
V_{INL}, $\overline{EN}$	ENABLE Low Level				0.8	V
I_{INH}, $\overline{EN}$	Input Current, High	$\overline{ENABLE}$ = 5V	180	250	320	µA
I_{INL}, $\overline{EN}$	Input Current, Low	$\overline{ENABLE}$ = 0V	-5		+5	µA
$t_{\overline{EN}}$ ON	Enable time, off to on	$\overline{ENABLE}$ = 5V to 0V		12		nS
t$\overline{EN}$ OFF	Disable time, on to off	$\overline{ENABLE}$ = 0V to 5V		250		nS
R_{IN}	IN+, IN- Input resistance disables state	V+ = 12V, Vin = 2V to 10V, $\overline{ENABLE}$ = 5V	1			MΩ
		V+ = 4.5V,Vin = 2V to 4V, $\overline{ENABLE}$ = 5V	1			MΩ
AC PERFORMANCE						
BW	-3dB Bandwidth, single-ended output to GND (Figure 3)	A_{VS} = +2.5, R_F = 750Ω, R_G = 374Ω, RL=100Ω		300		MHz
		A_{VS} = 5, R_F = 750Ω, R_G = 169Ω, RL=100Ω		200		MHz
THD, HD2, HD3	THD, A = 2; Differential	f = 1MHz, V_O = $1V_{P-P}$, R_L = 1kΩ		-63.8		dBc
		f = 1MHz, V_O = $10V_{P-P}$, R_L = 1kΩ		-73.3		dBc
		f = 4MHz, V_O = $1V_{P-P}$, R_L = 1kΩ		-57.4		dBc
		f = 4MHz, V_O = $10V_{P-P}$, R_L = 1kΩ		-62.4		dBc
	HD2, A_V = 2; Differential	f = 1MHz, V_O = $1V_{P-P}$, R_L = 1kΩ		-82.3		dBc
		f = 1MHz, V_O = $10V_{P-P}$, R_L = 1kΩ		77.6		dBc
		f = 4MHz, V_O = $1V_{P-P}$, R_L = 1kΩ		-62.3		dBc
		f = 4MHz, V_O = $10V_{P-P}$, R_L = 1kΩ		-64.6		dBc
	HD3, A_V = 2; Differential	f = 1MHz, V_O = $1V_{P-P}$, R_L = 1kΩ		-68.5		dBc
		f = 1MHz, V_O = $10V_{P-P}$, R_L = 1kΩ		-83.5		dBc
		f = 4MHz, V_O = $1V_{P-P}$, R_L = 1kΩ		-60.3		dBc
		f = 4MHz, V_O = $10V_{P-P}$, R_L = 1kΩ		-67.7		dBc
SR	Slew Rate, Single-ended	V_{OUT} from -3V to +3V, R_L = 1kΩ	600	1200		V/µs

Typical Performance Curves

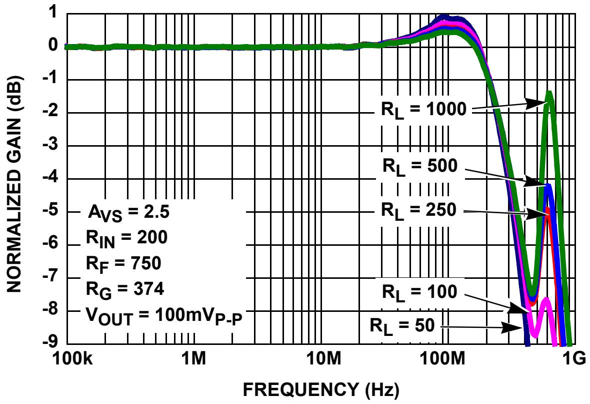


FIGURE 1. SINGLE-ENDED GAIN vs FREQUENCY vs R_L

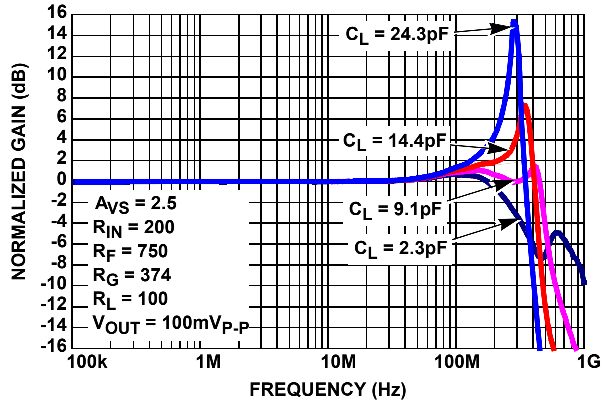


FIGURE 2. SINGLE-ENDED GAIN vs FREQUENCY vs C_L

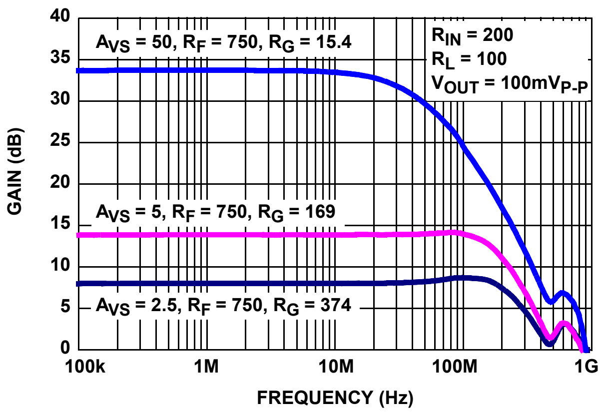


FIGURE 3. CLOSED LOOP GAIN vs FREQUENCY

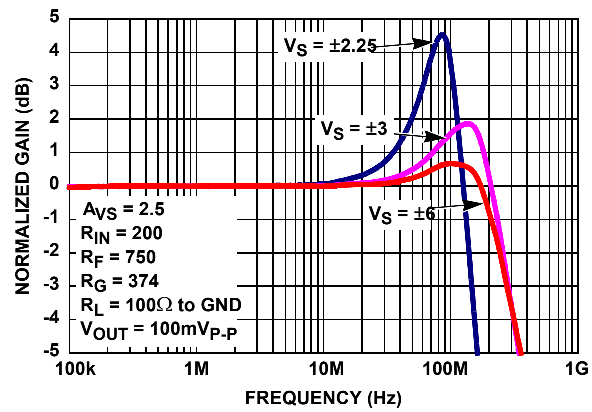


FIGURE 4. SINGLE-ENDED GAIN vs FREQUENCY vs V_S

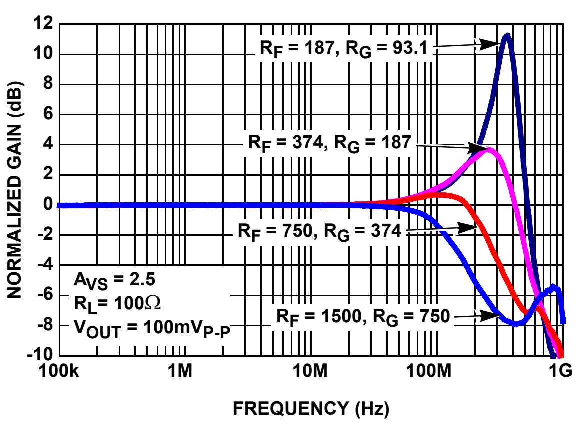


FIGURE 5. SINGLE-ENDED GAIN vs FREQUENCY vs R_F/R_G

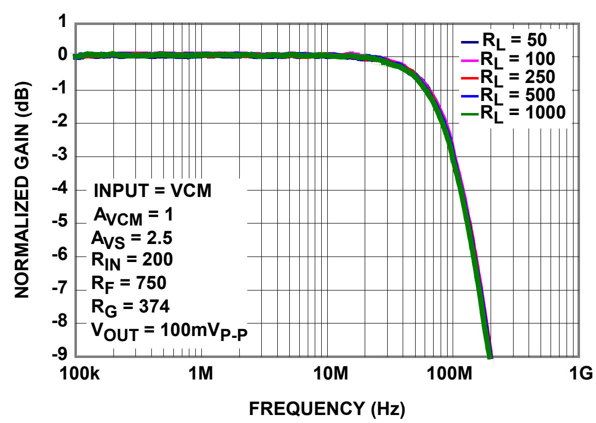


FIGURE 6. VCM GAIN vs FREQUENCY vs R_L

Typical Performance Curves (Continued)

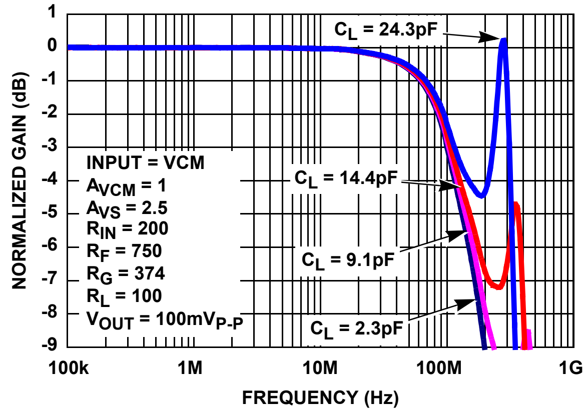


FIGURE 7. VCM GAIN vs FREQUENCY vs CL

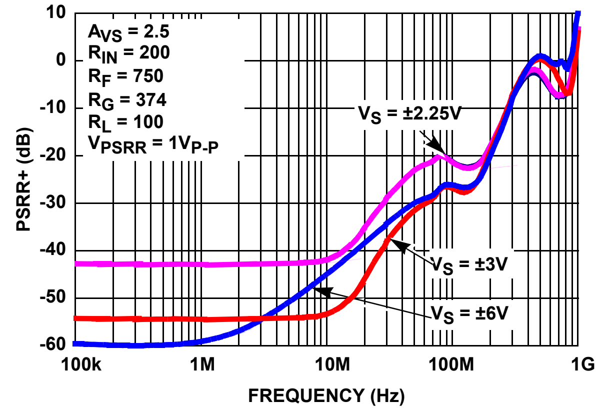


FIGURE 8. PSRR+ vs FREQUENCY vs V_S (DUAL SUPPLIES)

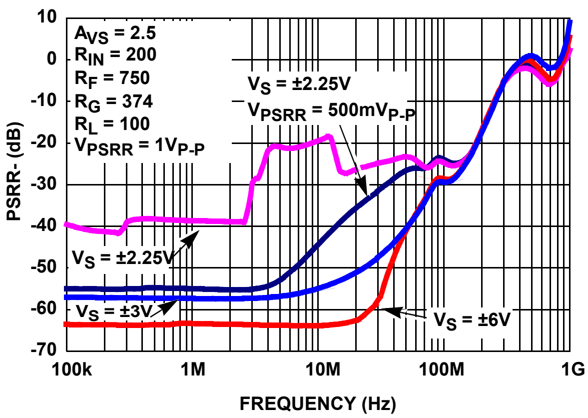


FIGURE 9. PSRR- vs FREQUENCY vs V_S

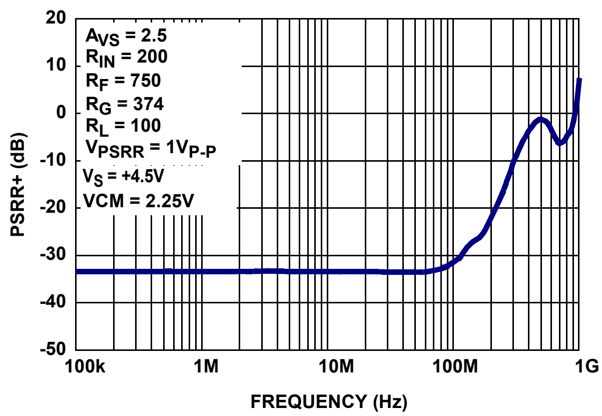


FIGURE 10. PSRR+ vs FREQUENCY vs V_S (SINGLE SUPPLY)

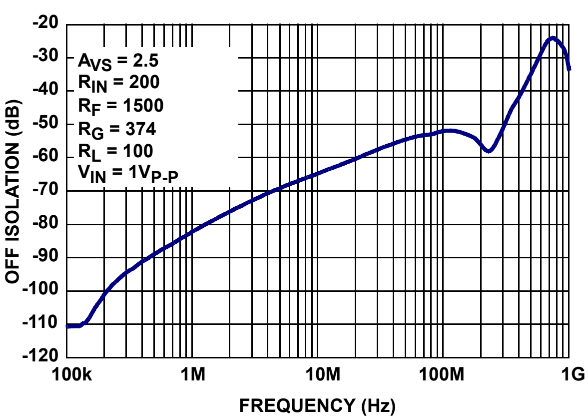


FIGURE 11. INPUT OFF ISOLATION GAIN vs FREQUENCY SINGLE-ENDED

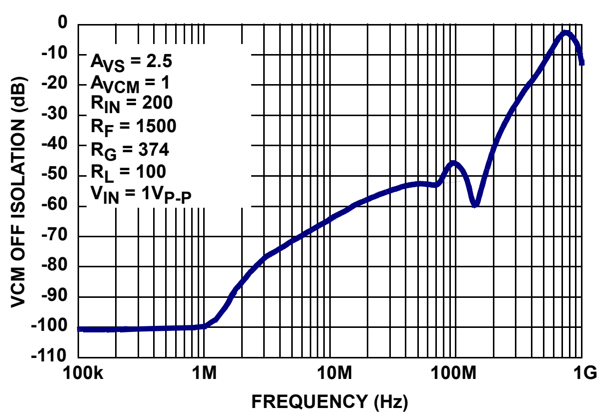


FIGURE 12. VCM OFF ISOLATION vs FREQUENCY - SINGLE-ENDED

Typical Performance Curves (Continued)

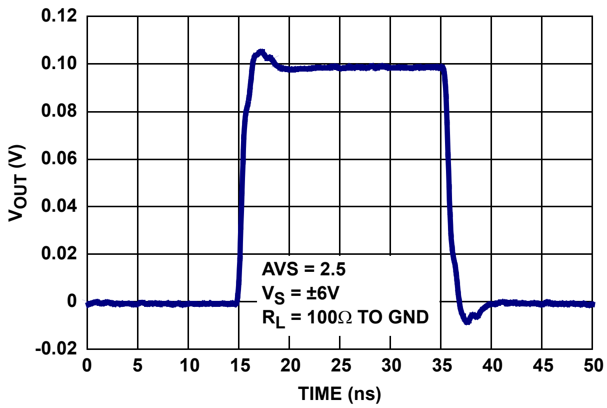


FIGURE 13. SMALL SIGNAL STEP RESPONSE

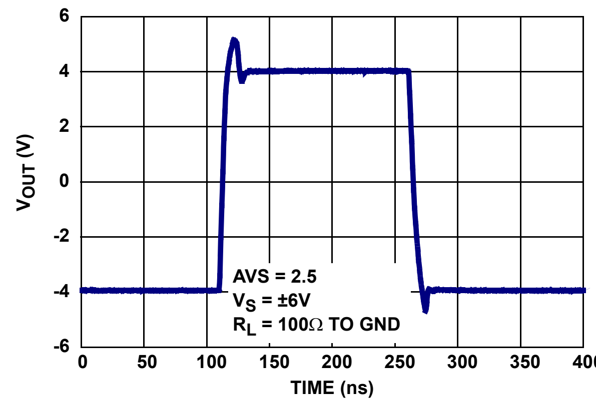


FIGURE 14. LARGE SIGNAL STEP RESPONSE

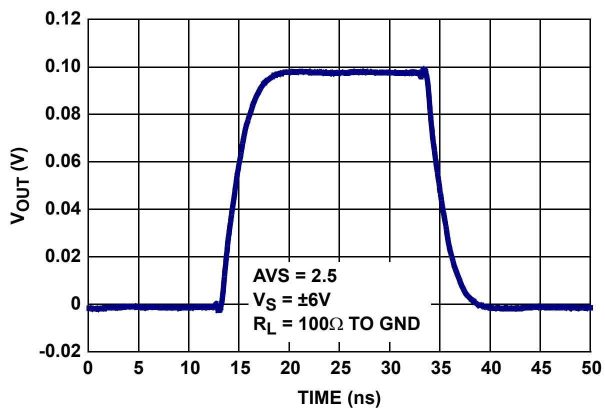


FIGURE 15. SMALL SIGNAL STEP RESPONSE - VCM TO V_{OUT}

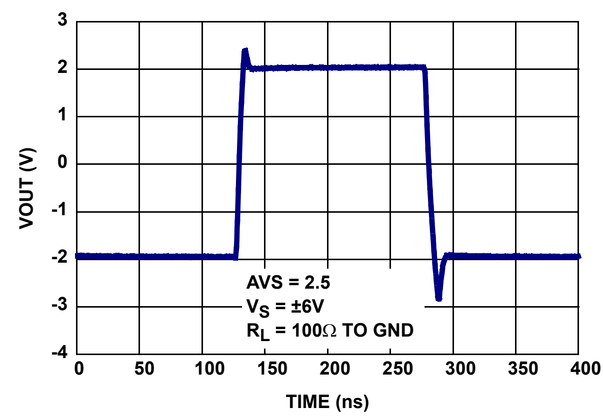


FIGURE 16. LARGE SIGNAL STEP RESPONSE - VCM TO V_{OUT}

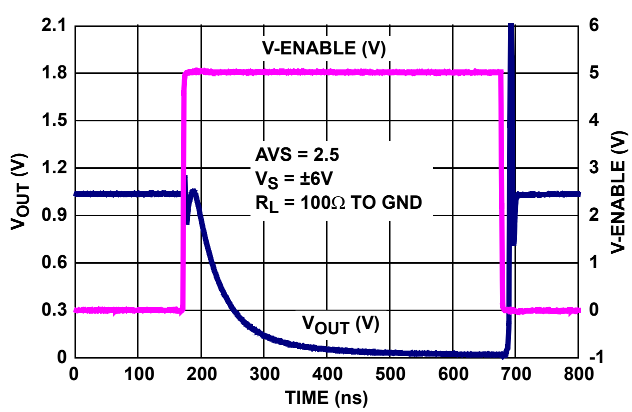
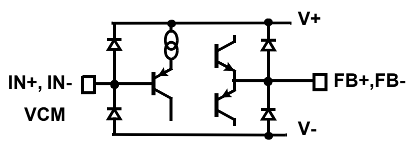


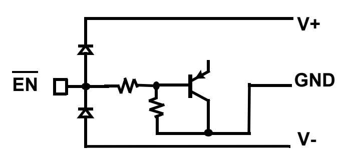
FIGURE 17. ENABLE TO OUTPUT DELAY

Pin Descriptions

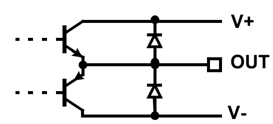
PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	PIN FUNCTION
1, 6, 9, 12, 15	NC		No connect; grounded for best AC performance
2	FB+	Circuit1	Feedback from non-inverting output
3	IN+	Circuit 1	Non-inverting input
4	GND	Circuit 4	Ground
5	VCM	Circuit 1	Reference input, sets common-mode output voltage with AV = 1. Must be st to V+/2 for single supply applications
7	V-	Circuit 4	Negative supply. Must be connected to GND for single supply operation
8	$\overline{EN}$	Circuit 2	Enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state
10	IN-	Circuit 1	Inverting input
11	FB-	Circuit 1	Feedback from inverting output
13	OUT-	Circuit 3	Inverting output
14	V+	Circuit 4	Positive supply
16	OUT+	Circuit 3	Non-inverting output
Thermal Pad		Circuit 5	Pack thermal pad electrically connected to IC substrate - must be connected to most negative voltage applied to the IC



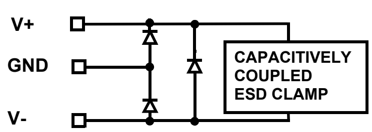
CIRCUIT 1



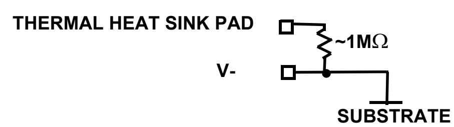
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4.



CIRCUIT 5

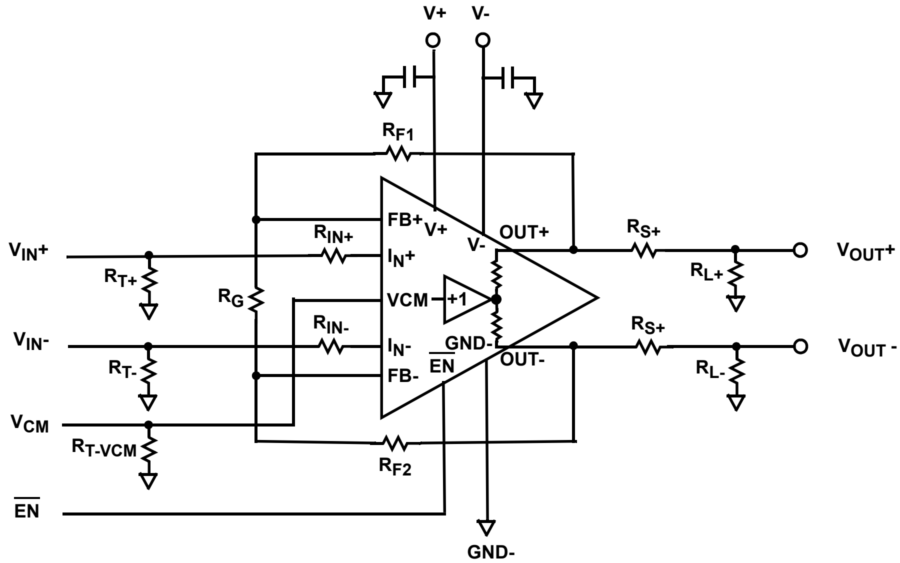


FIGURE 18. BASIC APPLICATION CIRCUIT

Description of Operation and Application Information

Product Description

The ISL55020 is a full differential Current Feedback Amplifier (CFA) featuring wide bandwidth and low power. The device contains a pair of high impedance differential inputs and a pair of differential outputs. It can be used in any combination of single/differential ended input/output configurations. A wide bandwidth unity gain, common mode amplifier with a 100MHz -3dB bandwidth (Figure 6) is included to provide DC offset correction or common mode signal injection to the differential output. The ISL55020 is internally compensated for single-ended closed loop gain (A_{VS}), differential closed gain (A_{VD}) of 2, or greater. Connected in differential gain of 5 (single ended gain of ±2.5 and driving a 200Ω differential load, the ISL55020 has a -3dB bandwidth of 300MHz. Driving a 200Ω differential load at gain of 10, the bandwidth is about 200MHz (Figure 3). The ISL55020 is available with a power down feature ($\overline{EN}$) to reduce the power while the amplifier is disabled.

Input, Output, and Supply Voltage Range

The ISL55020 is designed to operate with dual supplies over a range of +/-2.25V to +/-6V and can also operate with a single supply over the range of 4.5V to 12V. For single supply operation, the V- and GND pins must be connected together as close to the device as possible. The amplifiers have an input common mode voltage range from -4.3V to 3.4V when operated from ±5V supplies. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the VCM pin is from -3.3V to 3.7V. If the input common mode or differential mode signal is outside the above-specified ranges, the output signal will be distorted.

The output of the ISL55020 can swing from -3.8V to +3.8V at 100Ω differential load at ±5V supply. As the load resistance becomes lower, the output swing is reduced.

Single-ended, Differential and Common Mode Gain Settings

The ISL55020 can be used as a single/differential ended to differential/single converter. The voltage applied at VCM pin sets the output common mode voltage and the common mode gain is fixed at gain is one (A_{VCM} = 1).

The output differential voltage is given by the following:

$$V_{OD} = (V_{IN+} - V_{IN-}) \times (1 + 2R_F/R_G) \quad \text{(EQ. 1)}$$

Where:

$R_{F1} = R_{F2} = R_F$

The differential output gain (A_{VD}) is defined by the feedback resistors according to the following

$$A_{VD} = 1 + 2R_F/R_G \quad \text{(EQ. 2)}$$

The single ended output voltage (V_{OS}) contains a common mode component (V_{CM}) and a differential mode component equal to one-half the differential output (V_{OD}/2)., and is given by the following:

$$V_{OS} = V_{OD}/2 + V_{CM} = V_{CM} + (V_{IN+} - V_{IN-}) \times (0.5 + R_F/R_G) \quad \text{(EQ. 3)}$$

and the single-ended gain becomes:

$$A_{VS} = 0.5 + R_F/R_G \quad \text{(EQ. 4)}$$

Feedback Resistor, Gain Bandwidth Product and Stability Considerations *(See Figure 18 - Basic Application Schematic)*

For gains greater than 1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes lower in frequency, the amplifier's phase margin is reduced. Excessive parasitic capacitance at the input will cause excessive ringing in the time domain and peaking in the frequency domain. High feedback resistor values have the same effect, and therefore should be kept as low as possible. Figure 5 shows the gain-peaking effect of using higher feedback resistor values. Feedback resistor R_F has some maximum value that should not be exceeded for optimum performance.

Unlike voltage feedback (VFA) amplifier topologies that exhibit constant gain-bandwidth product, CFA amplifiers maintain high bandwidth at gains high greater than 1. Figure 3 illustrates the nearly constant bandwidth from a single-ended gain (A_{VS}) of 2.5 to 5, and only a slight reduction out to a A_{VS} of 50. For the gains other than 1, optimum response is obtained with R_F between 500Ω to 1kΩ.

The high impedance inputs IN+ and IN- are sensitive parasitic capacitance and inductance. To ensure input stability, a small value resistor (200Ω recommended) should be placed as close to the device IN+ and IN- pins as possible.

Driving Capacitive Loads and Cables

Excessive output capacitance also contributes to gain peaking (Figure 2) and high overshoot in pulse applications. For PC board layouts requiring long traces at the output, a small series resistor (Figure 17 - R_{S+}, R_{S-} usually between 5Ω to 50Ω) should be inserted as close to the device output pin as possible to each to minimize peaking,. The resultant gain error should be compensated with an appropriate adjustment of R_G.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor (R_S) at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The ISL55020 can be disabled with it's outputs in a high impedance state. The turn off time is about 250nS and the turn on time is about 12nS (Figure 17). When disabled, the amplifier's supply current is reduced to 1.4mA for I_S+ and -1.6mA for I_S- typically. The amplifier's power down can be controlled by standard ground-referenced CMOS signal levels at the $\overline{EN}$ pin. V.

Output Drive Capability

The ISL55020 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.internal short circuit protection.

Power Dissipation

With the high output drive capability of the ISL55020, It is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

A thermal shutdown circuit is included that implements a thermal shutdown if the junction temperature exceeds ~+185°C. The thermal shutdown includes thermal hysteresis of ~+15°C. The thermal shutdown feature is designed to protect the device during accidental overload conditions and continuous operation at junction temperatures greater than +150°C should never be allowed.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = V_S \times I_{SMAX} + V_S \times \frac{\Delta V_O}{R_{LD}}$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current per channel

ΔV_O = Maximum differential output voltage of the application

R_{LD} = Differential load resistance

I_{LOAD} = Load current

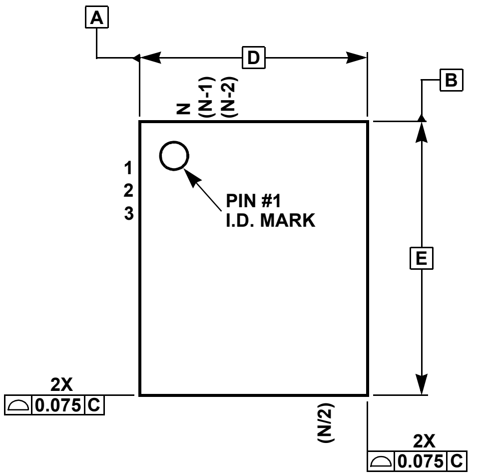
By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

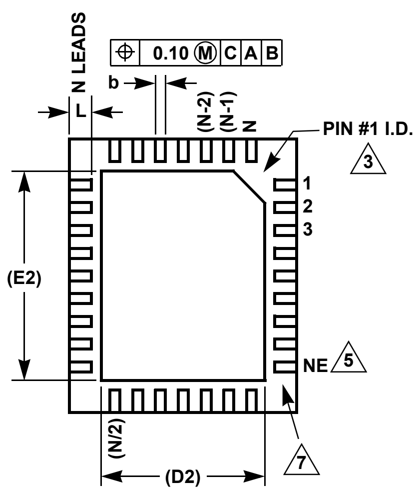
As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as sort as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

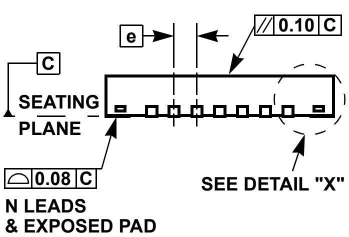
QFN (Quad Flat No-Lead) Package Family



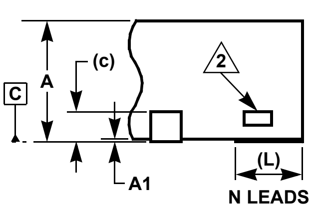
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	QFN44	QFN38	QFN32		TOLERANCE	NOTES
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	QFN28	QFN24	QFN20		QFN16	TOLER-ANCE	NOTES
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

Rev 10 12/04

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.