CDP1853C/3

March 1997

High-Reliability CMOS N-Bit 1 of 8 Decoder

Features

- **Provides Direct Control of Up to 7 Input and 7 Output Devices When used with a CDP1800-Series Microprocessor**
- **CHIP ENABLE (CE) Allows Easy Expansion for Multi-level I/O Systems**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
SBDIP	-55^{o}C to +125^{o}C	CDP1853CD3	-	D16.3

Description

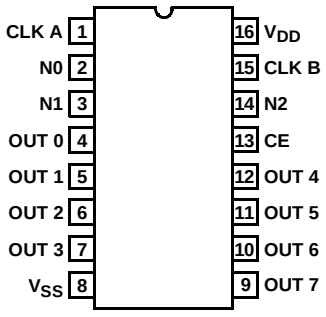
The CDP1853/3 and CDP1853C/3 are high-reliability 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-Series microprocessors without additional components. The CDP1853/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1853C/3 has a recommended operating voltage range of 4V to 6.5V.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Figure 2. The CDP1853/3 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to 1800-series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Figure 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Figure 6.

The CDP1853/3 can also be used as a general purpose 1 of 8 decoder for I/O and memory system applications as shown in Figure 4.

Pinout

16 LEAD SBDIP
TOP VIEW



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CDP1853/3 Functional Diagram

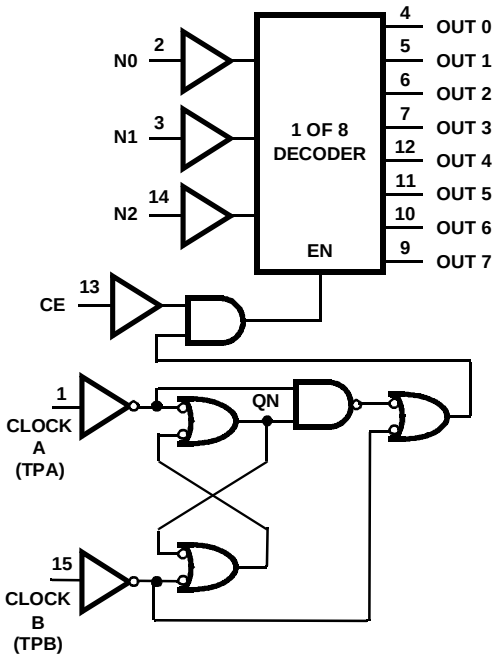


FIGURE 1.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1(Note 2)
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

NOTES:

1. 1 = High level, 0 = Low level, X = Don't care.
2. Qn-1 = Enable remains in previous state.

Static Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS			LIMITS				UNITS
					-55°C, +25°C		+125°C		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{SS} (Note 1)	-	0, 5	5	-50	-	-100	-	µA
		-	0, 10	10	-500	-	-1000	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	-	5	2.3	-	1.6	-	mA
		0.5	-	10	3.7	-	2.6	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	-	5	-	-1.7	-	-1.2	mA
		9.5	-	10	-	-3.7	-	-2.6	mA
Output Voltage Low-Level	V_{OL} (Note 2)	-	0, 5	5	-	0.1	-	0.2	V
		-	0, 10	10	-	0.1	-	0.2	V
Output Voltage High-Level	V_{OH} (Note 2)	-	0, 5	5	4.9	-	4.8	-	V
		-	0, 10	10	9.9	-	9.8	-	V
Input Low Voltage	V_{IL}	0.8, 4.2	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
Input High Voltage	V_{IH}	0.8, 4.2	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
Input Leakage Low	I_{IL}	-	0	5	-1	-	-5	-	µA
		-	0	10	-1	-	-5	-	µA
Input Leakage High	I_{IH}	-	5	5	-	1	-	5	µA
		-	10	10	-	1	-	5	µA
Input Capacitance	C_{IN} (Note 2)	-	-	-	-	10	-	10	pF
Output Capacitance	C_{OUT} (Note 2)	-	-	-	-	15	-	15	pF

NOTES:

1. The CDP1853C meets all 5V static electrical characteristics of the CDP1853 except quiescent device current for which the limits are: I_{SS} = -500µA at -55°C and +25°C and I_{SS} = -1000µA at +125°C.
2. Guaranteed but not tested.

Dynamic Electrical Specifications

See Figure 2, C_L = 100pF, t_R, t_F = 15ns

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Propagation Delay Time:	t_{EOH}	5	-	175	-	275	ns
Chip Enable (CE) to Output High		10	-	90	-	150	ns

Dynamic Electrical Specifications

See Figure 2, C_L = 100pF, t_R, t_F = 15ns

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Disable to Output Low	t_{EOL}	5	-	295	-	400	ns
		10	-	200	-	250	ns
N Input to Output	t_{NO}	5	-	225	-	315	ns
		10	-	120	-	165	ns
Clock A to Output Low	t_{AO}	5	-	210	-	300	ns
		10	-	110	-	150	ns
Clock B to Output Low	t_{BO}	5	-	295	-	400	ns
		10	-	200	-	250	ns
Pulse Width:	t_{CACA}	5	50	-	75	-	ns
Clock A		10	25	-	50	-	ns
Clock B	t_{CBCB}	5	50	-	75	-	ns
		10	25	-	50	-	ns

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1853/3		CDP1853C/3		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1853/3 . . . . . -0.5V to +11V
CDP1853C/3. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
SBDIP Package.	85	22

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55^{o}C to +125^{o}C
Storage Temperature Range (T_{STG}) . . . . . -65^{o}C to +150^{o}C
Lead Temperature (During Soldering)
At distance 1/16 □± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max. . . . . +265^{o}C

Timing Diagrams

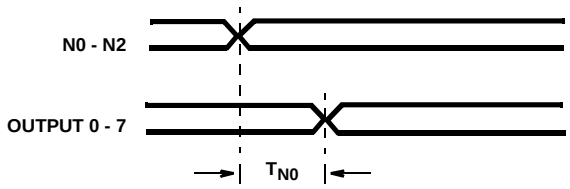


FIGURE 2A. N - INPUTS TO OUTPUTS DELAY TIME

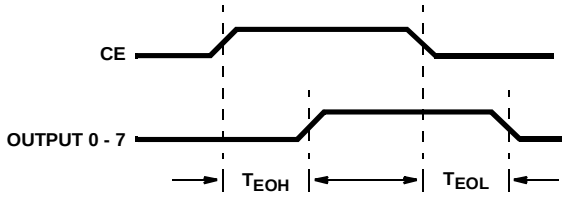


FIGURE 2B. CE TO OUTPUT DELAY TIME

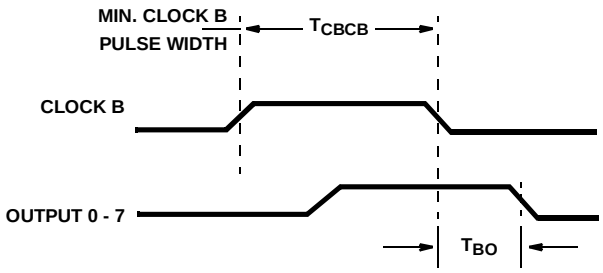
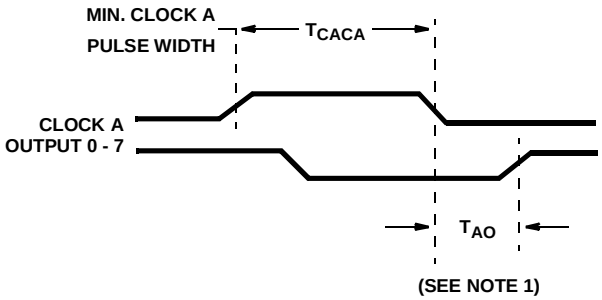


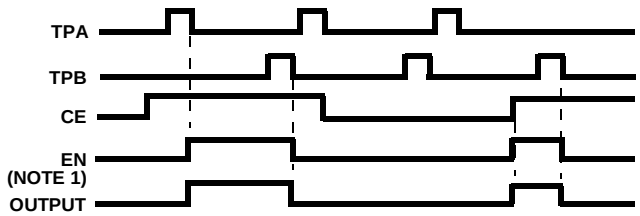
FIGURE 2C. CLOCK B TO OUTPUT DELAY TIME



NOTE:
1. To measure T_{AO}, Clock B must be tied low.

FIGURE 2D. CLOCK A TO OUTPUT DELAY TIME

FIGURE 2. PROPAGATION DELAY TIME DIAGRAMS



NOTE:
1. Output enabled when EN = high. Internal signal shown for reference only (see Figure 1).

FIGURE 3. TIMING DIAGRAM

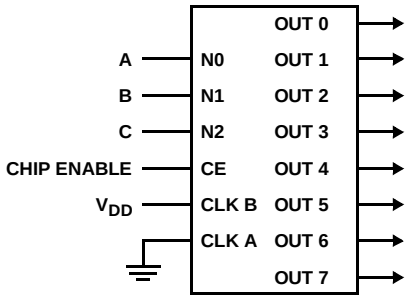


FIGURE 4. N-BIT DECODER USED AS A 1 OF 8 DECODER

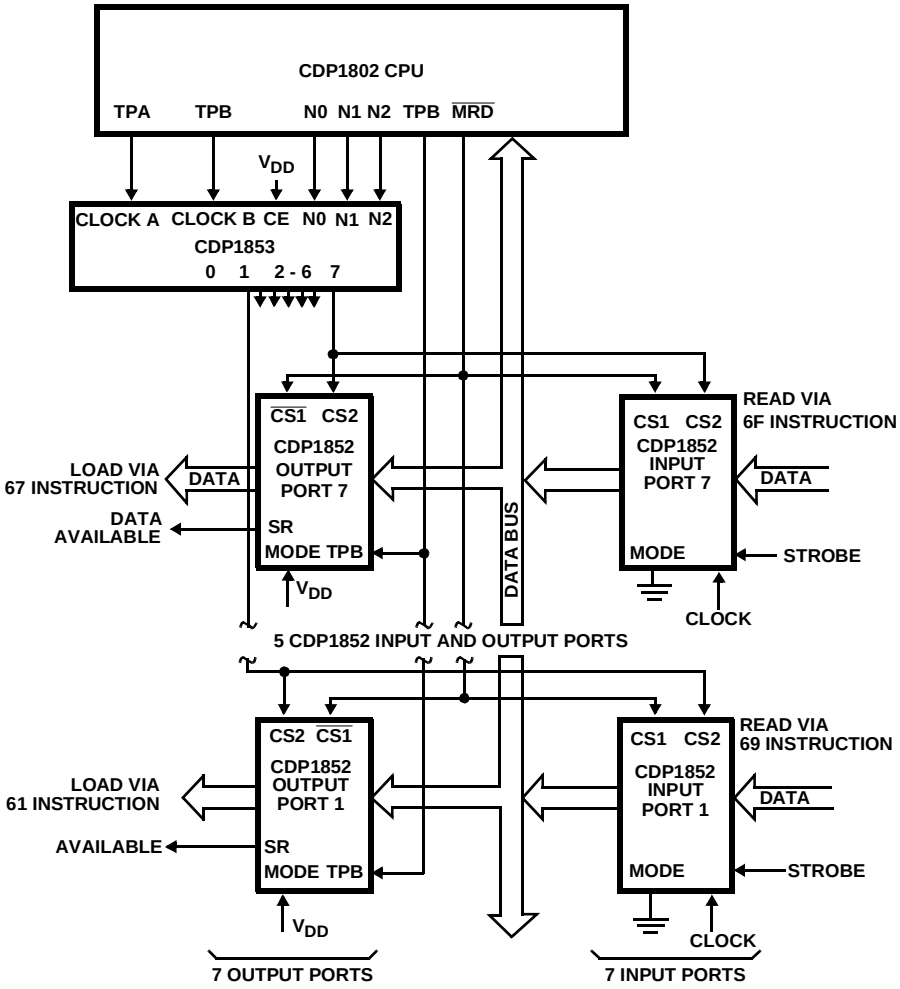
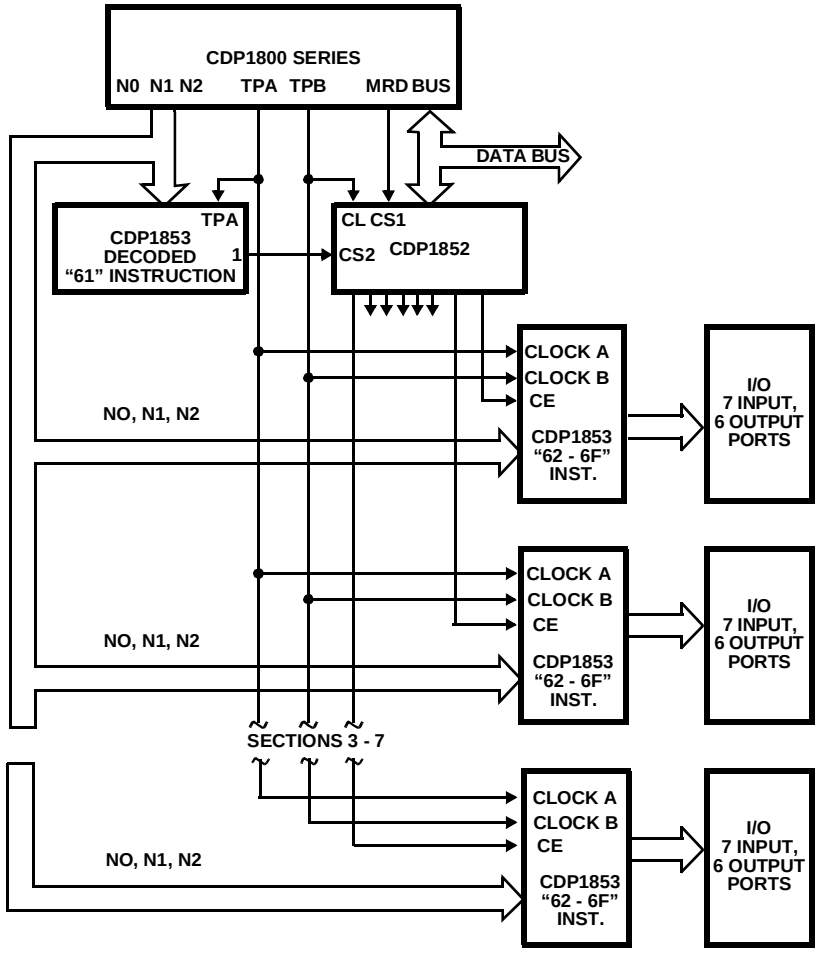


FIGURE 5. N-BIT DECODER IN A ONE LEVEL I/O SYSTEM

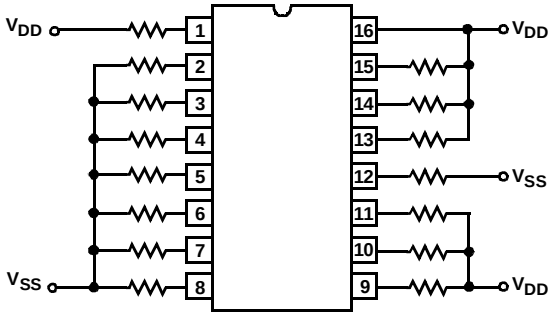


NOTE:

1. System shown will select up to 56 input and 48 output ports. With additional decoding, the total number of input and output ports can be further expanded.

FIGURE 6. TWO LEVEL I/O USING CDP1853 AND CDP1852

Bias/Static Burn-In Circuit



TYPE	V_{DD}	TEMPERATURE	TIME
CDP1853C	7V	+125°C	160 Hrs.

NOTE:

1. All resistors are 47kΩ ±20%.