DATA SHEET

Intel® Enpirion® Power Solutions

EM2260P01QI 60A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor, Featuring Digital Control with PMBus™ Compliant Interface

Description

The EM2260 is a fully integrated 60A PowerSoC synchronous dual-phase buck converter. It features an advanced digital controller, gate drivers, synchronous MOSFETs, and high-performance inductors. Only input and output filter capacitors and a few small signal components are required for a complete solution. A PMBus version 1.2 compliant interface provides setup, control, and telemetry.

Differential remote sensing and ±0.5% set-point accuracy provides precise regulation over line, load and temperature variation. Very low ripple further reduces accuracy uncertainty to provide best in class static regulation for today's FPGAs, ASICs, processors, and DDR memory devices.

The EM2260 can be configured and controlled in any application by two methods, either in pin-strap mode using onboard resistors, or using the PMBUS interface. The customer can also configure the device during engineering evaluation using the PMBUS interface, which offers a high degree of flexibility and programmability, and then use the pin strap mode when devices are deployed in production. Advanced digital control techniques ensure stability and excellent dynamic performance and eliminate the need for external compensation components. The Intel Enpirion Digital Power Configurator provides a user-friendly and easy-to-use interface for communicating with and configuring the device.

The EM2260 features high conversion efficiency and superior thermal performance to minimize thermal de-rating limitations, which is key to product reliability and longevity.

Features

- Integrated digital controller, inductors and FETs
- Wide 4.5V to 16V V_{IN} range
- 0.5V to 1.3V V_{OUT} range
- 60A continuous current with no thermal de-rating at 80ºC (12Vin, 0.9Vout)
- 23mm x 18mm x 5.0mm QFN package
- 88% efficiency at V_{IN} = 12V, V_{OUT} = 1.2V
- Meets all high-performance FPGA requirements
    - Digital loop for best in class transient response
    - 0.5% set-point over line, load, temperature
    - Output ripple as low as 10 mV peak-peak
    - Differential remote sensing
    - Monotonic startup into pre-bias output
    - Optimized FPGA configs stored in NVM
- Programmable through PMBus
    - V_{OUT} margining, startup and shutdown delays
    - Programmable warnings, faults and response
- Operational without PMBus
    - RVSET resistor for setting V_{OUT}
    - RTUNE resistor for single resistor based compensation
- Programmable Overcurrent Response
    - Latch Off (default)
    - Hiccup
- Tracking pin for complex sequencing
- RoHS compliant, MSL level 3, 260°C reflow

Applications

- High performance FPGA Core Supply
- ASIC and processor supply rails

Ordering Information

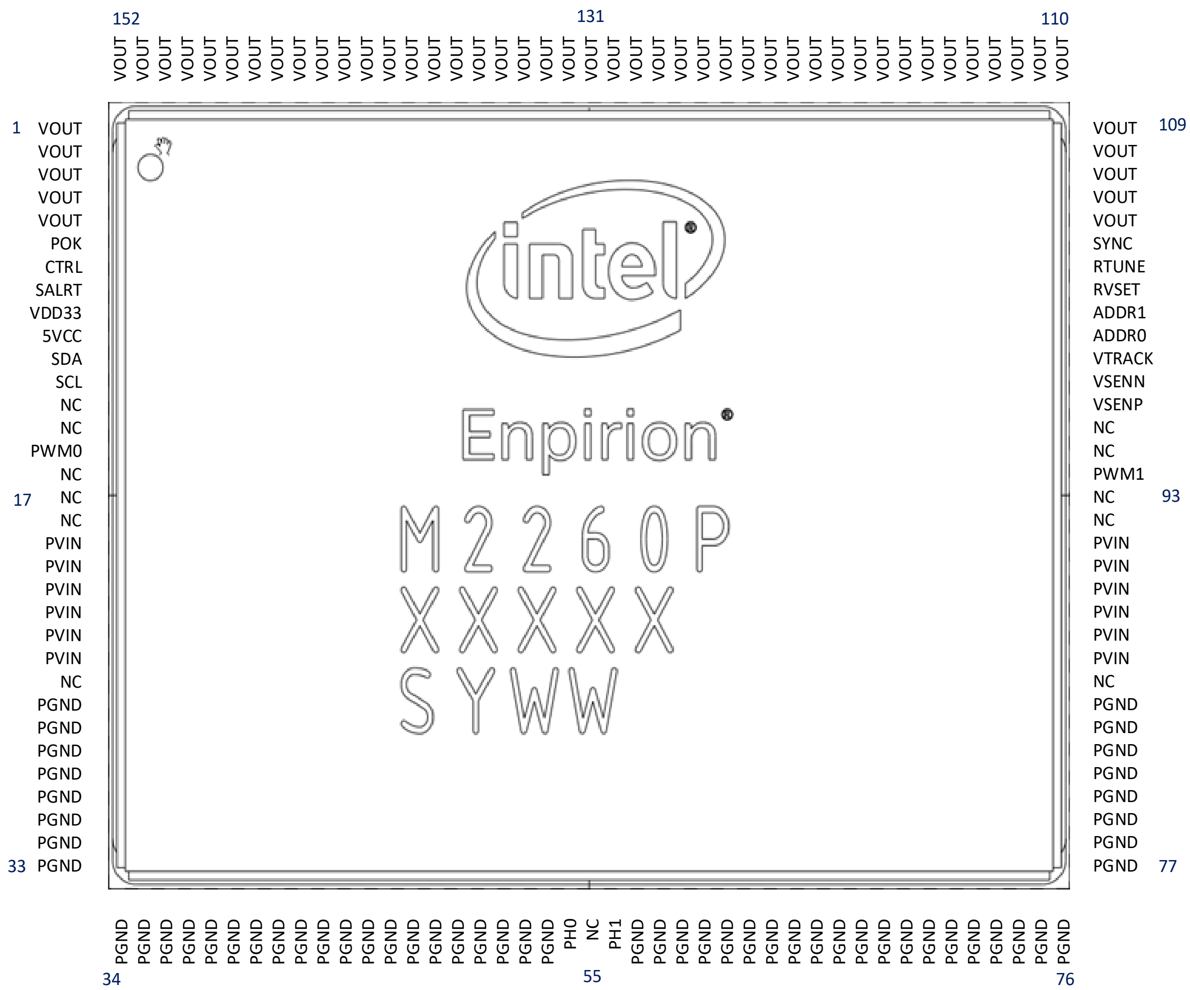
Table 1

Part Number	Supported V_{OUT} Range	Package Markings	Package Description
EM2260P01QI	0.5V to 1.3V	M2260P	18 mm x 23 mm x 5mm QFN152 provided in 48 units per tray
EVB-EM2260P01	0.5V to 1.3V	Evaluation board; 60A dual phase	
EVI-EM2COMIF	GUI interface dongle		

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments

Figure 1: Pin Out Diagram (Top side)



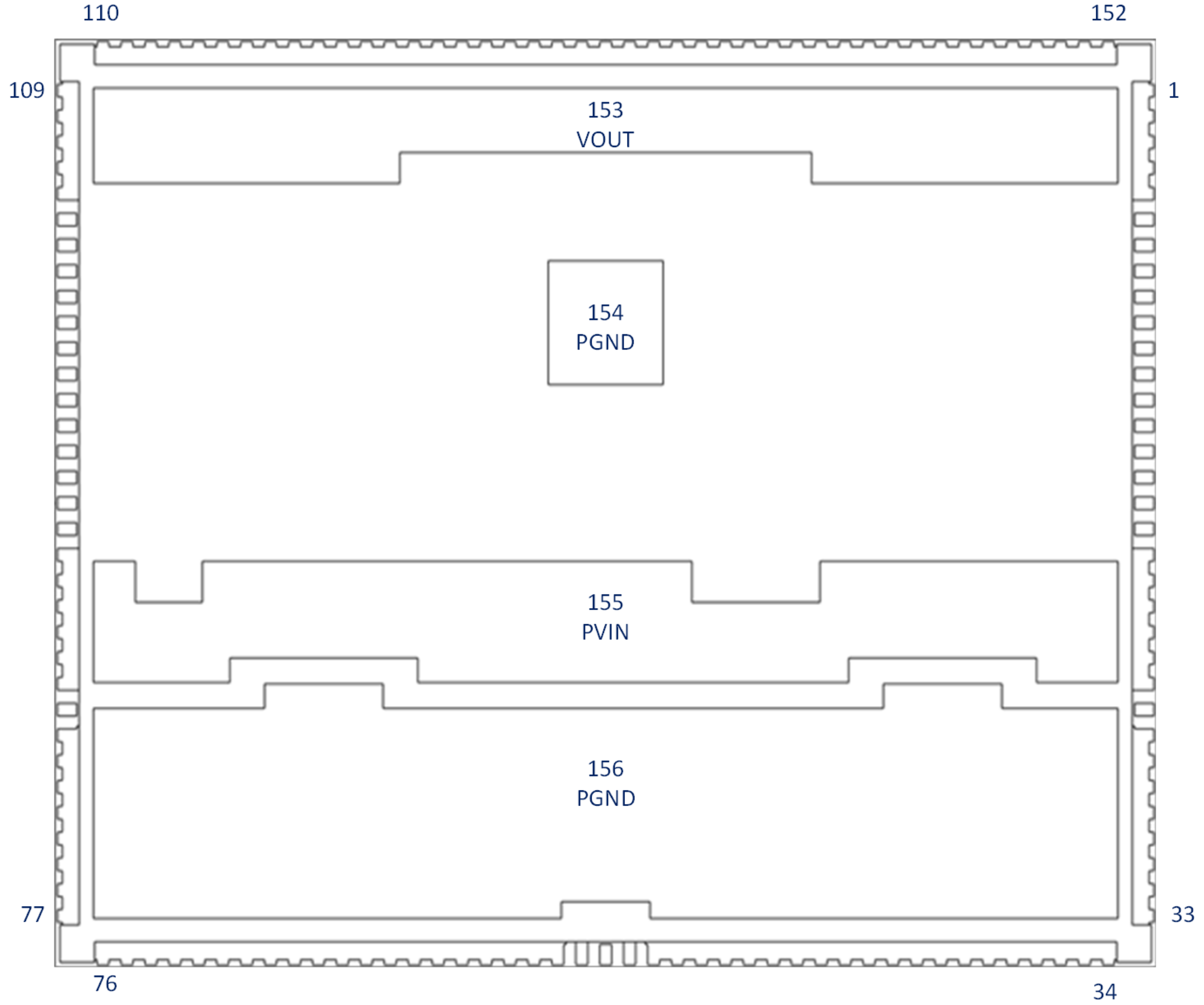


Figure 2: Pin Out Diagram Bottom side

Pin Description

Table 2

PIN	NAME	I/O	FUNCTION
1-5, 105-153	VOUT	Regulated Output	Regulated output voltage. Decouple to PGND with appropriate filter capacitors
6	POK	Digital I/O	Power OK is an open drain transistor for power system state indication. See the Power OK description for details.
7	CTRL	Digital Input	PMBus-compatible control pin with programmable functionality. CTRL should never be left floating if enabled in Configuration. The default configuration is for V_{OUT} to be on with CTRL high (positive edge)
8	SALRT	Digital Output	PMBus™ alert line.

PIN	NAME	I/O	FUNCTION
9	VDD33	Output	3.3V output of the internal LDO. May be used as pull-up supply for PMBus™ pins and CTRL pin.
10	VCC	Input Supply	5.0V supply voltage for analog circuitry.
11	SDA	Digital I/O	PMBus™ serial data I/O.
12	SCL	Digital Input	PMBus™ serial clock input.
15	PWM0	PWM	Phase 0 PWM signal test pin.
13-14, 16-18, 25, 55, 85, 92, 93, 95, 96	NC	NC	No connect. Do not connect to any signal, supply, or ground.
19-24, 86-91, 155	PVIN	Input Supply	Input supply for MOSFET switches. Decouple to PGND with appropriate filter capacitors. Refer to Recommended Application Circuit section for more details.
26-53, 57-84, 154,156	PGND	Ground	Power ground. Ground for MOSFET switches.
54	PH0	PHASE	PHASE 0 signal test pin.
56	PH1	PHASE	PHASE 1 signal test pin.
94	PWM1	PWM	Phase 1 PWM signal test pin.
97	VSENP	Analog Input	Differential output voltage sense input (positive).
98	VSENN	Analog Input	Differential output voltage sense input (negative).
99	VTRACK	Analog Input	Voltage tracking reference input VTRACK, which is not enabled in the default configuration and may remain floating if not used (default configuration). If voltage tracking mode is used (or enabled), please refer to Functional Description Section.
100	ADDR0	Analog I/O	A resistor from ADDR0 to PGND can be used to set the PMBus™ address. Use a 1% tolerance or better resistor.
101	ADDR1	Analog I/O	A resistor from ADDR1 to PGND can be used to set the PMBus™ address. Use a 1% tolerance or better resistor.
102	RVSET	Analog I/O	A resistor from RVSET to PGND can be used to program the V_{OUT} set-point. Using 1% tolerance or better resistor.
103	RTUNE	Analog I/O	A resistor from RTUNE to PGND can be used to tune the transient compensator for output capacitance. Using 1% tolerance or better resistor.
104	SYNC	Digital I/O	SYNC is not enabled in the default configuration. May remain floating if not used (default configuration). If SYNC is used (or enabled), please refer to Functional Description Section.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Voltage measurements are referenced to PGND.

Absolute Maximum Pin Ratings

Table 3

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply voltage PVIN	PVIN	-0.3	18	V
Supply voltage VCC	VCC	-0.3	5.5	V
VCC ramp time	VCC		20	ms
VDD33	VDD33	-0.3	3.6	V
Power ground	PGND	-0.3	0.3	V
Phase pins	PH0, PH1 (DC)	-0.3	25.0	V
	PH0, PH1 (AC<20ns)	-7.0	30.0	V
Digital I/O pins	SALRT, POK, SYNC	-0.3	5.5	V
Digital I/O pins	SCL, SDA, CTRL	-0.3	3.6	V
Analog I/O pins	ADDR0, ADDR1, RVSET, RTUNE, VTRACK	-0.3	2.0	V
Voltage feedback, positive	VSENP	-0.3	2.0	V
Voltage feedback, negative	VSENN	-0.3	0.3	V
PWM pin	PWM	-0.3	5.5	V
Output voltage pins	VOUT	-0.3	2.0	V
DC current on VOUT	VOUT		65	A

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Operating junction temperature			+125	°C
Storage temperature range		-65	+150	°C
Reflow peak body temperature	(10 Sec) MSL3		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBD	All pins;	1000		V
CDM; all pins		500		V

Recommended Operating Conditions

Table 4

PARAMETER	PINS	MIN	MAX	UNITS
PVIN supply voltage range	PVIN	4.5	16	V
Supply voltage V_{CC}	VCC	4.75	5.25	V
Continuous load current	V_{OUT}		60	A

Thermal Characteristics

Table 5

PARAMETER	PINS	TYPICAL	UNITS
Thermal shutdown [programmable]	T_{SD}	120	°C
Thermal shutdown Hysteresis	T_{SDH}	18	°C
Thermal resistance: junction to ambient (0 LFM) *(Note 1)*	θ_{JA}	7.25	°C/W
Thermal resistance: junction to case bottom (0 LFM)	θ_{JC}	1.35	°C/W

Note 1: Based on 2 oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51 standards for high thermal conductivity boards. No top side cooling required.

Electrical Characteristics

PV_{IN} = 12V and V_{CC} = 5.0V. The minimum and maximum values are over the ambient temperature range (-40°C to 85°C) unless otherwise noted. Typical values are at T_A = 25°C.

Table 6

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
		SUPPLY CHARACTERISTICS				
PVIN supply voltage range	PVIN		4.5		16	V
PVIN supply quiescent current		Device switching; no load; f_{sw} = 800 kHz; V_{IN} = 12.0V, V_{OUT} = 1.0V		125		mA
		Device not switching		1		
VCC supply voltage range	VCC		4.75	5.0	5.25	V
VCC POR rising				2.85		V
VCC POR falling				2.75		V
VCC UVLO rising				4.4		V
VCC UVLO falling				4.2		V
VCC supply current		Normal operation; no load; f_{sw} = 800 kHz		120 (Note 1)		mA
		Idle; communication and telemetry only; no switching		34		mA
		Disabled (V_{CC} ≤ 2.8V)		1.25		mA
		INTERNALLY GENERATED SUPPLY VOLTAGE				
VDD33 voltage range	VDD33		3.0	3.3	3.6	V
VDD33 output current					2	mA
		DIGITAL I/O PIN (SYNC)				
Input high voltage			2.0		5.5	V
Input low voltage			0		0.8	V
Output high voltage			2.4		VDD33	V
Output low voltage					0.4	V
Input leakage current					±1	µA
Output current - source					2.0	mA
Output current - sink					2.0	mA
		Open Drain PIN (POK)				
Low voltage			0		0.8	V
Input leakage current					±1	µA
Output current - sink					2.0	mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O PIN (CTRL)						
Input high voltage			2.0		3.6	V
Input low voltage			-0.3		0.8	V
CTRL response delay (stop)		Configurable polarity; extra turn-off delay configurable (assumes 0s turn-off delay)		120		µs
CTRL response delay (start)		Configurable polarity; extra turn-on delay configurable (assumes 0s turn-on delay)		160		µs
ANALOG INPUT PINS (RVSET, RTUNE, ADDR0 AND ADDR1)						
Input voltage			0		1.44	V
PWM AND SYNCHRONIZATION						
PWM output voltage - high			2.4			V
PWM output voltage - low					0.4	V
PWM tristate leakage					±1	µA
PWM pulse width		Minimum value allowed to be issued by controller	42			ns
Resolution				163		ps
Switching frequency – EM2260	f_{SW}	With internal oscillator		800		kHz
SYNC frequency range		Percent of nominal switching frequency			±12.5	%
SYNC pulse width			25			ns
OUTPUT VOLTAGE SENSE, REPORTING, AND MANAGEMENT						
Output voltage adjustment range			0.5		1.3	V
Output voltage set-point accuracy		0˚C < T_A < 85˚C	+0.5		+0.5	%
		-40˚C < T_A < 85˚C	-1		+1	%
Output set-point resolution				1.5		mV
Line regulation		IOUT = 15A (PVIN 4.5V-16V)		0.01		mV/V
Load regulation		IOUT = 0A – 60A		0.08		mV/A
Output voltage startup delay		From V_{CC} valid, to start of output voltage ramp, if configured to regulate from power on reset, and TON_DELAY is set to 0.		5		ms
Output voltage ramp delay (TON_DELAY & TOFF_DELAY)		Configurable, no V_{OUT} pre-bias condition.	0		500	ms

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VTRACK ramp rate					2.0	V/ms
VTRACK range			0		1.4	V
VTRACK offset voltage				±100		mV
OUTPUT CURRENT SENSE, REPORTING, AND MANAGEMENT						
Current sense reporting accuracy		I_{OUT} > 5A, 25°C ≤ T_A < 85°C		±3		A
		I_{OUT} > 5A, T_A = 25°C		±2		A
TEMPERATURE SENSE, REPORTING, AND MANAGEMENT						
Temperature reporting accuracy				5		°C
Resolution				0.22		°C
FAULT MANAGEMENT PROTECTION FEATURES						
PV_{IN} UVLO rising				4.4		V
PV_{IN} UVLO falling				4.2		V
PV_{IN} UV Fault threshold				3.96		V
PV_{IN} OV Fault threshold				16.5		V
V_{OUT} OV Fault threshold		Percentage of output voltage		120		%
V_{OUT} UV Fault threshold		Percentage of output voltage		85		%
I_{OUT} Fault OCP				94		A
OTP Fault threshold		Controller		120		°C
OTP Fault threshold		Power Trains		125		°C
OTP Fault hysteresis		Fixed. (Controller & Power Trains)		85		%
POK threshold		On level		95		%
POK threshold		Off level		90		%
Watchdog Timer Interval					3	ms
SERIAL COMMUNICATION PMBUS DC CHARACTERISTICS						
Input voltage – high (VIH)		SCL and SDA	1.11			V
Input voltage – low (VIL)		SCL and SDA			0.8	V
Rise & Fall Time		SCL and SDA >0.8V<1.1V			2	ms
Input leakage current		SCL, SDA and CTRL.	-10		10	µA
leakage current		SALRT		65		µA
Output voltage – low (VOL)		SDA and SALRT at rated pull-up current of 20mA.			0.4	V
Nominal bus voltage		SCL and SDA termination voltage.			3.6	V

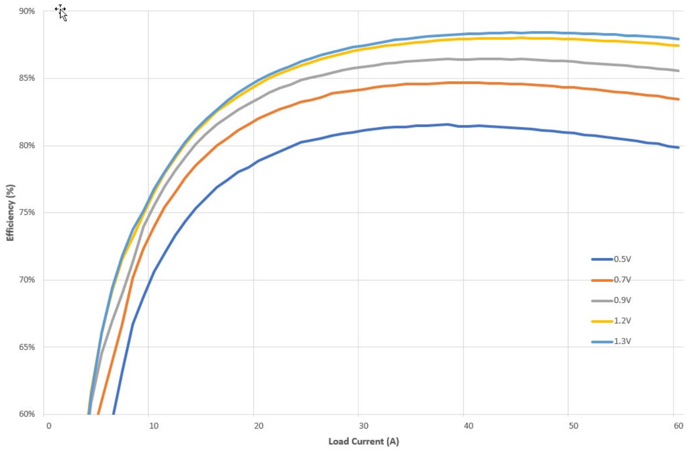
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Nominal SLART voltage		SALRT termination voltage.		3.3	3.6	V

Note 1: For 5V regulator design, allocate 200mA for EM2260

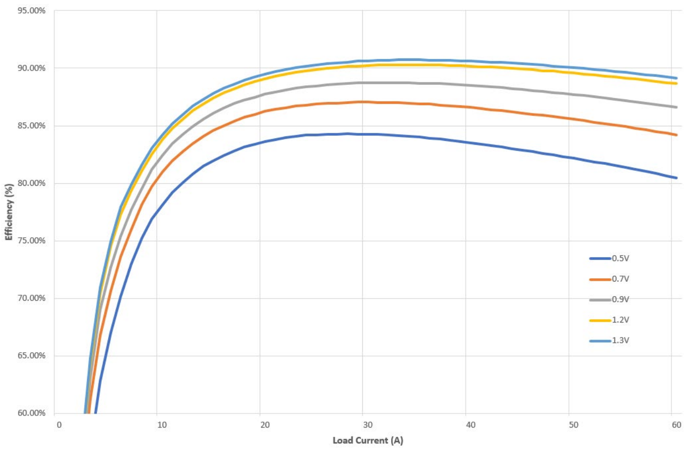
Typical Performance Characteristics

All the performance curves are measured with EM2260 evaluation board at 25°C ambient temperature unless otherwise noted. The output capacitors configuration for the evaluation board is 8 x 470 µF (3 mΩ ESR) + 8 x 100 µF (Ceramic)

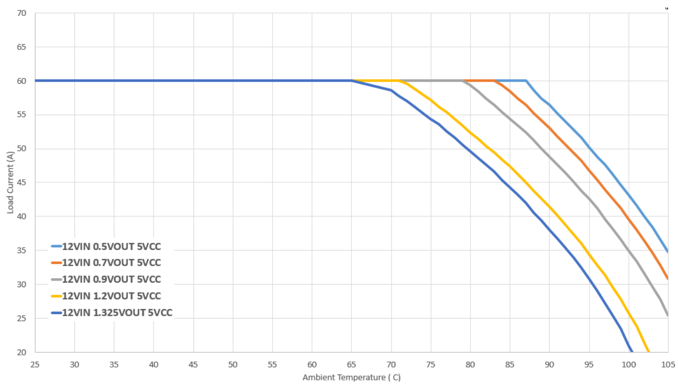
Efficiency, V_{IN} = 12V



Efficiency, V_{IN} = 5V

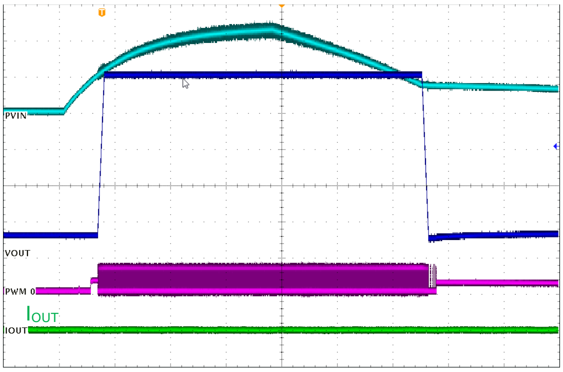


EM2260 Thermal Derating, No Airflow



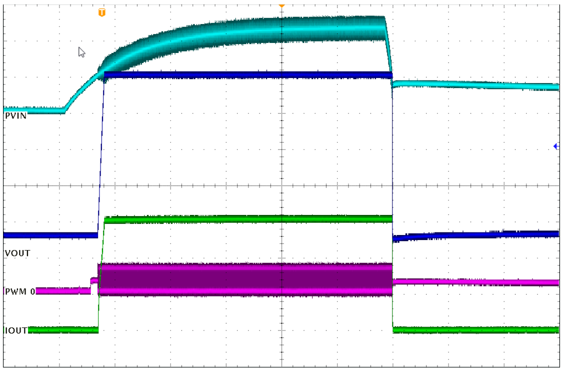
Typical Performance Characteristics (Continued)

Start-up/Shutdown, PVIN at No Load, 20ms/div



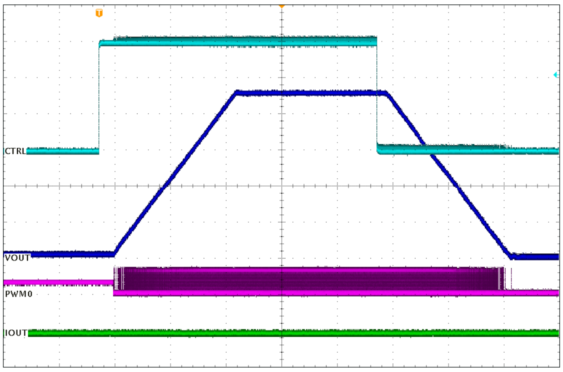
PV_{IN} and PWM: 5 V/div,
V_{OUT}: 200 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, PVIN at 60A Load, 20ms/div



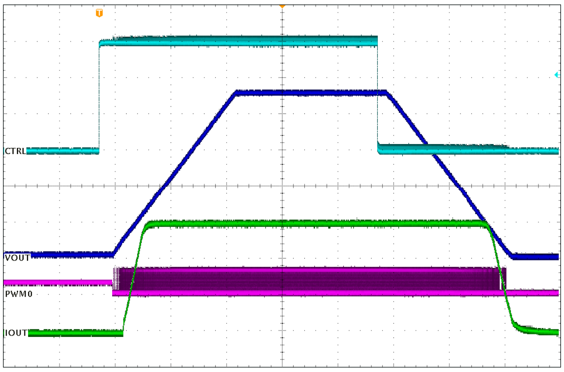
PV_{IN} and PWM: 5 V/div,
V_{OUT}: 200 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, CTRL at No Load, 800µs/div



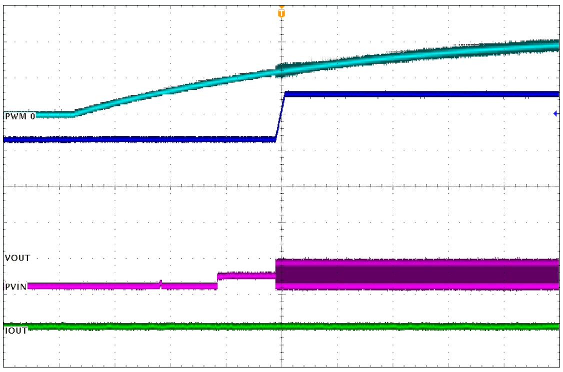
CTRL: 1 V/div, PWM: 5 V/div,
V_{OUT}: 200 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, CTRL At 60A Load, 800µs/div



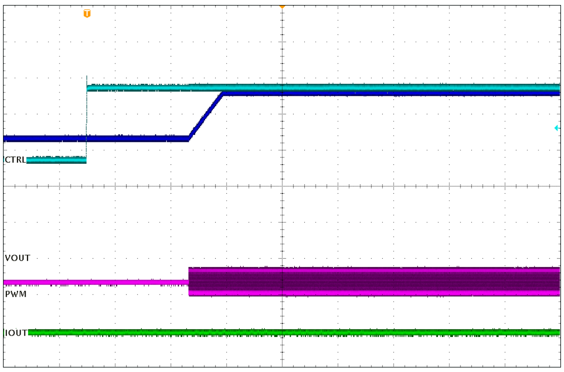
CTRL: 1 V/div, PWM: 5 V/div,
V_{OUT}: 200 mV/div, I_{OUT}: 20 A/div

Start-up into 0.6V Pre-Bias With PVIN, 4ms/div



PV_{IN}: 5 V/div, PWM: 5 V/div,
V_{OUT}: 200 mV/div, I_{OUT}: 20 A/div

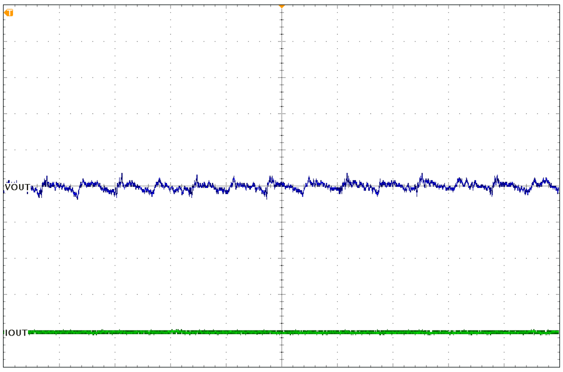
Start-up into 0.7V Pre-Bias With CTRL, 800µs/div



CTRL: 1 V/div, PWM: 5 V/div,
V_{OUT}: 200 mV/div, I_{OUT}: 20 A/div

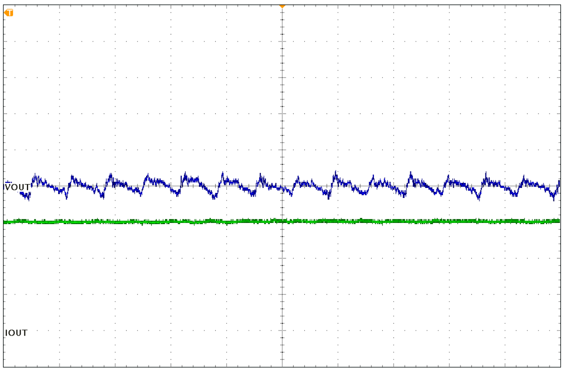
Typical Performance Characteristics (Continued)

Output Voltage Ripple, No Load



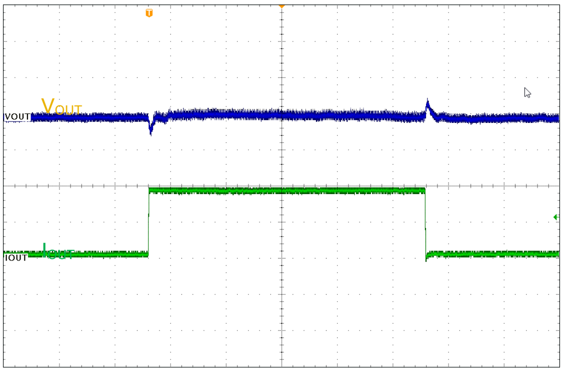
V_{IN} = 12V, V_{OUT} = 0.9V
1 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Ripple, 60A Load



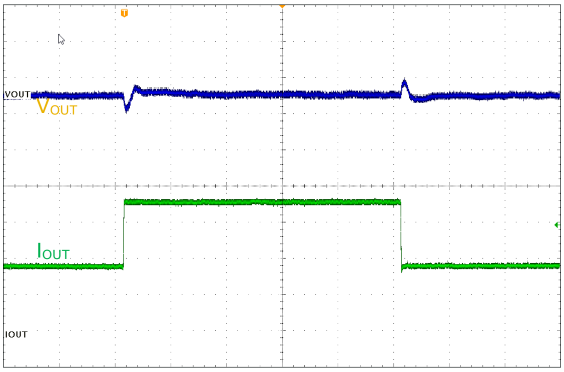
V_{IN} = 12V, V_{OUT} = 0.9V
1 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Transient Response, Load Step From 0A to 30A



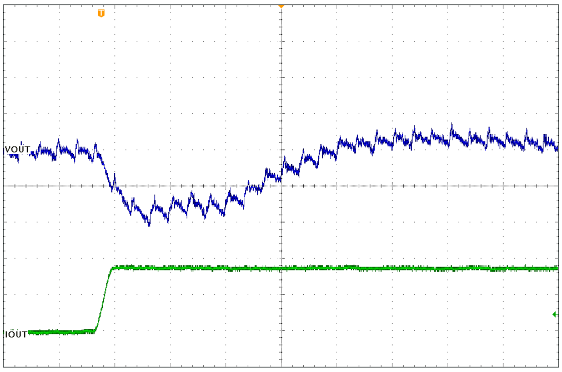
V_{IN} = 12V, V_{OUT} = 0.9V, 40µs/div
V_{OUT}: 50 mV/div, I_{OUT}: 16.67 A/div, 50 A/µs

Output Voltage Transient Response, Load Step From 30A to 60A



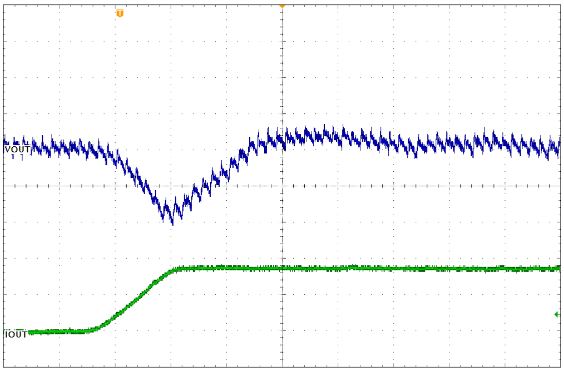
V_{IN} = 12V, V_{OUT} = 0.9V, 40µs/div
V_{OUT}: 50 mV/div, I_{OUT}: 16.67 A/div, 50 A/µs

Output Voltage Transient Response, Load Step From 0A to 30A



V_{IN} = 12V, V_{OUT} = 0.9V, 2µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 16.67 A/div, 50 A/µs

Output Voltage Transient Response, Load Step From 0A to 30A



V_{IN} = 12V, V_{OUT} = 0.9V, 2µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 16.67 A/div, 5 A/µs

Functional Block Diagram

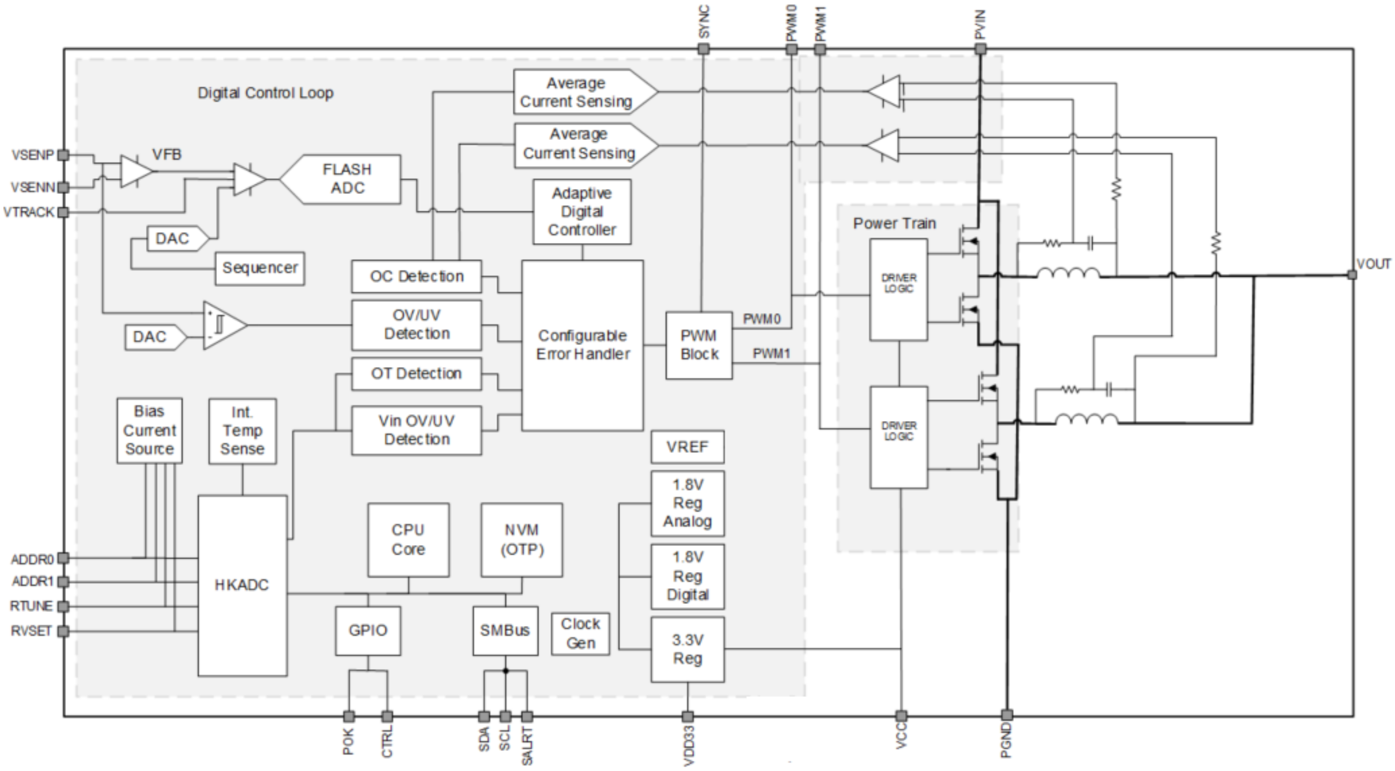


Figure 3: Functional Block Diagram

Functional Description

FUNCTIONAL DESCRIPTION: DEFAULT CONFIGURATION

The EM2260 is a two-phase, single output digital PowerSoC synchronous step-down converter with advanced digital control techniques, capable of supplying up to 60A of continuous output current. The PowerSoC includes integrated power MOSFETs, high-performance inductors and a digital controller which offers a PMBus version 1.2 compliant interface to support an extensive suite of telemetry, configuration and control commands.

In the default configuration, the EM2260 requires only two resistors total to set the output voltage and set the digital compensator for the most optimized performance. This easy-to-use default configuration allows the user to tune the EM2260 to meet the most demanding accuracy and load transient requirements without requiring any programming or digital interface. The following sections describe the default configuration. Refer to the Advanced Configuration section for details on the many ways the EM2260 may be customized and configured through the PMBus interface.

The advanced digital control loop works as a voltage-mode controller using a PID-type compensation. The basic structure of the controller is shown in Figure 4. The EM2260 controller features two PID compensators for steady-state operation and fast transient operation. Fast, reliable switching between the different compensation modes ensures good transient performance and quiet steady state performance. The EM2260 has been pre-programmed with a range of default compensation coefficients which lets the user select the best compensation for the best transient response and stability for the output capacitance of the system.

The EM2260 uses two additional technologies to improve transient performance. First, the EM2260 uses over-sampling techniques to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any changes in output voltage. Second, a non-linear gain adjustment is applied during large load transients to boost the loop gain and reduce the settling time.

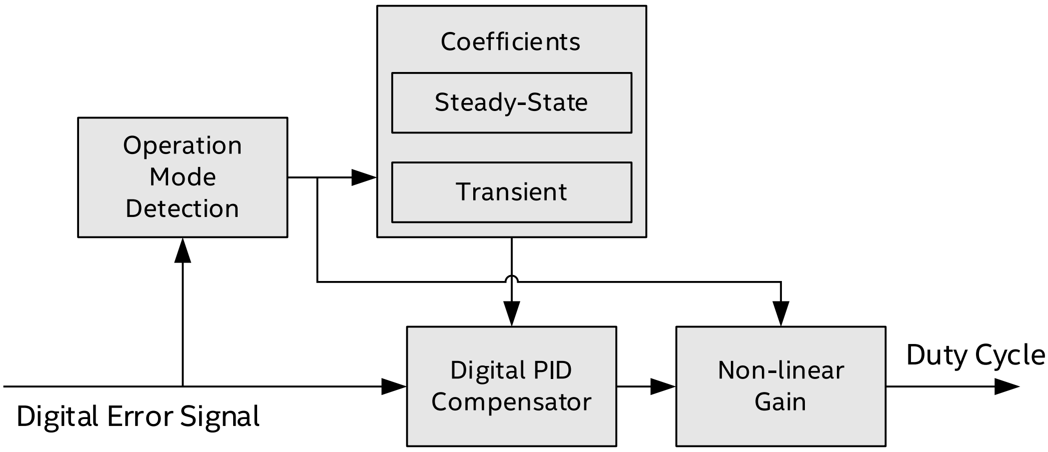


Figure 4: Simplified Block Diagram of The Digital Compensation

In the default configuration, the EM2260 offers a complete suite of fault warnings and protections. Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored. A dedicated ADC is used to provide fast and accurate current information over the switching period allowing for fast Over-Current Protection (OCP) response. Over Temperature Protection (OTP) is accomplished by direct monitoring of the internal controller's temperature and the temperature of both Power Trains.

POWER ON RESET

The EM2260 employs an internal power-on-reset (POR) circuit to ensure proper start-up and shut down with a changing supply voltage. Once the VCC supply voltage increases above the POR threshold voltage, the EM2260 begins the internal start-up process. Upon its completion, the device is ready for operation.

Two separate input voltage supplies are necessary to operate, PVIN (4.5V to 16V) and V_{CC} (4.75V to 5.25V). Both voltage rails are internally monitored for proper power-up and to protect the power MOSFETs under various input power fault conditions.

The EM2260 also monitors PVIN for input voltage feed-forward, which eliminates variations in the output voltage due to sudden changes in the input voltage supply. It does this by immediately changing the duty cycle to compensate for the input supply variation by normalizing the DC gain of the loop.

SETTING THE OUTPUT VOLTAGE

Differential remote sensing provides for precise regulation at the point of load. One of thirty output voltages may be selected in the default configuration, based on a resistor connected to the RVSET pin. At power-up, an internal current source biases the resistor and the voltage is measured by an ADC to decode the Vout selection. Use Table 7 for the details of V_{OUT} selection and RVSET values.

The digital control loop ADC of the EM2260 supports direct output voltage feedback connection over the entire V_{OUT} range.

Note: at output voltage <0.7V, high PVin values >10V and very light loads <3A pulse skipping may occur on the PWM which may results in a slight increase in output ripple. This is the due to the very narrow PWM outputs resulting from these conditions and the minimum pulse width accepted by the Power Trian to ensure no cross conduction between the Top and Bottom MOSFET's.

Table 7: Supported Configuration Voltage Values for EM2260P01 Output Voltage

RVSET Resistor (Using 1% tolerance or better resistor)	V_{OUT}
0kΩ	Reserved
0.392kΩ	Reserved
0.576kΩ	1.3V
0.787kΩ	1.25V
1.000kΩ	1.2V
1.240kΩ	1.175V
1.500kΩ	1.15V
1.780kΩ	1.12V
2.100kΩ	1.1V
2.430kΩ	1.05V
2.800kΩ	1.03V
3.240kΩ	1.0V
3.740kΩ	0.975V
4.220kΩ	0.95V
4.750kΩ	0.92V
5.360kΩ	0.9V
6.040kΩ	0.89
6.810kΩ	0.875V
7.680kΩ	0.85V
8.660kΩ	0.825V
9.530kΩ	0.8V
10.500kΩ	0.775V
11.800kΩ	0.75V
13.000kΩ	0.72V
14.300kΩ	0.7V
15.800kΩ	0.65V
17.400kΩ	0.6V
19.100kΩ	0.55V
21.000kΩ	0.52V
23.200kΩ	0.5V

ENABLE AND OUTPUT START-UP BEHAVIOR

The control pin (CTRL) provides a means to enable normal operation or to shut down the device. When the CTRL pin is asserted (high) the device will undergo a normal soft-start. A logic low on this pin will power the device down in a controlled manner. Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this period.

The typical power sequencing, including ramp up/down and delays is shown in **Figure 5**.

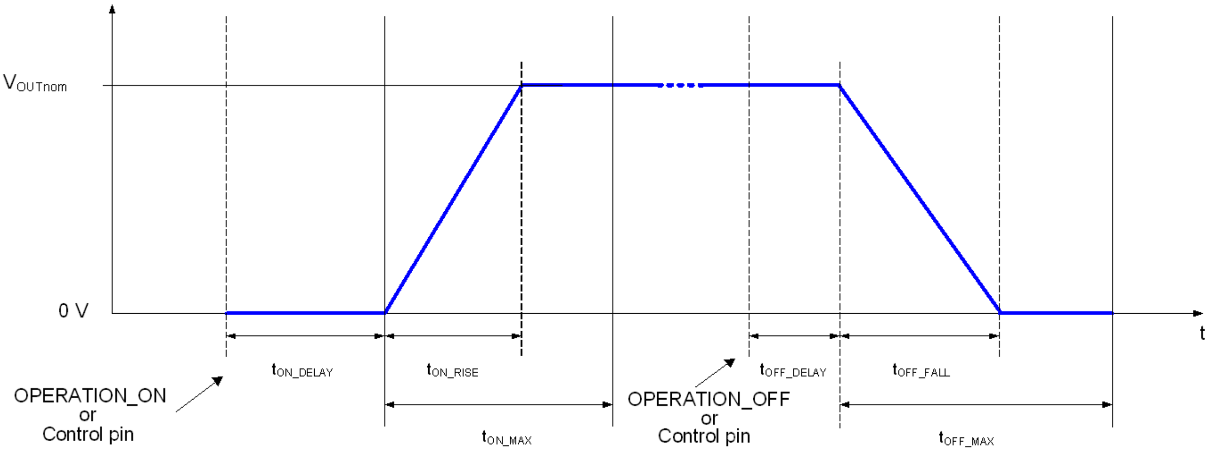


Figure 5: Power Sequencing

POWER OK

The EM2260 has a Power OK indicator at its output pin POK, which is Open Drain and therefore requires a pull-up resistor. The Pull-Up resistor may be connected to the VDD33 pin but it is not recommended to use the 5VCC supply. When de-asserted, POK indicates that the output voltage is below the threshold value, 90% of the programmed output voltage in the default configuration. When asserted, POK indicates that the output is in regulation, and no major faults are present. As a result, POK de-asserts during any serious fault condition where power conversion stops and re-asserts when the output voltage recovers.

In a noisy application, it is strongly recommended that a 100nf decoupling capacitor be placed between the POK pin and GND to act as a filter to unwanted external noise.

SMBAlert Pin

The SMBAlert pin is intended to operate using an external pull-up voltage of 3.3V and contains a weak internal pull-up.

If operating in applications with a lower voltage pull-up voltage, it is recommended that an external low Vf Schottky diode be placed at the input to localise this voltage.

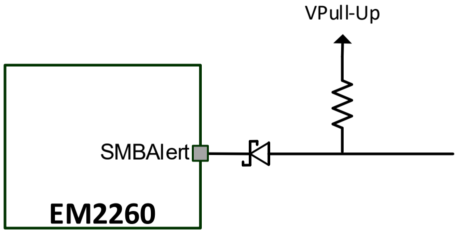


Figure 6: SMBAlert Pin Low Voltage Pull-up Option

Table 8: Schottky Diode Options

Description	Manufacturer	P/N
40V, 300mA, Schottky, SOD523	ST	BAT54KFILM
40V, 250mA, Schottky, SOD523	Diode Inc	BAT64T5Q

COMPENSATING THE DIGITAL CONTROL LOOP

To improve the transient performance for a typical point-of-load design, it is common to add output capacitance to the converter. This moves the output LC resonant frequency lower as capacitance increases which results in lower bandwidth, lower phase margin, and longer settling times unless the control loop is compensated for added capacitance.

However, with EM2260 the user does not need to be concerned with, or even understand, the details of control loop compensation techniques. The default configuration allows users to select from preconfigured PID control loop settings (known as compensators) using pin-strapping. A single resistor from the RTUNE pin to GND informs the EM2260 of the compensator selection.

The selection of the compensator is driven first by the type of output capacitors used, as the ESL and ESR of different capacitor types demands different PID coefficients to optimize transient deviation and recovery characteristics. The default compensator is a design with a combination of ceramic and polymer capacitors, i.e. SP-CAP. **Table 9** shows typical output capacitor part number recommendations.

The five different compensators can then be subdivided into groups of six each whereby the initial capacitance value in the appropriate compensator can be scaled upwards by multiplication factor M to match the additional capacitance.

Table 9: RTUNE configuration table for EM2260P01

Compensator Description	C_{OUT}	RTUNE Resistor (Using 1% tolerance or better resistor)	Multiplication factor (M)	Typical Deviation with 50% Load Step
Polymer Aluminum (SP-CAP) and Ceramic MLCC Output Capacitors Base capacitance = 4 x 470µF (Polymer) + 4 x 100µF (Ceramic)	Base	0kΩ	1	± 5%
	2 x Base	0.392kΩ	2	± 3%
	2.5 x Base	0.576kΩ	2.5	
	3 x Base	0.787kΩ	3	
	3.5 x Base	1.000kΩ	3.5	
	4 x Base	1.240kΩ	4	± 1.5%
Reserved for User Programmed Compensation Values		1.500kΩ		
		1.780kΩ		
		2.100kΩ		
		2.430kΩ		
		2.800kΩ		
		3.240kΩ		
		3.740kΩ		
		4.220kΩ		
		4.750kΩ		
		5.360kΩ		
		6.040kΩ		
		6.810kΩ		
		7.680kΩ		
		8.660kΩ		
		9.530kΩ		
		10.500kΩ		
		11.800kΩ		
		13.000kΩ		
		14.300kΩ		
		15.800kΩ		
		17.400kΩ		
		19.100kΩ		
		21.000kΩ		
		23.200kΩ		

Table 10: Recommended Output Capacitors

Description	Manufacturer	P/N
470µF, 2.5V, ESR 3mΩ SP-CAP	Panasonic	EEFGX0E471R
100µF, 6.3V, X5R, 1206 Ceramic	Kemet	C1206C107M9PACTU

OUTPUT CAPACITOR RECOMMENDATION

EM2260 is designed for fast transient response and low output ripple noise. The output capacitors should be a mix of low ESR polymer and ceramic capacitors. **Table 8** shows different output capacitor combinations to optimize the load transient deviation performance. With the RTUNE feature, the user can simply scale up the total output capacitance to meet further stringent transient requirement.

Please consult the documentation for your particular FPGA, ASIC, processor, or memory block for the transient and the bulk decoupling capacitor requirements.

INPUT CAPACITOR RECOMMENDATION

The EM2260 PVIN input should be decoupled with at least four 22µF 1206 case size ceramic capacitors. More bulk capacitor may be needed if there are long inductive traces at the input source, there is not enough source capacitance or at low PVIN values.

These input decoupling ceramic capacitors may be mounted on the PCB back-side to reduce the solution size. These input filter capacitors should have the appropriate voltage rating for the input voltage on PVIN, and use a X5R, X7R, or equivalent dielectric rating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

PROTECTION FEATURES

The EM2260 offers a complete suite of programmable fault warnings and protections. Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored. A dedicated ADC is used to provide fast and accurate current information during the entire switching period to provide fast Over-Current Protection (OCP) response.

To prevent damage to the load, the EM2260 utilizes an output over-voltage protection circuit. The voltage at VSENP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, a fault response is generated and the PWM output is turned off.

The output voltage is also sampled, filtered, and compared with an output over-voltage warning threshold. If the output voltage exceeds this threshold, a warning is generated and the preconfigured actions are triggered. The EM2260 also monitors the output voltage with two lower thresholds. If the output voltage is below the under-voltage warning level and above the under-voltage fault level, an output voltage under-voltage warning is triggered. If the output voltage falls below the fault level, a fault event is generated.

Similar to output over and under voltage protection, the EM2260 monitors the input voltage PVIN continuously with a configurable threshold. If the input voltage exceeds the over voltage threshold or is below the under-voltage threshold, the default response is generated.

Over Temperature Protection (OTP) is based on direct monitoring of the device's internal controller temperature and the internal Power Train temperature. If the temperature exceeds either OTP thresholds, the device will enter a soft-stop mode slowly ramping the output voltage down until the temperature falls below the default recovery temperature.

The default fault response is zero delay and latch off for most fault conditions. The CTRL pin may be cycled to clear the latch. Table 10 summarizes the default configurations that have been pre-programmed to the device.

Table 11: Fault Configuration Overview

Signal	Fault Level	Default Response Type	Delay (ms)	Retries
Output Over-Voltage	Warning		0	None
	Fault	High-impedance		
Output Under-Voltage	Warning		0	None
	Fault	High-impedance		
Input Over-Voltage	Warning		0	None
	Fault	High-impedance		
Input Under-Voltage	Warning		0	Infinity
	Fault	High-impedance		
Over-Current	Warning		0	None
	Fault	High-impedance		
Controller Over-Temperature	Warning		0	Infinity
	Fault	Soft Off		
Power Train Over-Temperature	Warning		0	Infinity
	Fault	Soft Off		

FUNCTIONAL DESCRIPTION: ADVANCED CONFIGURATION

All EM2260 modules are delivered with a pre-programmed default configuration, allowing the module to be powered up without a need to configure the device or even the need for the GUI to be connected. However, a PMBus version 1.2 compliant interface allows access to an extensive suite of digital communication and control commands. This includes configuring the EM2260 for optimum performance, setting various parameters such as output voltage, and monitoring and reporting device behavior including output voltage, output current, and fault responses.

The device may be reconfigured multiple times without storing the configuration into the non-volatile memory (NVM). Any configuration changes will be lost upon power-on reset unless specifically stored into NVM using either STORE_DEFAULT_ALL or STORE_DEFAULT_CODE PMBus commands. Please see Table **13** for more details.

For RVSET and RTUNE configurations, there is no reprogramming permitted.

After writing a new configuration to NVM, the user may still make changes to the device configuration through the PMBus interface; however, now upon power cycling the device, the stored NVM configuration will be recalled upon power-up rather than the factory default configuration of the EM2260.

The NVM configuration can be stored three times in its entirety. However, the consumption of the available NVM is dynamic, based on the configuration parameters that have changed. The unused NVM information is given in the GUI or through the manufacture specific command MFR_STORE_PARAMS_REMAINING.

INTEL DIGITAL POWER CONFIGURATOR

The Intel Enpirion Digital Power Configurator is a Graphical User Interface (GUI) software which allows the EM2260 to be controlled via a USB interface to a host computer.

The user can view the power supply's status, I/O voltages, output current and fault conditions detected by the device, program settings to the converter, and issue PMBus commands using the GUI. Most of the parameters (for example, VOUT turn on/off time, protection and fault limits) can be configured and adjusted within the GUI environment. These parameters can also be configured outside of the GUI environment using the relevant PMBus™ commands.

The GUI also allows the user to easily create, modify, test and save a configuration file which may then be used to permanently burn the configuration into NVM within a production test environment.

ALTERNATIVE OUTPUT VOLTAGE CONTROL METHODS

In the default configuration, output voltage selection is determined at power-up by the pin-strapped resistor RVSET. This functionality can be disabled using the PMBus command MFR_PIN_CONFIG. When RVSET is disabled, the output voltage will be determined by the nominal output voltage setting in the user configuration. The EM2260 supports a subset of the output voltage commands outlined in the PMBus specification. For example, the output voltage can be dynamically changed using the PMBus command VOUT_COMMAND. When the output is being changed by the PMBus command, POK remains at a logic high.

POWER SEQUENCING AND THE CONTROL (CTRL) PIN

Three different configuration options are supported to enable the output voltage. The device can be configured to turn on after an OPERATION_ON command, via the assertion of the CTRL pin or a combination of both per the PMBus convention. The EM2260 supports power sequencing features including programmable ramp up/down and delays. The typical sequence of events is shown in Figure 5 and follows the PMBus standard. The individual timing values shown in Figure 5 and Figure 6 can be configured using the appropriate configuration setting in Intel Digital Power Configurator GUI.

PRE-BIASED START-UP AND SOFT-STOP

In systems with complex power architectures, there may be leakage paths from one supply domain which may charge capacitors in another supply domain, leading to a pre-biased condition on one or more power supplies. This condition is not ideal and can be avoided through careful design, but is generally not harmful. Attempting to discharge the pre-bias is not advised as it may force high current though the leakage path. The EM2260 includes features to enable and disable into pre-biased output capacitors.

If the output capacitors are pre-biased when the EM2260 is enabled, start-up logic in the EM2260 ensures that the output does not pull down the pre-biased voltage and the t_{ON_RISE} timing is preserved. Closed-loop stability is ensured during the entire start-up sequence under all pre-bias conditions.

The EM2260 also supports pre-biased off, in which the output voltage ramp down to a user-defined level (PMBus command : V_{OFF_nom}) rather than to zero. After receiving the disable command, via PMBus command or the CTRL pin, the EM2260 ramps down the output voltage to the predefined value. Once the value is reached, the output driver goes into a tristate mode to avoid excessive currents through the leakage path.

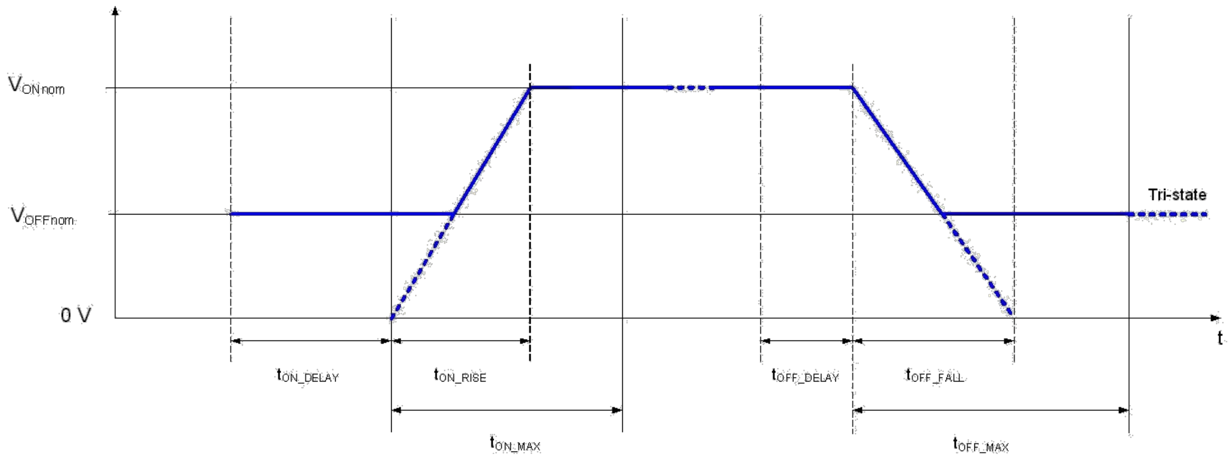


Figure 7: Power Sequencing with Non-Zero Off Voltage

VOLTAGE TRACKING

The EM2260 can control the output voltage based on the external voltage applied to the VTRACK pin, thus allowing sequencing of the output voltage from an external source. Pre-bias situations are also supported. The VTRACK pin voltage is a single-ended input referenced to analog ground. Tracking mode is disabled by default, but it can be enabled using the GUI software or via the manufacturer-specific PMBus command, MFR_FEATURES_CTRL (see **Table 13**).

If VTRACK is not intended to be used, tie the VTRACK pin low or leave it floating.

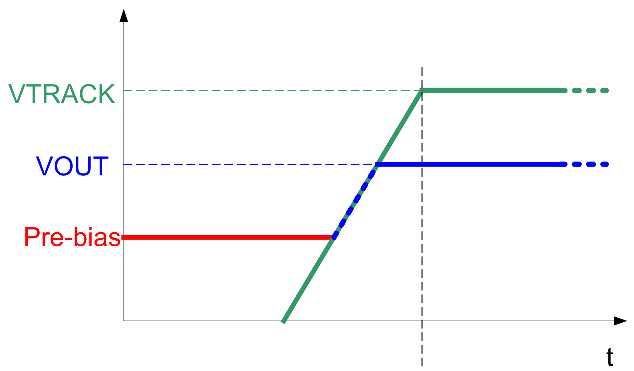


Figure 8: **Power Sequencing Using VTRACK With Bias Voltage On VOUT**

The set point voltage for the EM2260 is defined by the lower value of the V_{OUT} setting or an external voltage applied to the VTRACK pin. If the VTRACK voltage rises above the V_{OUT} set point voltage, then the final output voltage will be limited by the V_{OUT} setting. If the tracking feature is enabled, but the VTRACK pin is tied low or floating, then the output will never start as the VTRACK pin input is always the lower value and will always be in control. Conversely, if tracking is enabled, but VTRACK is tied high, the output will start but will follow the V_{OUT} set point, not the VTRACK pin.

If tracking is used for sequencing, it is recommended that the VTRACK signal be kept greater than the V_{OUT} voltage. This ensures that the internal V_{OUT} set point is used as the final steady-state output voltage and accuracy is not a function of the externally applied VTRACK voltage. The tracking function will override a programmed pre-bias off level (V_{OFF_nom}).

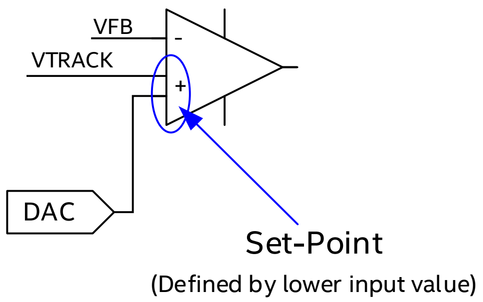


Figure 9: VTRACK Circuitry

The following figures demonstrate ratio-metric and simultaneous sequencing of the output voltage, which can be accomplished by applying an appropriate external voltage on the VTRACK pin. When using the VTRACK feature, the sequencing will be ratio-metric as shown in Figure 9, if an external resistor network is used at the VTRACK pin as shown in Figure 11. If no external resistors are used, the output sequence is simultaneous as shown in Figure 10.

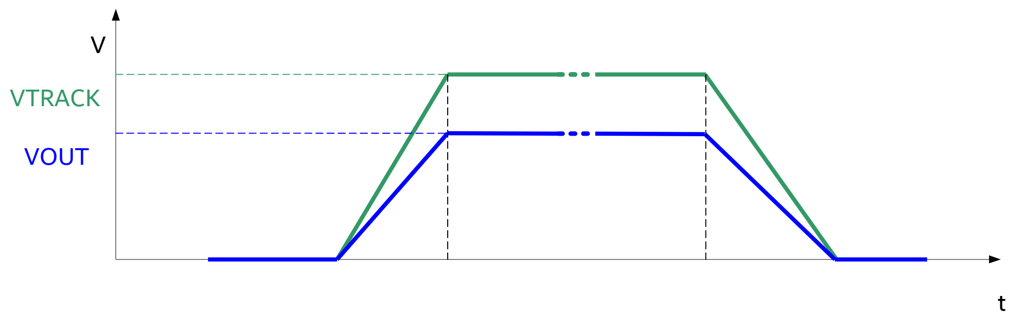


Figure 10: Ratiometric Sequencing Using VTRACK

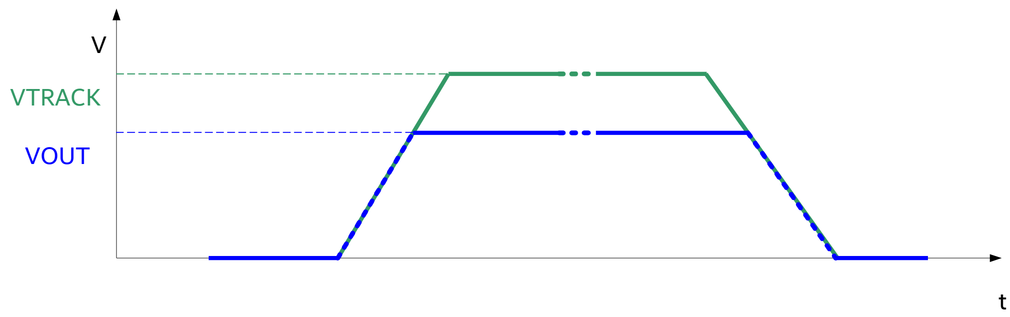


Figure 11: Simultaneous Sequencing Using VTRACK

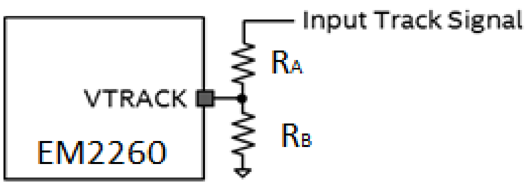


Figure 12: VTRACK Sense Circuitry with Resistor Divider

In the event that the tracking voltage applied to VTRACK is greater than 1.4V, then a 2kΩ resistor is required in series with the VTRACK pin to minimize leakage current as shown in Figure 12.

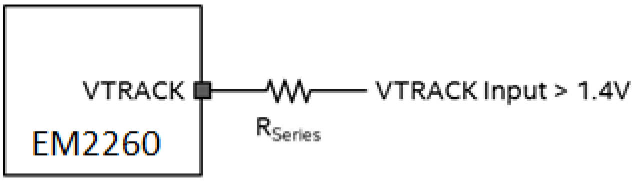


Figure 13: VTRACK Sense Circuitry (Input > 1.4V)

CLOCK SYNCHRONIZATION

The EM2260's PWM synchronization feature allows the user to synchronize the switching frequency of multiple devices. The SYNC pin can be configured as an input or an output.

The EM2260 SYNC functionality maybe configured as an input or an output using Intel's GUI software or via the manufacturer-specific PMBus command, MFR_PIN_CONFIG. The default configuration for synchronization control is OFF.

TEMPERATURE AND OUTPUT CURRENT MEASUREMENT

The EM2260 temperature sense block provides the device and the system with precision temperature information over a wide range of temperatures (-40°C to +150°C). The temperature sense block measures both the digital controller's temperature and a combination of both Power Train temperatures.

The EM2260 monitors output current by real-time, temperature compensated DCR current sensing across the inductor. This real-time current waveform is then digitally filtered and averaged for accurate telemetry, fault warning, and management.

Factory calibration has been performed for every EM2260 device to improve measurement accuracy over the full output current range. This allows the EM2260 to correct for DCR manufacturing variations.

For over-current protection, an unfiltered ADC is used to minimize delays in protecting the device. Because this measurement is unfiltered, the accuracy of the protection threshold is less than that of the average current reading.

PROTECTION AND FAULT RESPONSE

The EM2260 monitors various signals during operation to detect fault conditions. Measured and filtered signals are compared to a configurable set of warnings and fault thresholds. In typical usage, a warning sets a status flag, but does not trigger a response; whereas a fault sets a status flag and generates a response. The assertion of the SMBALERT signal can be configured to individual application requirements.

The EM2260 supports many different response types depending on the fault detected.

In the default configuration, the EM2260 responds to an over temperature event by ramping down V_{OUT} in a controlled manner at a slew rate defined by the T_{OFF_FALL} value. This response type is termed "Soft-Off". The final state of the output signals depends on the value selected for V_{OFFnom}.

For all other faults the EM2260 will respond by immediately turning off both the top-side MOSFET and low-side MOSFET. This response type is termed "High-Impedance".

For each fault response, a delay and a retry setting can be configured. If the delay-to-fault value is set to non-zero, the EM2260 will not respond to a fault immediately. Instead it will delay the response by the configured value and then reassesses the signal. If the fault remains present during the delay time, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded.

If the delay-to-retry value is set to non-zero, the EM2260 will not attempt to restart immediately after fault detection. Instead it will delay the restart by the configured value. If the fault is still present when attempting to restart, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded. If the delay-to-fault is a non-zero value, then the delay-to-retry value will be a factor of 100 times greater than the delay-to-fault value.

The retry setting, i.e. the number of EM2260 restarts after a fault event, can be configured. This number can be between zero and six. A setting of seven represents infinite retry operation. This setting is commonly known as “Hiccup Mode.”

Watchdog Timer

General house-keeping operations are managed by an internal microcontroller (MCU). To ensure reliable MCU operation in all environments a watchdog timer has been incorporated. The purpose of the watchdog timer is to reset the MCU as a last resort in the unlikely event of it entering an unknown state.

In the exceptional event of a reset the MCU will shut down the controller into a safe state and will then reload its memory, restarting the controller and output into its known good default operating condition.

PMBus Functionality

INTRODUCTION

The EM2260 supports the PMBus protocol (version 1.2) to enable the use of configuration, monitoring, and fault management features during run-time.

The PMBus host controller is connected to the EM2260 via the PMBus pins (SDA, SCL). A dedicated SMBALERT pin is provided to notify the host that new status information is present.

The EM2260 supports packet correction (PEC) according to the PMBus™ specification.

The EM2260 supports clock stretching according to the SMBus specification.

The EM2260 communciations utilizes clock stretching as required and this requires the PMBus master to support clock stretching.

The EM2260 supports more than 60 PMBus commands in addition to several manufacturer specific commands related to output voltage, faults, telemetry, and more.

The EM2260 supports more than 60 PMBus commands in addition to several manufacturer specific commands related to output voltage, faults, telemetry, and more.

The EM2260 provides a PMBus set of synchronous communication lines, with serial clock input (SCL), serial data I/O (SDA), and serial alarm output (SALRT) pins.

The communication lines provide 1.8V I/O compatibility and open-drain outputs (SDA, SCL and SALRT). The communication lines require external pull-up resistors; typical applications require pull-up resistors on each end of the communication lines (typically values of 10 kΩ each), connected to VDD33 or an alternative termination voltage. Please refer to the PMBus specification (www.pmbus.org) for full details.

The EM2260 provides configurable behavior for the SALRT pin to allow users to determine which fault or warning conditions to communicate over the SALRT line. The default behavior of the controller ensures that any fault or warning results in the EM2260 SALRT pin going low; the alert behavior is enabled for all faults and warnings. You can deselect any of the faults or warnings so when one of these conditions occur, the SALRT pin is not pulled low.

The EM2260 provides a PMBus compliant power conversion control signal through input CTRL. You can configure input CTRL through the standard PMBus command ON_OFF_CONFIG.

In the default configuration, the CTRL pin must be pulled high to enable operation and the PMBus command OPERATION is ignored. You can override this function with the ON_OFF_CONFIG PMBus command.

Remote measurement and reporting of telemetry information at the power supply level provides feedback on key parameters such as voltages, current levels, temperature, and energy, and allows reporting of information such as faults and warning flags. With this information, data is collected and analyzed while the power supply is in development, such as in the qualification or verification phases, or in the field, and system level interaction such as power capping is implemented. Several telemetry parameters are supported by standard PMBus commands.

The EM2260 supports PMBus output current telemetry through the READ_IOUT command and reports the low-pass filtered, or DC, output current.

The standard PMBus command READ_VOUT supports output voltage telemetry.

The standard PMBus command READ_VIN supports input voltage telemetry.

The EM2260 supports temperature telemetry and reporting through standardized PMBus commands, READ_TEMPERATURE_1 is mapped to the summation of the Power Trains die temperatures and READ_TEMPERATURE_2 is mapped to the controller die temperature.

The EM2260 supports the LINEAR data format according to the PMBus specification. Note that in accordance with the PMBus specification, all commands related to the output voltage are subject to the VOUT_MODE settings.

A detailed description of the supported PMBus commands supported by the EM2260 can be found in EM2260 *Application Note – PMBus Commands Guide.*

TIMING AND BUS SPECIFICATION

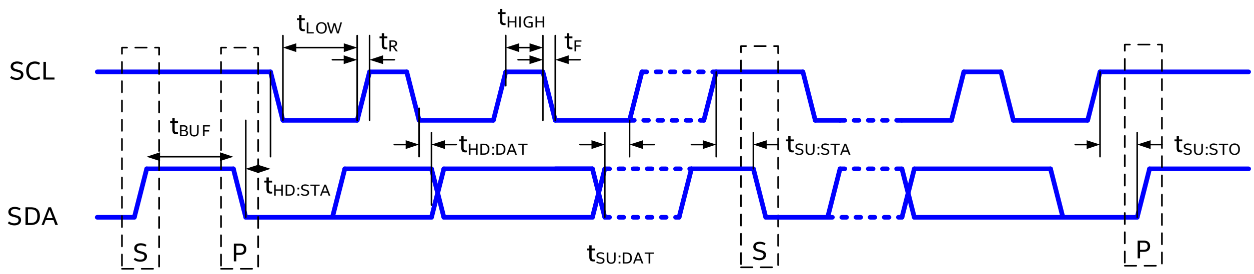


Figure 14: PMBus Timing Diagram

Table 12: EM2260 PMBus Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PMBus operation frequency	f_{SMB}		10	100	400	kHz
Bus free time between start and stop	t_{BUF}		1.3			µs
Hold time after start condition	$t_{HD:STA}$		0.6			µs
Repeat start condition setup time	$t_{SU:STA}$		0.6			µs
Stop condition setup time	$t_{SU:STO}$		0.6			µs
Data hold time	$t_{HD:DAT}$		300			ns
Data setup time	$t_{SU:DAT}$		100			ns
Clock low time-out	$t_{TIMEOUT}$			25	35	ms
Clock low period	t_{LOW}		1.3			µs
Clock high period	t_{HIGH}		0.6			µs
Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
Clock or data fall time	t_F				300	ns
Clock or data rise time	t_R				300	ns

ADDRESS SELECTION VIA EXTERNAL RESISTORS

The PMBus protocol uses a 7-bit device address to identify different devices connected to the bus. This address can be selected via external resistors connected to the ADDRx pins.

The resistor values are sensed using the internal ADC during the initialization phase and the appropriate PMBus address is selected. Note that the respective circuitry is only active during the initialization phase; hence no DC voltage can be measured at the pins. The supported PMBus addresses and the values of the respective required resistors are listed in Table 12.

Table 13: Supported Resistor Values For PMBus Address Selection

Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω
0x40	0	0	0x2B	1.2 k	12 k	0x56	3.9 k	4.7 k
0x01*	0	680	0x2C	1.2 k	15 k	0x57	3.9 k	5.6 k
0x02*	0	1.2 k	0x2D	1.2 k	18 k	0x58	3.9 k	6.8 k
0x03*	0	1.8 k	0x2E	1.2 k	22 k	0x59	3.9 k	8.2 k
0x04*	0	2.7 k	0x2F	1.2 k	27 k	0x5A	3.9 k	10 k
0x05*	0	3.9 k	0x30	1.8 k	0	0x5B	3.9 k	12 k
0x06*	0	4.7 k	0x31	1.8 k	680	0x5C	3.9 k	15 k
0x07*	0	5.6 k	0x32	1.8 k	1.2 k	0x5D	3.9 k	18 k
0x08*	0	6.8 k	0x33	1.8 k	1.8 k	0x5E	3.9 k	22 k
0x09	0	8.2 k	0x34	1.8 k	2.7 k	0x5F	3.9 k	27 k
0x0A	0	10 k	0x35	1.8 k	3.9 k	0x60	4.7 k	0
0x0B	0	12 k	0x36	1.8 k	4.7 k	0x61*	4.7 k	680
0x0C*	0	15 k	0x37*	1.8 k	5.6 k	0x62	4.7 k	1.2 k
0x0D	0	18 k	0x38	1.8 k	6.8 k	0x63	4.7 k	1.8 k
0x0E	0	22 k	0x39	1.8 k	8.2 k	0x64	4.7 k	2.7 k
0x0F	0	27 k	0x3A	1.8 k	10 k	0x65	4.7 k	3.9 k
0x10	680	0	0x3B	1.8 k	12 k	0x66	4.7 k	4.7 k
0x11	680	680	0x3C	1.8 k	15 k	0x67	4.7 k	5.6 k
0x12	680	1.2 k	0x3D	1.8 k	18 k	0x68	4.7 k	6.8 k
0x13	680	1.8 k	0x3E	1.8 k	22 k	0x69	4.7 k	8.2 k
0x14	680	2.7 k	0x3F	1.8 k	27 k	0x6A	4.7 k	10 k
0x15	680	3.9 k	0x40	2.7 k	0	0x6B	4.7 k	12 k
0x16	680	4.7 k	0x41	2.7 k	680	0x6C	4.7 k	15 k
0x17	680	5.6 k	0x42	2.7 k	1.2 k	0x6D	4.7 k	18 k
0x18	680	6.8 k	0x43	2.7 k	1.8 k	0x6E	4.7 k	22 k
0x19	680	8.2 k	0x44	2.7 k	2.7 k	0x6F	4.7 k	27 k
0x1A	680	10 k	0x45	2.7 k	3.9 k	0x70	5.6 k	0
0x1B	680	12 k	0x46	2.7 k	4.7 k	0x71	5.6 k	680
0x1C	680	15 k	0x47	2.7 k	5.6 k	0x72	5.6 k	1.2 k
0x1D	680	18 k	0x48	2.7 k	6.8 k	0x73	5.6 k	1.8 k
0x1E	680	22 k	0x49	2.7 k	8.2 k	0x74	5.6 k	2.7 k
0x1F	680	27 k	0x4A	2.7 k	10 k	0x75	5.6 k	3.9 k
0x20	1.2 k	0	0x4B	2.7 k	12 k	0x76	5.6 k	4.7 k

Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω
0x21	1.2 k	680	0x4C	2.7 k	15 k	0x77	5.6 k	5.6 k
0x22	1.2 k	1.2 k	0x4D	2.7 k	18 k	0x78*	5.6 k	6.8 k
0x23	1.2 k	1.8 k	0x4E	2.7 k	22 k	0x79*	5.6 k	8.2 k
0x24	1.2 k	2.7 k	0x4F	2.7 k	27 k	0x7A*	5.6 k	10 k
0x25	1.2 k	3.9 k	0x50	3.9 k	0	0x7B*	5.6 k	12 k
0x26	1.2 k	4.7 k	0x51	3.9 k	680	0x7C*	5.6 k	15 k
0x27	1.2 k	5.6 k	0x52	3.9 k	1.2 k	0x7D*	5.6 k	18 k
0x28*	1.2 k	6.8 k	0x53	3.9 k	1.8 k	0x7E*	5.6 k	22 k
0x29	1.2 k	8.2 k	0x54	3.9 k	2.7 k	0x7F*	5.6 k	27 k
0x2A	1.2 k	10 k	0x55	3.9 k	3.9 k			

Note 2: The gray-highlighted addresses with an asterick are reserved by the SMBus specification.

PMBUS COMMANDS

A detailed description of the PMBus commands supported by the EM2260 can be found in a separate document - *EM22xx PMBus Commands Guide.* Below, Table **13** lists of all supported PMBus commands.

Table 14 : List of Supported PMBus Commands

Command Code	PMBus Parameter	Description	Default Value
01_{HEX}	**OPERATION**	On/off command	0x00*
02_{HEX}	**ON_OFF_CONFIG**	On/off configuration	0x16*
03_{HEX}	**CLEAR_FAULTS**	Clear status information	N/A
10_{HEX}	**WRITE_PROTECT**	Protect against changes	0x00
11_{HEX}	**STORE_DEFAULT_ALL**	Copy entire memory into OTP	N/A
12_{HEX}	**RESTORE_DEFAULT_ALL**	Copy entire memory from OTP	N/A
13_{HEX}	**STORE_DEFAULT_CODE**	Copy single parameter into OTP	N/A
14_{HEX}	**RESTORE_DEFAULT_CODE**	Copy single parameter from OTP	N/A
19_{HEX}	**CAPABILITY**	PMBus Capabilities	0xB0
20_{HEX}	**VOUT_MODE** (*Note 3*)	Exponent of the VOUT_COMMAND value	0x13
21_{HEX}	**VOUT_COMMAND**	Set output voltage	0x1CCC*
22_{HEX}	**VOUT_TRIM**	Apply a fixed offset voltage	0x0000
23_{HEX}	**VOUT_CAL_OFFSET**	Apply a fixed offset voltage	0x0000
25_{HEX}	**VOUT_MARGIN_HIGH**	Sets maximum value	0x1FAE* (0.99V)
26_{HEX}	**VOUT_MARGIN_LOW**	Sets minimum value	0x19EB* (0.81V)

Command Code	PMBus Parameter	Description	Default Value
29_{HEX}	**VOUT_SCALE_LOOP**	Scalar for output voltage divider	0xBA00
$2A_{HEX}$	**VOUT_SCALE_MONITOR**	Scalar for read-back with output voltage divider	0xBA00
35_{HEX}	**VIN_ON**	Input voltage turn on threshold	0xCA34
36_{HEX}	**VIN_OFF**	Input voltage turn off threshold	0xCA1A
40_{HEX}	**VOUT_OV_FAULT_LIMIT**	Over-voltage fault limit	0x228F* (1.08V)
41_{HEX}	**VOUT_OV_FAULT_RESPONSE**	Over-voltage fault response	0xB0
42_{HEX}	**VOUT_OV_WARN_LIMIT**	Over-voltage warning level	0x1ED0* (0.963V)
43_{HEX}	**VOUT_UV_WARN_LIMIT**	Under-voltage warning level	0x1AC8* (0.937V)
44_{HEX}	**VOUT_UV_FAULT_LIMIT**	Under-voltage fault level	0x187A* (0.765V)
45_{HEX}	**VOUT_UV_FAULT_RESPONSE**	Under-voltage fault response	0xB0
$4F_{HEX}$	**OT_FAULT_LIMIT**	Power Train Over-temperature fault level	0xEBE7
50_{HEX}	**OT_FAULT_RESPONSE**	Power Train Over-temperature fault response	0xB8
51_{HEX}	**OT_WARN_LIMIT**	Power Train Over-temperature warning level	0xEBBF
55_{HEX}	**VIN_OV_FAULT_LIMIT**	Over-voltage fault limit	0xDA0E* (16.44V)
56_{HEX}	**VIN_OV_FAULT_RESPONSE**	Over-voltage fault response	0X80
57_{HEX}	**VIN_OV_WARN_LIMIT**	Over-voltage warning level	0xD3FD* (15.96V)
58_{HEX}	**VIN_UV_WARN_LIMIT**	Under-voltage warning level	0xCA19* (4.2V)
59_{HEX}	**VIN_UV_FAULT_LIMIT**	Under-voltage fault level	0xC3F5* (3.96V)
$5A_{HEX}$	**VIN_UV_FAULT_RESPONSE**	Under-voltage fault response	0xB8
$5E_{HEX}$	**POWER_GOOD_ON**	Power good on threshold	0x1B85* (0.86V)
$5F_{HEX}$	**POWER_GOOD_OFF**	Power good off threshold	0x19EB* (0.81V)
60_{HEX}	**TON_DELAY**	Turn-on delay	0xF800* (0ms)

Command Code	PMBus Parameter	Description	Default Value
61HEX	**TON_RISE**	Turn-on rise time	0xBB54* (1.666ms)
62HEX	**TON_MAX_FAULT_LIMIT**	Turn-on maximum fault time	0xCA6F* (4.867ms)
64HEX	**TOFF_DELAY**	Turn-off delay	0xF800* (0ms)
65HEX	**TOFF_FALL**	Turn-off fall time	0xBB54* (1.666ms)
66HEX	**TOFF_MAX_WARN_LIMIT**	Turn-off maximum warning time	0xCA6F* (4.867ms)
78HEX	**STATUS_BYTE**	Unit status byte	0x00*
79HEX	**STATUS_WORD**	Unit status word	0x0000*
7AHEX	**STATUS_VOUT**	Output voltage status	0x00*
7BHEX	**STATUS_IOUT**	Output current status	0x00*
7CHEX	**STATUS_INPUT**	Input status	0x00*
7EHEX	**STATUS_CML**	Communication and memory status	0x00*
80HEX	**STATUS_MFR_SPECIFIC**	Manufacturer specific status	0x00*
88HEX	**READ_VIN**	Reads input voltage	0x00*
8BHEX	**READ_VOUT**	Reads output voltage	0x1CC8* (0.8994V)
8CHEX	**READ_IOUT**	Reads output current	0x0000* (0A)
8DHEX	**READ_TEMPERATURE_1**	Power Train Temperature read back	0xDB20* (25ºC)
8EHEX	**READ_TEMPERATURE_2**	Controller Temperature read back	0xDB20* (25ºC)
94HEX	**READ_DUTY_CYCLE**	Current Duty Cycle read back	0xCB0F*
95HEX	**READ_FREQUENCY**	Reads switching frequency	0x0320
96HEX	**READ_POUT**	Reads output power	0x0000*
98HEX	**PMBUS™_REVISION**	PMBus™ revision	0x33
99HEX	**MFR_ID**	Manufacturer ID	0x04494E544C
9AHEX	**MFR_MODEL**	Manufacturer model identifier	0x0432323630
9BHEX	**MFR_REVISION**	Manufacturer product revision	0x0830302E39382E3338
A0HEX	**MFR_VIN_MIN**	Minimum input voltage	0xC265

Command Code	PMBus Parameter	Description	Default Value
$A4_{HEX}$	**MFR_VOUT_MIN**	Minimum output voltage	0xA3D6
AD_{HEX}	**IC_DEVICE_ID**	Device Family ID #	0x0438323031
AE_{HEX}	**IC_DEVICE_REV**	Device IC revision #	0x0131
$D0_{HEX}$	**MFR_SPECIFIC_00**	Write word (once) / Read word – 2 bytes	0x00
$D1_{HEX}$	**MFR_SPECIFIC_01**	Write word / read word – 12 bytes	0x00
$D2_{HEX}$	**MFR_READ_VCC**	Reads VCC voltage	0xCA80* (5.0V)
DA_{HEX}	**MFR_RTUNE_CONFIG**	Gets/sets RTUNE settings	0x2000*
DD_{HEX}	**MFR_RTUNE_INDEX**	Returns index derived from resistor detected on RTUNE pin	0x01*
DE_{HEX}	**MFR_RVSET_INDEX**	Returns index derived from resistor detected on RVSET pin	0x0F* (0.9V)
$E0_{HEX}$	**MFR_VOUT_OFF**	Sets the target turn-off voltage	0x0000
$E2_{HEX}$	**MFR_OT_FAULT_LIMIT**	Controller Over-temperature fault level	0xEBBF* (119.875ºC)
$E3_{HEX}$	**MFR_OT_WARN_LIMIT**	Controller Over-temperature warning level	0xEB6F* (109.875ºC)
$E5_{HEX}$	**MFR_OT_FAULT_RESPONSE**	Controller Over-temperature fault response	0xB8
$E6_{HEX}$	**MFR_TEMP_ON**	Over-temperature on level	0xEB51* (106.125ºC)
$E7_{HEX}$	**MFR_PIN_CONFIG**	Enable/disable – RTUNE, RVSET, VTRACK and SYNC	0x00BC
$E9_{HEX}$	**MFR_STORE_CONFIG_ADDR_READ**	Reads a configuration value	N/A
EA_{HEX}	**MFR_STORE_PARAMS_REMAINING**	Number of STORE_DEFAULT_ALL commands remaining	-
EB_{HEX}	**MFR_STORE_CONFIGS_REMAINING**	Number of full configurations remaining	-
EC_{HEX}	**MFR_STORE_CONFIG_BEGIN**	Commence programming of OTP	N/A
ED_{HEX}	**MFR_STORE_CONFIG_ADDR_DATA**	Program a configuration value	N/A
EE_{HEX}	**MFR_STORE_CONFIG_END**	Completed programming of OTP	N/A

Note 3: VOUT_ MODE is read only for the EM2260

Note 4: *All values relevant to VOUT = 0.9V (RVSET = 5k36V & RTUNE = Index1 0Ohms), VOUT operating and no Fault or warning events occurring. Also some values may vary slightly due to digital read-back.

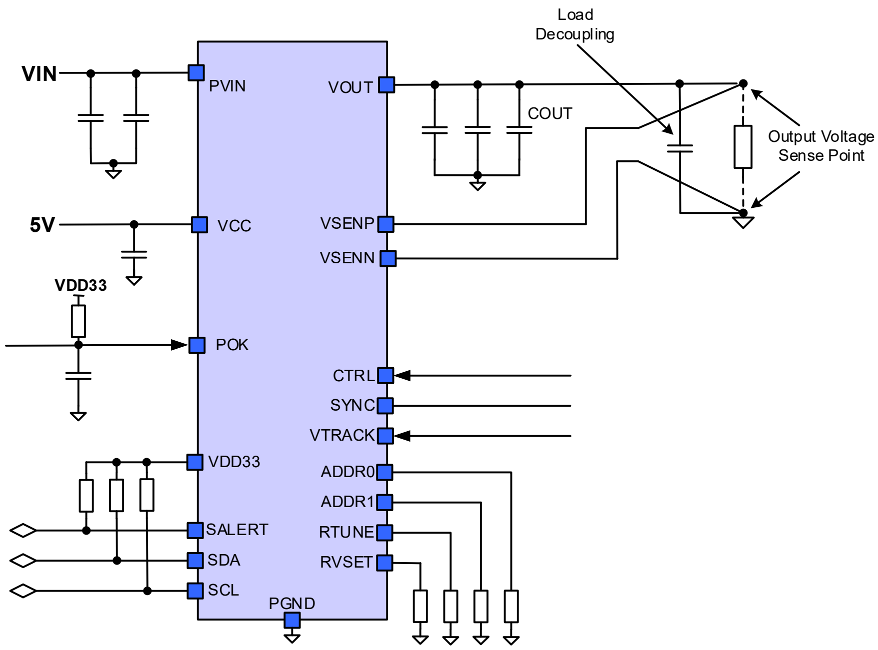


Figure 15: Recommended Application Circuit

Layout Recommendations

Recommendation 1: It is good practice to minimize ground loops. Whenever possible the input and output loops should close to the same point, which is the ground of the EM2260 module. Module decoupling ceramic capacitors are to be placed as close as possible to the module in order to contain the switching noise in the smallest possible loops and to improve PVIN decoupling by minimizing the series parasitic inductance of the PVIN traces. For achieving this goal, it helps to place decoupling capacitors on the same side as the module since VIAs are generally more inductive, thus reducing the effectiveness of the decoupling. Of course, bulk and load high frequency decoupling should be placed closer to the load.

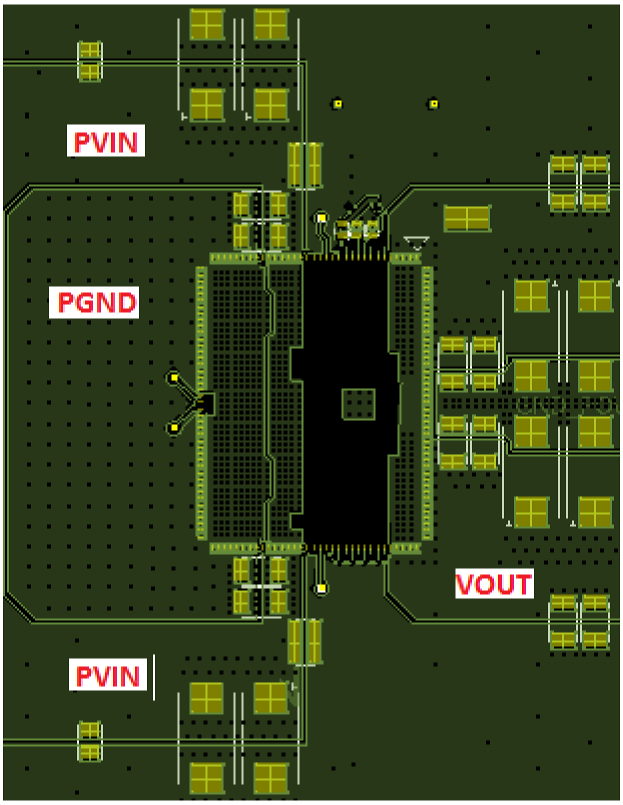


Figure 16: Top Layer Layout with Critical Components Only

Recommendation 2: It is good practice to place the other small components needed by the EM2260 on the opposite side of the board, in order to avoid cutting the power planes on the module side. Since the EM2260's heat is evacuated mostly through the PCB, this will also help with heat dissipation; wide copper planes under the module can also help with cooling. The PVIN copper plane should not be neglected as it helps spread the heat from the high side FET.

Recommendation 3: It is recommended that at least below the EM2260 module, the next layers to the surface (2 and n-1) be solid ground planes, which provides shielding and lower the ground impedance at the module level, in order to reduce the ground impedance and reduce noise injection.

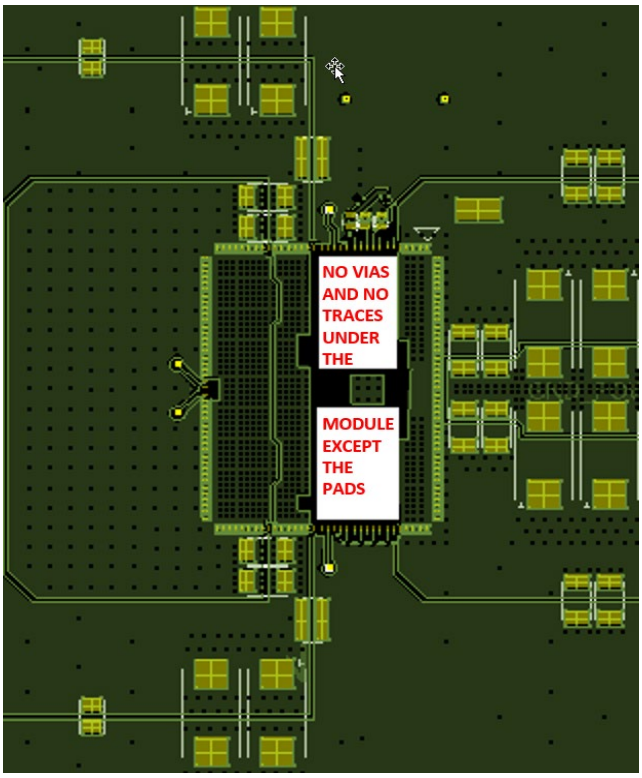


Figure 17: VIAs in the Power Pads

Recommendation 4: In order to better spread the current and the heat through the inner layers, arrays of VIAs should be placed in the power pads. 10mils diameter is a good size for the plated in-pad VIAs. It is critical that through VIAs should not be placed by any means elsewhere under the module; the non-pad area around GND is VIA keep out area.

Recommendation 5: All other signal and LDO decoupling capacitors should be placed as close as possible to the terminal they are decoupling.

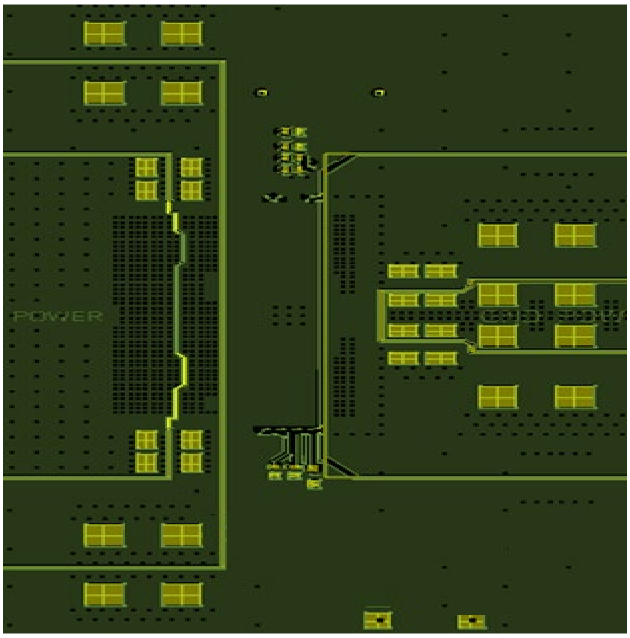


Figure 18: Backside Decoupling
All Signal Decoupling goes to the Bottom GND Plane and gets connected to the EM2260 Module GND through the GND In-PAD VIAs (Again, no other VIAs are allowed in that Area)

Recommendation 6: Differential remote sense should be routed as much as possible as a differential pair, on an inner layer, preferably shielded by a ground plane.

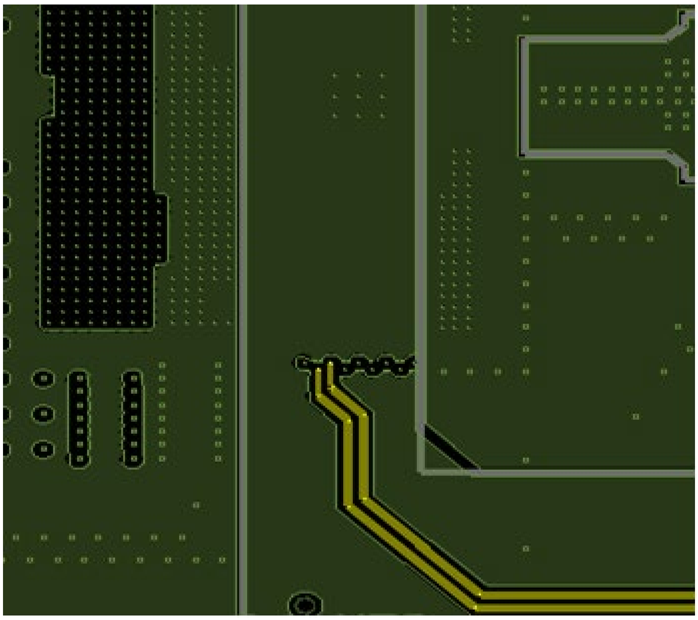


Figure 19: Remote Sense Routing on An Inner Layer (Highlighted, Yellow)

Recommendation 7: If the design allows it, stitching VIAs can be used on the power planes, close to the module in order to help with cooling. This is a thermal consideration and does not matter much for the electrical design.

Package Bottom Side View

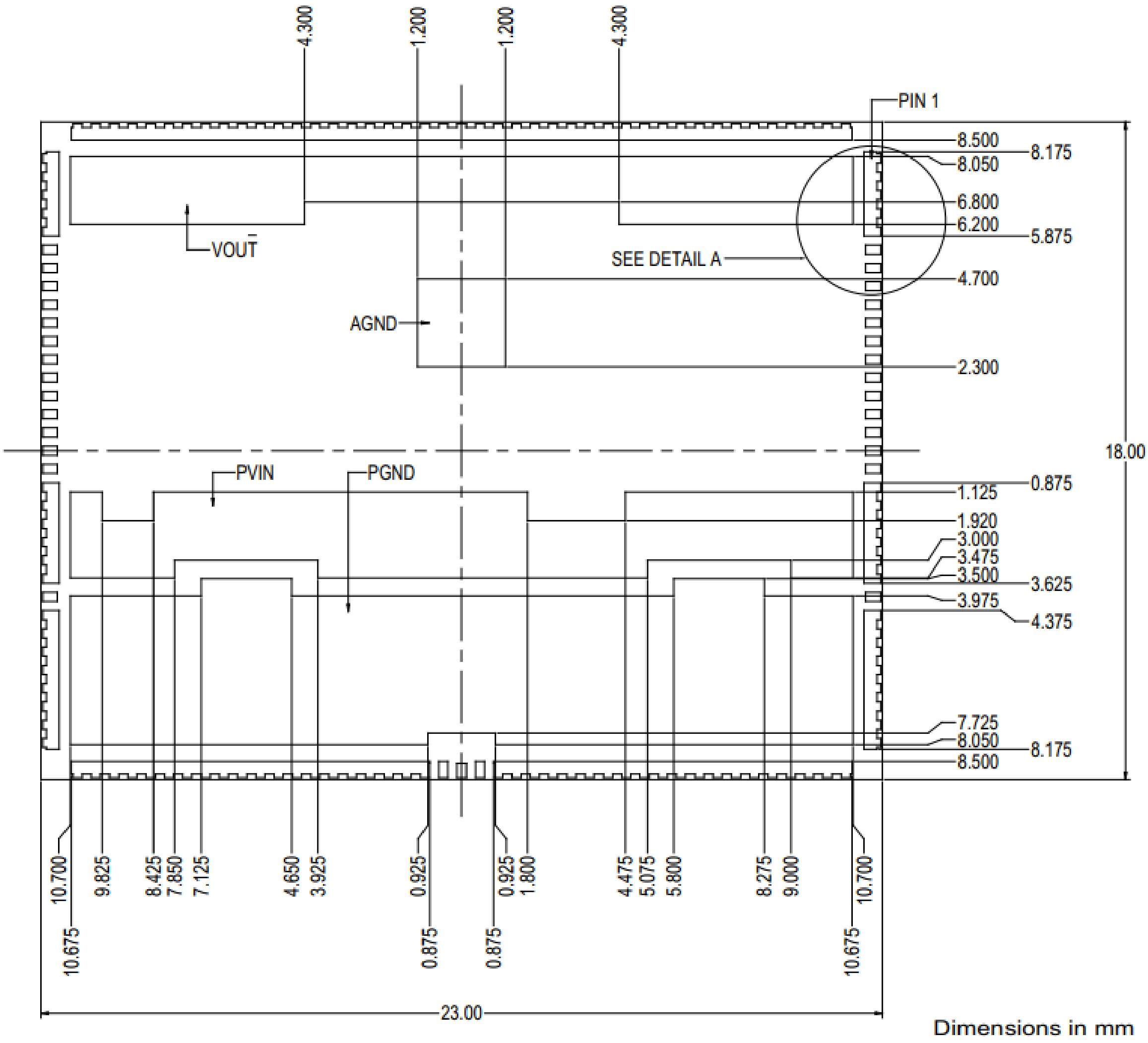


Figure 20: Package Bottom side (Bottom View)

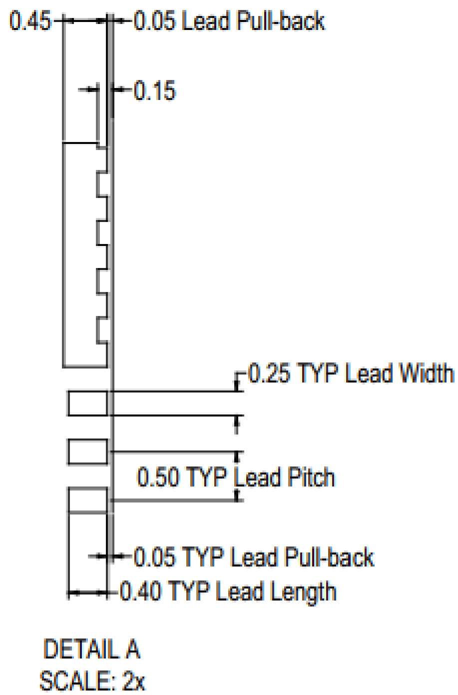


Figure 21: Package Bottom side Detail A

Recommended PCB Footprint

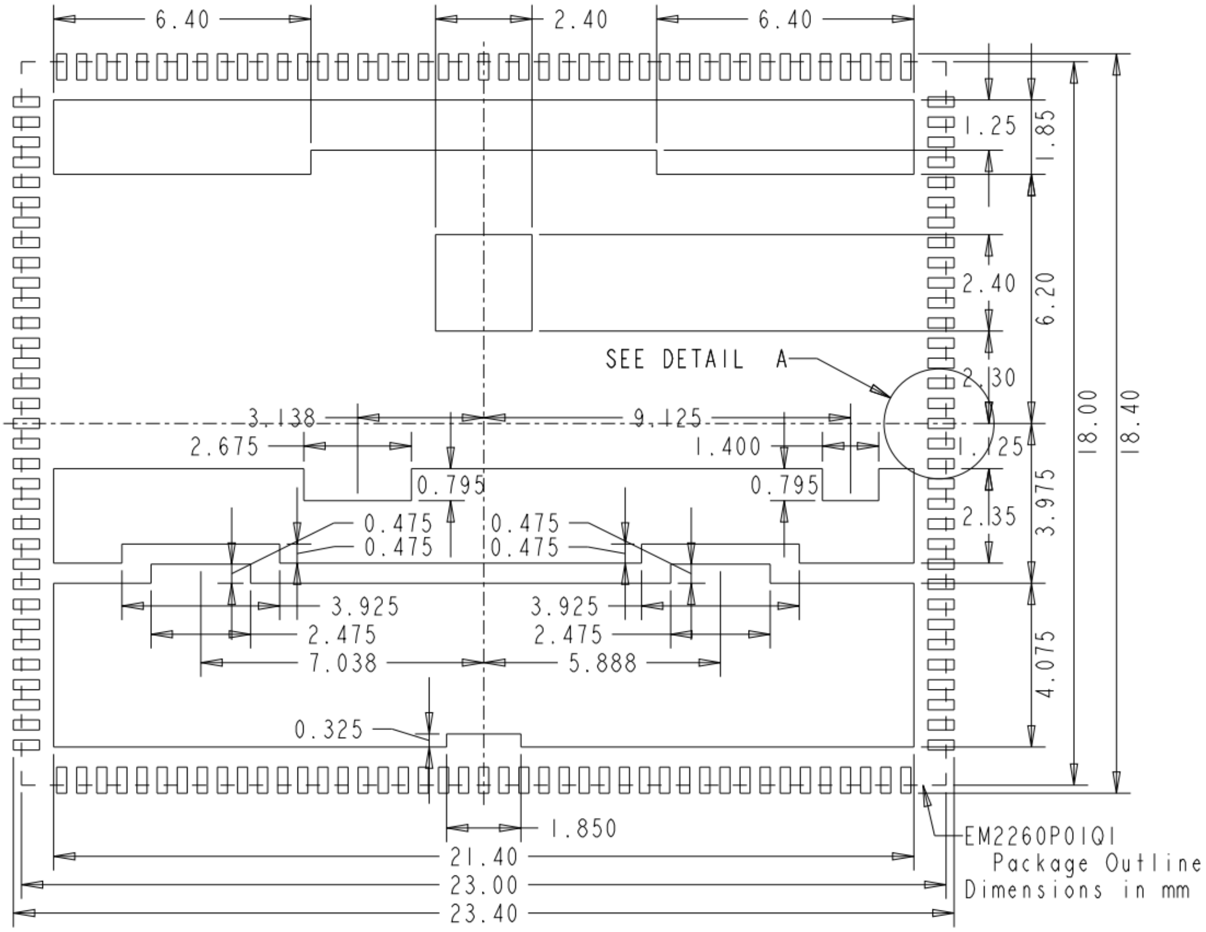


Figure 22: Recommended PCB Footprint (Top View)

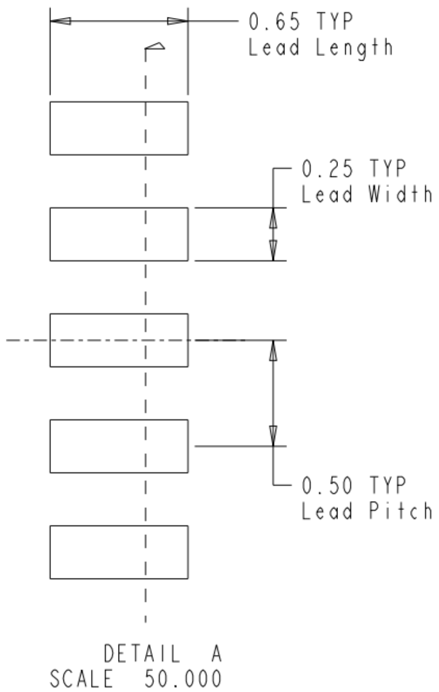


Figure 23: Recommended PCB Footprint Detail A

30% Solder Stencil Aperture (see note below)

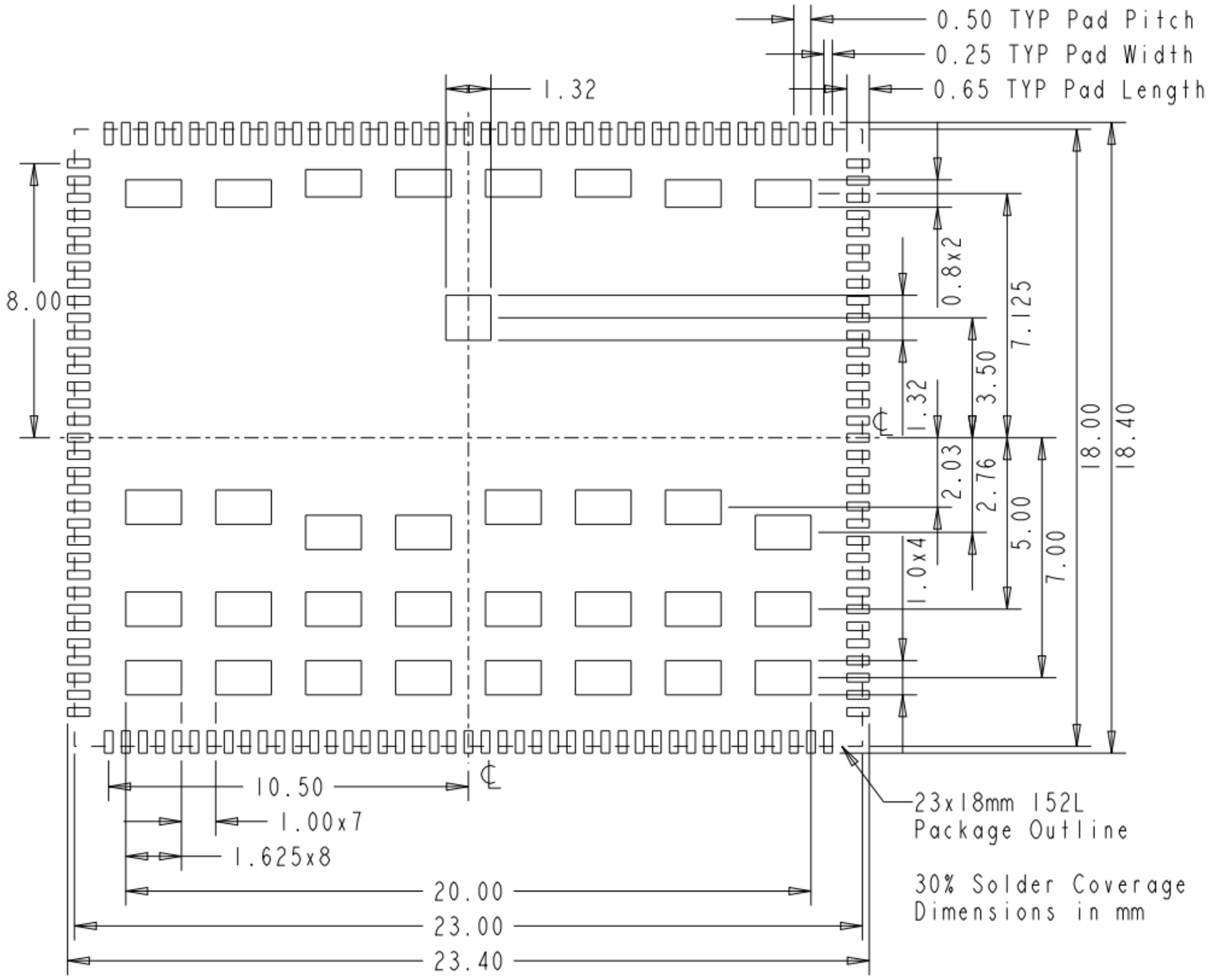


Figure 24: 30% Solder Stencil Aperture Dimensions

Notes:

- The solder stencil for each pad under the device is recommended to be up to 30% of the total pad size.
- The aperture dimensions are based on a 4mil stencil thickness

Package Dimensions

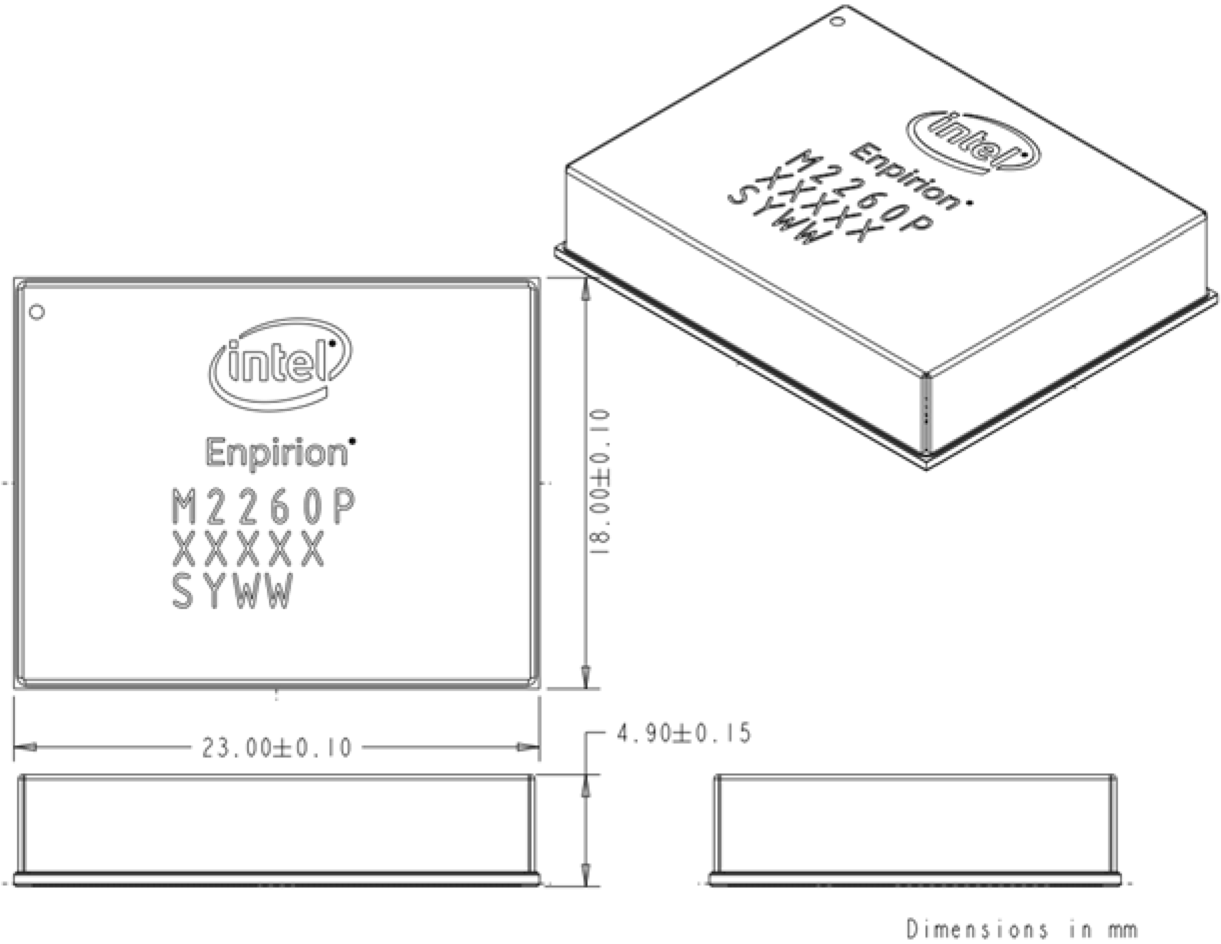


Figure 25: Package Dimensions 1/3

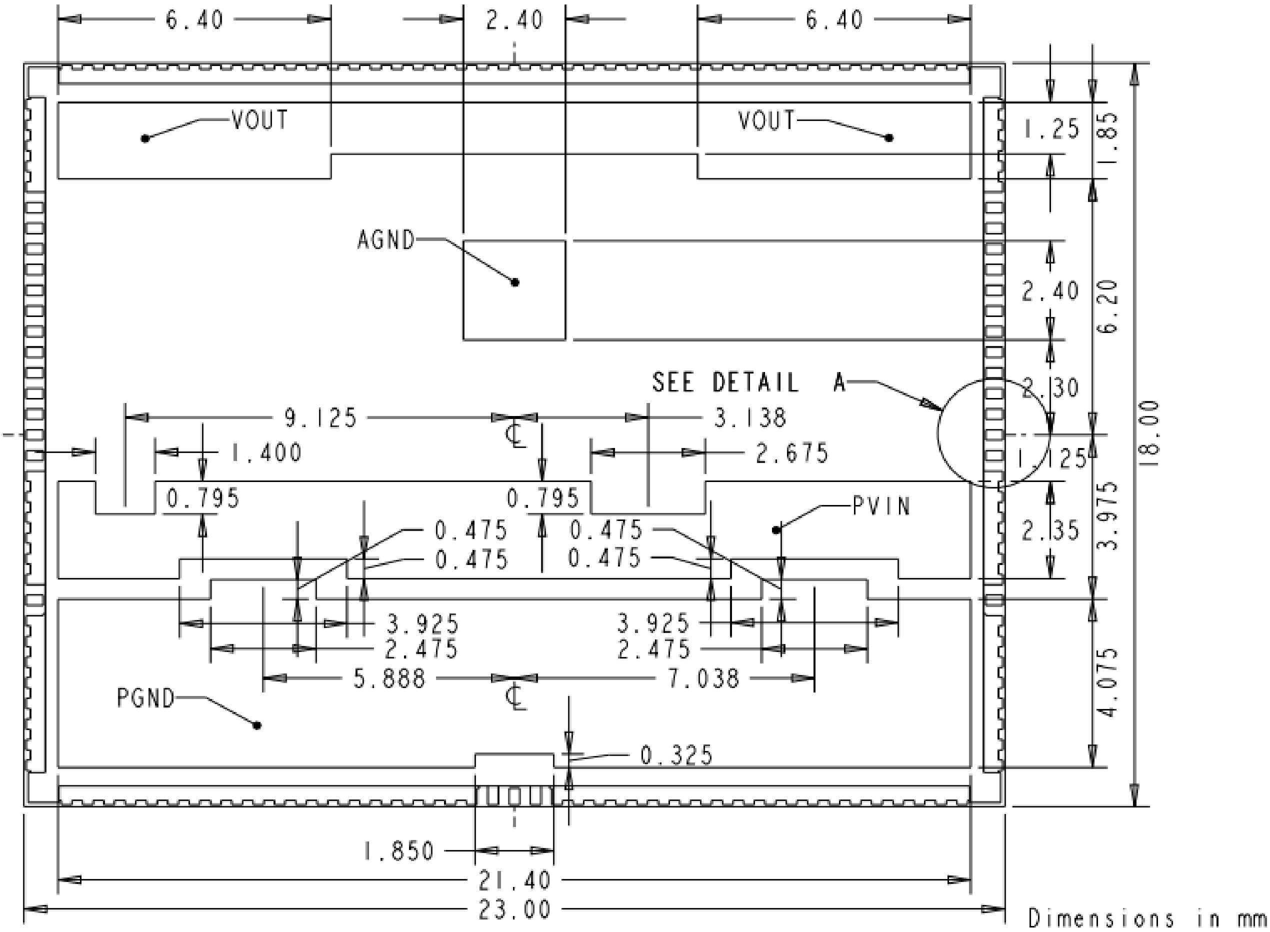


Figure 26: Package Dimensions 2/3

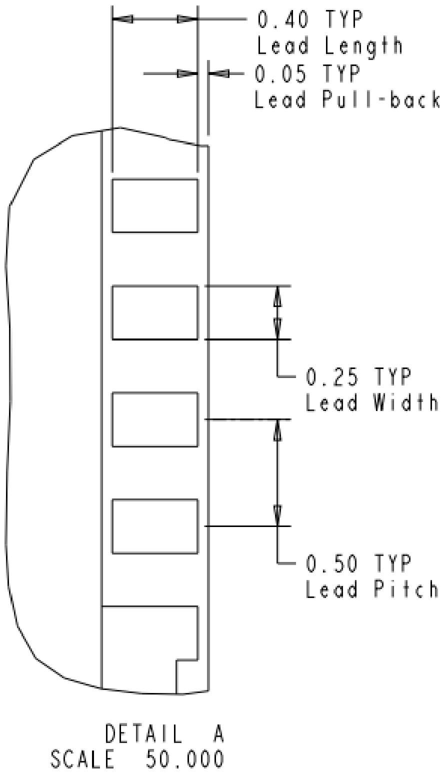


Figure 27: Package Dimensions 3/3

Tray Information

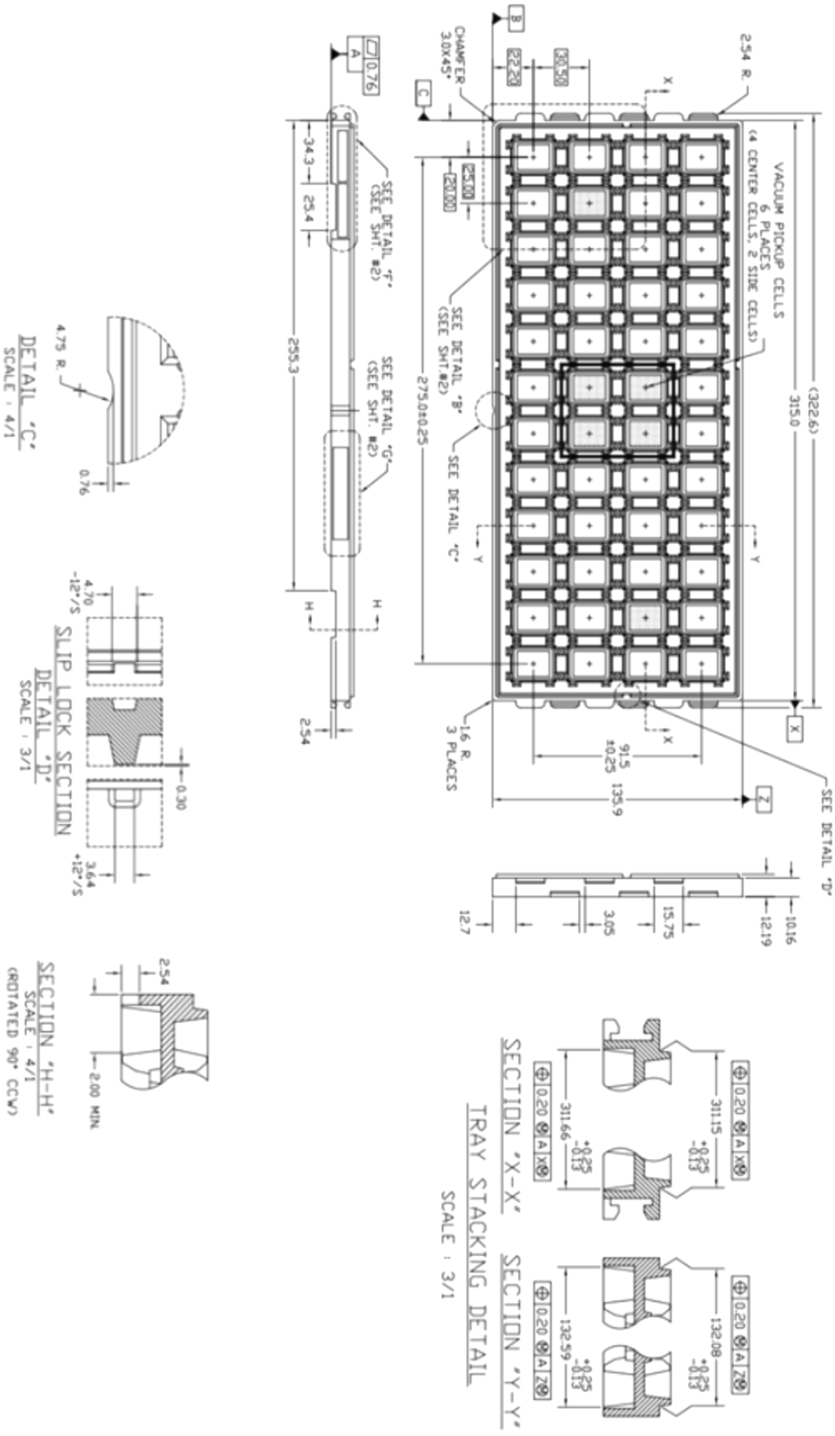


Figure 28: Tray Information 1/2

Tray Information (Continued)

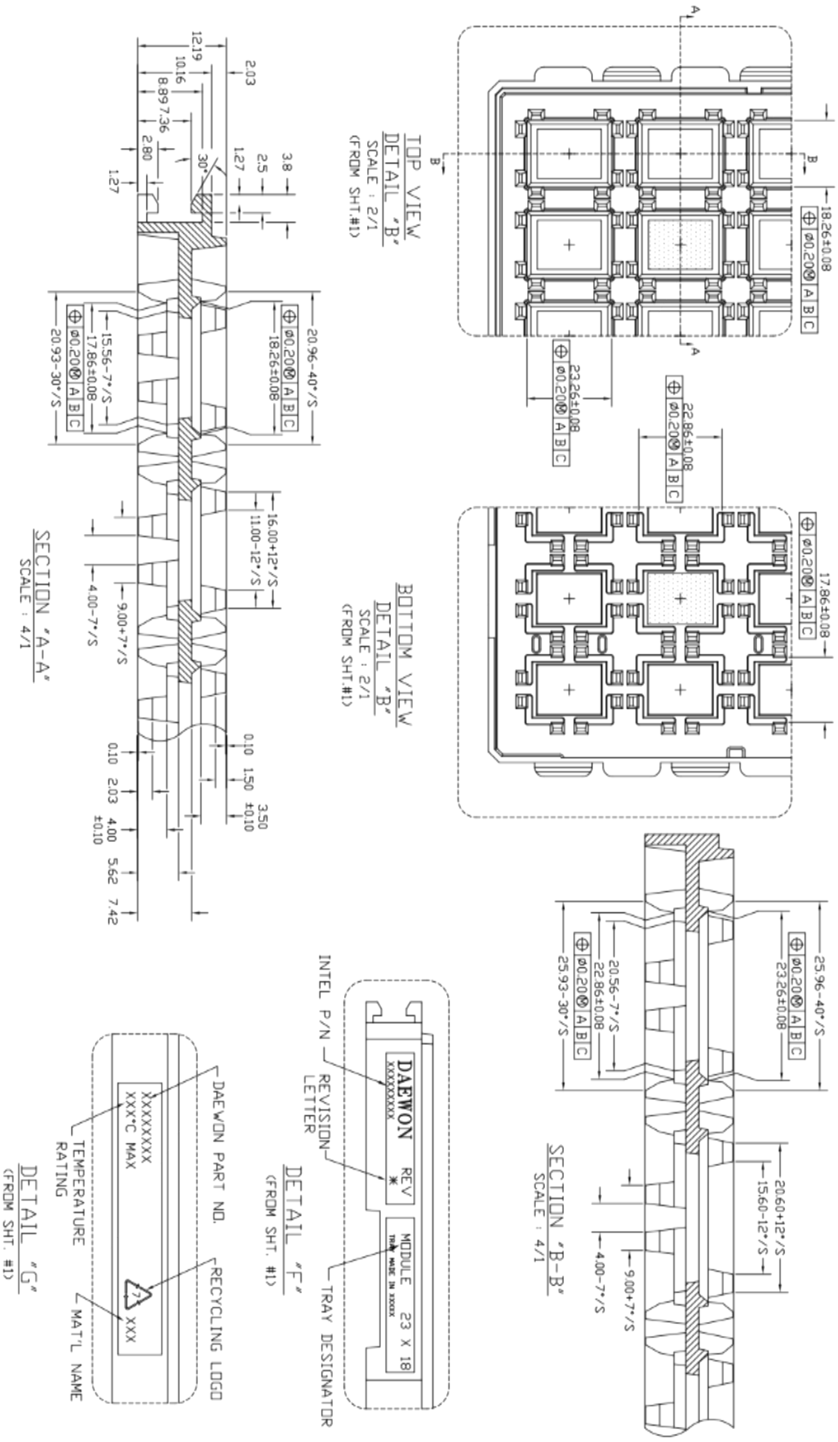


Figure 29: Tray Information 2/2

Revision History

Rev	Date	Change(s)
A	Jan 18	Initial Release
B	Mar 18	Update drawings and small edits.
C	May 18	Update to PMBus section and note on Watchdog Timer
D	Jun 18	Rev. control changed from Numbers to Letters
E	Jul 18	Added the solder stencil options for 30% & 45% opening
F	Mar 20	Added information relating to SMBALERT, removed stencil option for 45% opening

Where to Get More Information

For more information about Intel and Intel Enpirion PowerSoCs, visit **https://www.altera.com/enpirion**