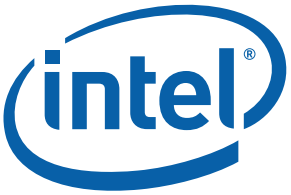

Intel® Core™ i7-660UE, i7-620LE/ UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series

Datasheet Addendum

August 2010

Document Number: 323178-003

Contents

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Tables

Revision History

Date	Revision	Description
January 2010	001	• Initial release of this document.
April 2010	002	• Added information for the Intel® Celeron® Processor P4500 and P4505 Series. • Corrected first bullet in Section 2.1.1 to “No support for mixed ECC and non-ECC DIMM configurations.”
August 2010	003	• Added information for the Intel® Core™ i7-660UE, i3-330E and Celeron® Processor U3405 • Removed all references to Celeron® Processor P4500 since it is a PGA package and does not relate to this document (was included by error in last revision). • CMD mode for DDR3 is restated to 1n instead of 1n and 2n

1 Introduction and Features Summary

1.1 Introduction

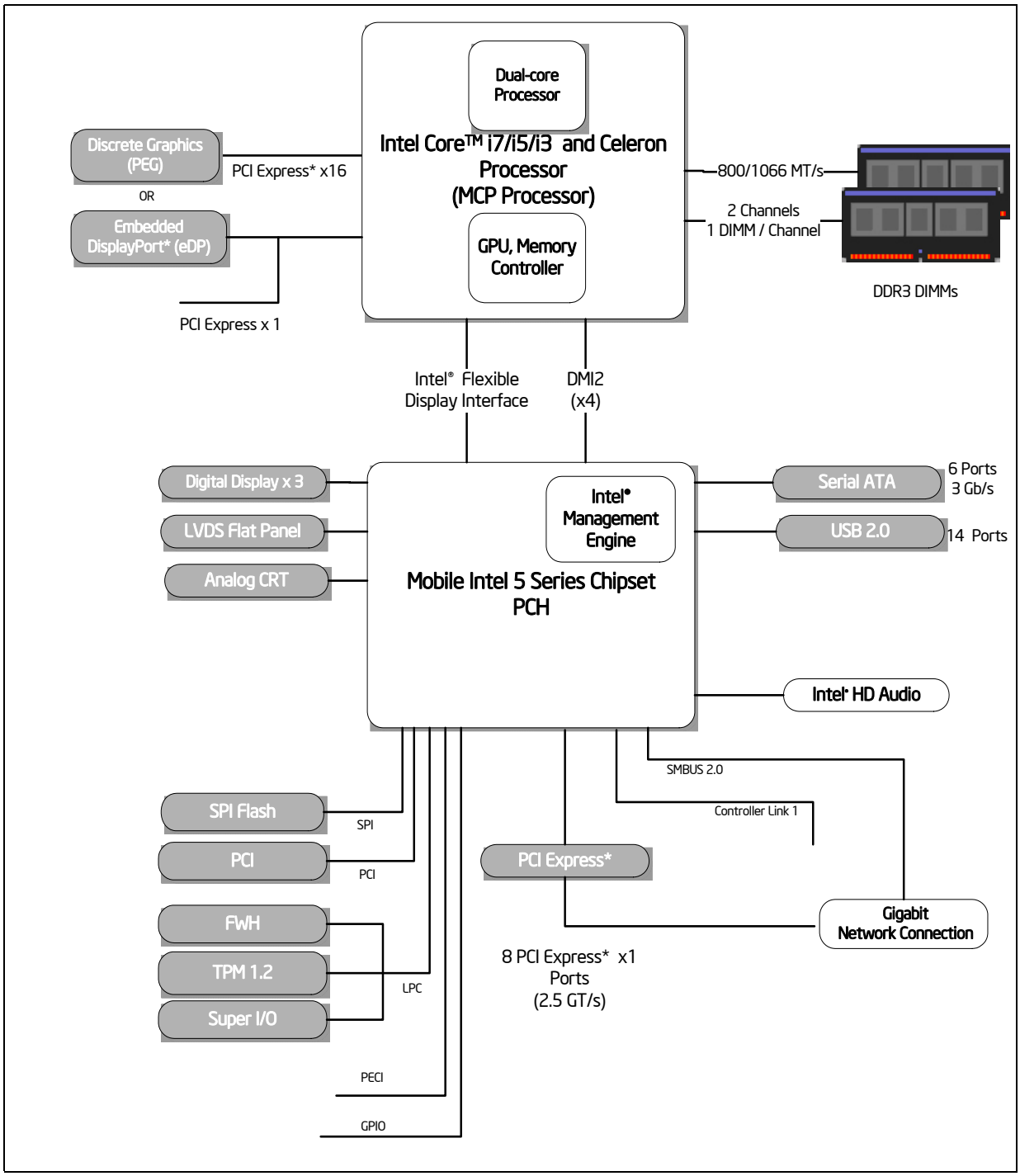
This Datasheet Addendum is a supplement to the *Intel® Core™ i7-600, i5-500 and i3-300 Mobile Processor Series Datasheet*. It contains the additional DC and AC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, additional feature information and configuration registers pertinent to the implementation and operation of the Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series on its respective platform.

Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series is the next generation of 64-bit, multi-core mobile processor built on a 32- nanometer process technology. Throughout this document, Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series may be referred to as simply the processor. The processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint. The PCH may also be referred to as Mobile Intel® 5 Series Chipset (formerly Ibex Peak-M). Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series is designed for the Intel® Core™ i7 processor based low-power platform and is offered in a BGA1288 package.

Included in this family of processors is an integrated graphics and memory controller die on the same package as the processor core die. This two-chip solution of a processor core die with an integrated graphics and memory controller die is known as a multi-chip package (MCP) processor.

Note: Integrated graphics and memory controller die is built on 45-nanometer process technology.

Figure 1. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series on the Intel® Core™ i7 processor based low-power platform



1.2 Interfaces

1.2.1 System Memory Support

- One or two channels of DDR3 memory with a maximum of one DIMM per channel
- Single- and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- Memory DDR3 data transfer rates of 800 and 1066 MT/s
- 64-bit wide channels (72-bit wide including ECC)
- DDR3 I/O Voltage of 1.5 V
- Supports ECC and non-ECC, unbuffered DDR3 DIMMs
  - — Mixing of ECC and Non-ECC DIMMS is not supported
- Theoretical maximum memory bandwidth of:
  - — 12.8 GB/s in dual-channel mode assuming DDR3 800 MT/s
  - — 17.1 GB/s in dual-channel mode assuming DDR3 1066 MT/s
- 1-Gb, and 2-Gb DDR3 DRAM technologies for x8 and x16 devices
- Using 2-Gb device technologies, the largest memory capacity possible is 8 GB, assuming dual-channel mode with two x8, dual-rank, un-buffered, DIMM memory configuration.
- Up to 32 simultaneous open pages, 16 per channel (assuming 4 Ranks of 8 Bank Devices)
- Memory organizations:
  - — Single-channel modes
  - — Dual-channel modes
    Dual-channel symmetric (Interleaved)
    Dual-channel asymmetric
    Intel® Flex Memory Technology
- Command launch mode of 1n
- Partial Writes to memory using Data Mask (DM) signals
- On-Die Termination (ODT)
- Intel® Fast Memory Access (Intel® FMA):
  - — Just-in-Time Command Scheduling
  - — Command Overlap
  - — Out-of-Order Scheduling

1.2.2 PCI Express*

- The processor PCI Express* port(s) are fully-compliant to the *PCI Express Base Specification, Revision 2.0* at 2.5GT/s.
- The processor supports:
  - — One 16-lane PCI Express port for graphics or I/O.
  - — Two 8-lane PCI Express ports for graphics or I/O.
- PCI Express Port 0 is mapped to PCI Device 1.
- PCI Express Port 1 is mapped to PCI Device 6.

1.3 Package

The Intel Core i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel Celeron Processor P4505, U3405 Series are available on a 34 x 28 mm BGA package (BGA1288).

Note: Although the BGA1288 package is shared with Intel® Core™ i7-640UM/LM, i7-620M/UM/LM, i5-540M, i5-520M/UM and i5-430M Processor Series they are not ball-out compatible.

1.4 Terminology

Term	Description
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR3	Third generation Double Data Rate SDRAM memory technology
DP	DisplayPort*
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code
eDP*	Embedded DisplayPort*
Intel® DPST	Intel® Display Power Saving Technology
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
EU	Execution Unit
(G)MCH	Legacy component - Graphics Memory Controller Hub.
GPU	Graphics Processing Unit
ICH	The legacy I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the legacy (G)MCH over a proprietary interconnect called DMI.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
Intel® FDI	Intel® Flexible Display Interface.
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
ITPM	Integrated Trusted Platform Module
IOV	I/O Virtualization
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling A high speed, low power data transmission standard used for display connections to LCD panels.
MCP	Multi-Chip Package
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
PCH	Platform Controller Hub. The new 2009 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features. The PCH may also be referred to using the code name Ibex Peak.
PECI	Platform Environment Control Interface

Term	Description
PEG	PCI Express* Graphics. External Graphics using PCI Express Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications.
Processor	The 64-bit, single-core or multi-core component (package)
Processor Core	The term “processor core” refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to “free air” (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TOM	Top of Memory
TTM	Time-To-Market
V_{CC}	Processor core power supply
V_{SS}	Processor ground
V_{AXG}	Graphics core power supply
V_{TT}	L3 shared cache, memory controller, and processor I/O power rail
V_{DDQ}	DDR3 power rail
VLD	Variable Length Decoding
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.5 Related Documents

Refer to the documents in Table 1 for additional information.

Table 1. Processor Documents

Document	Document Number/ Location
Intel® Core™ i7-600, i5-500 and i3-300 Mobile Processor Series Datasheet	http://www.intel.com
Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Datasheet Addendum Specification Update	http://www.intel.com

Table 2. PCH Documents

Document	Document Number / Location
Intel® 5 Series Chipset and Intel® 3400 Series Chipset Datasheet	http://www.intel.com

Table 3. Public Specifications

Document	Document Number / Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express Base Specification 2.0	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

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2 Interfaces

This chapter describes the interfaces supported by the processor.

2.1 System Memory Interface

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3 protocols with two, independent, 64-bit wide channels each accessing one DIMM. It supports:

— ECC and non-ECC un-buffered DIMMs. No support for mixed ECC and non-ECC DIMM configurations.

DDR3 Data Transfer Rates:

— 800 MT/s (PC3-6400), and 1066 MT/s (PC3-8500)

- DDR3 DIMM Modules:
  - — Raw Card A – single rank x8 unbuffered non-ECC
  - — Raw Card B – dual rank x8 unbuffered non-ECC
  - — Raw Card C – single rank x16 unbuffered non-ECC
  - — Raw Card D – single rank x8 unbuffered ECC
  - — Raw Card E – dual rank x8 unbuffered ECC
  - — Raw Card F - dual rank x16 unbuffered non-ECC
- DDR3 DRAM Device Technology:
  - — Standard 1-Gb, and 2-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

Table 4. Supported DIMM Module Configurations (Sheet 1 of 2)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row / Col Address Bits	# of Banks Inside DRAM	Page Size
A	512 MB	512 Mb	64 M x 8	8	1	13/10	8	8K
	1 GB	1 Gb	128 M x 8	8	1	14/10	8	8K
	2 GB	2 Gb	256M x 8	8	1	15/10	8	8K
B	1 GB	512 Mb	64 M x 8	16	2	13/10	8	8K
	2 GB	1 Gb	128 M x 8	16	2	14/10	8	8K
	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K
C	256MB	512 Mb	32 M x 16	4	1	12/10	8	8K
	512 MB	1 Gb	64 M x 8	4	1	13/10	8	8K
	1 GB	2 Gb	128 M x 16	4	1	14/10	8	8K

Table 4. Supported DIMM Module Configurations (Sheet 2 of 2)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row / Col Address Bits	# of Banks Inside DRAM	Page Size
D	512 MB	512 Mb	64 M x 8	9	1	13/10	8	8K
	1 GB	1 Gb	128 M x 8	9	1	14/10	8	8K
	2 GB	2 Gb	256 M x 8	9	1	15/10	8	8K
E	1 GB	512 Mb	64M x 8	18	2	13/10	8	8K
	2 GB	1 Gb	128 M x 8	18	2	14/10	8	8K
	4 GB	2 Gb	256 M x 8	18	2	15/10	8	8K
F	512 MB	512 Mb	32 M x 16	8	2	12/10	8	8K
	1 GB	1 Gb	64 M x 16	8	2	13/10	8	8K
	2 GB	2 Gb	128 M x 16	8	2	14/10	8	8K

2.1.2 System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock. Command launch mode programming depends on the transfer rate and memory configuration.

Table 5. DDR3 System Memory Timing Support

Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	CMD Mode	Notes
800	6	6	6	5	1n	1
1066	7	7	7	6	1n	1
	8	8	8			

NOTES:
1. System Memory timing support is based on availability and is subject to change.

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the DIMM Modules are populated in each memory channel, a number of different configurations can exist.

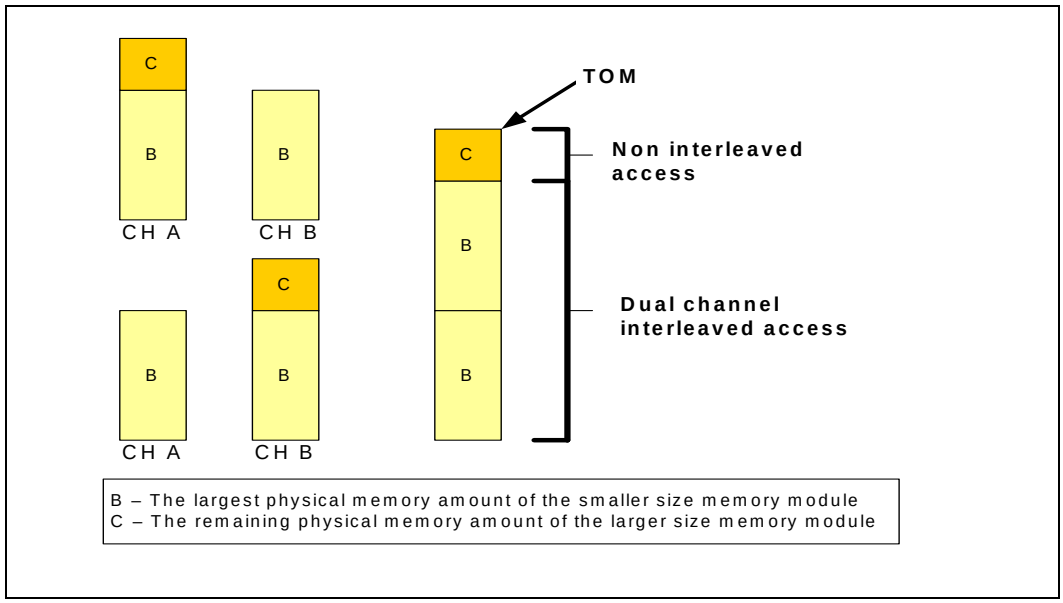
2.1.3.1 Single-Channel Mode

In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B DIMM connectors are populated in any order, but not both.

2.1.3.2 Dual-Channel Mode - Intel® Flex Memory Technology Mode

The IMC supports Intel® Flex Memory Technology Mode. This mode combines the advantages of the Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes. Memory is divided into a symmetric and a asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Figure 2. Intel® Flex Memory Technology Operation



2.1.3.2.1 Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

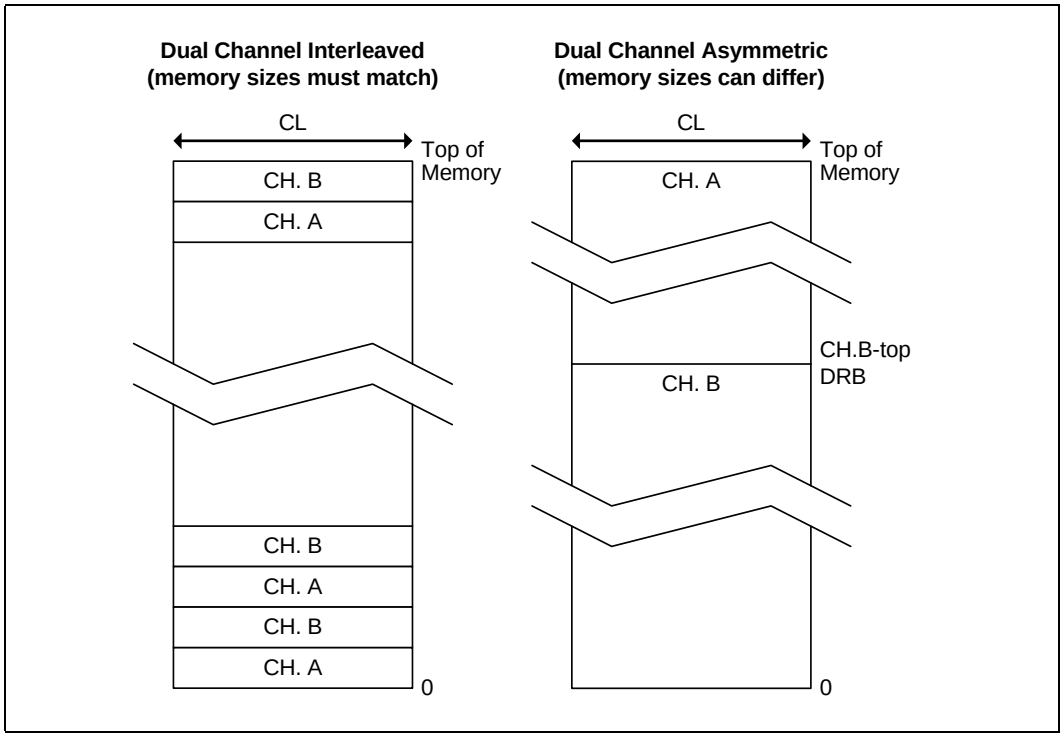
Note: The DRAM device technology and width may vary from one channel to the other.

2.1.3.2.2 Dual-Channel Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start at the bottom of Channel B and stay there until the end of the highest rank in Channel B, and then addresses continue from the bottom of Channel A to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth is limited to a single channel.

This mode is used when Intel® Flex Memory Technology is disabled and both Channel A and Channel B DIMM connectors are populated in any order with the total amount of memory in each channel being different.

Figure 3. Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes



2.1.4 Rules for Populating Memory Slots

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports only one DIMM connector per channel.For dual-channel modes both channels must have an DIMM connector populated and for single-channel mode only a single-channel must have an DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel® FMA technology enhancements.

2.1.5.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without

interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

2.1.5.2 Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.1.5.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 DRAM Clock Generation

Two differential clock pairs for every supported DIMM. There are total of four clock pairs driven directly by the processor to two DIMMs.

2.1.7 DDR3 On-Die Termination

On-Die Termination (ODT) is a feature that allows a DRAM device to turn on/off internal termination resistance for each DQ, DQS/DQS#, and DM signal via the ODT control pin.

The ODT feature improves signal integrity of the memory channel by allowing the DRAM controller to independently turn on or off the termination resistance for any or all DRAM devices themselves instead of on the motherboard.

The IMC drives out the required ODT signals, based on the memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted DIMM module rank to enable or disable their termination resistance.

2.2 PCI Express* Interface

This section describes the PCI Express* interface capabilities of the processor. See the *PCI Express Base Specification* for further details on PCI Express.

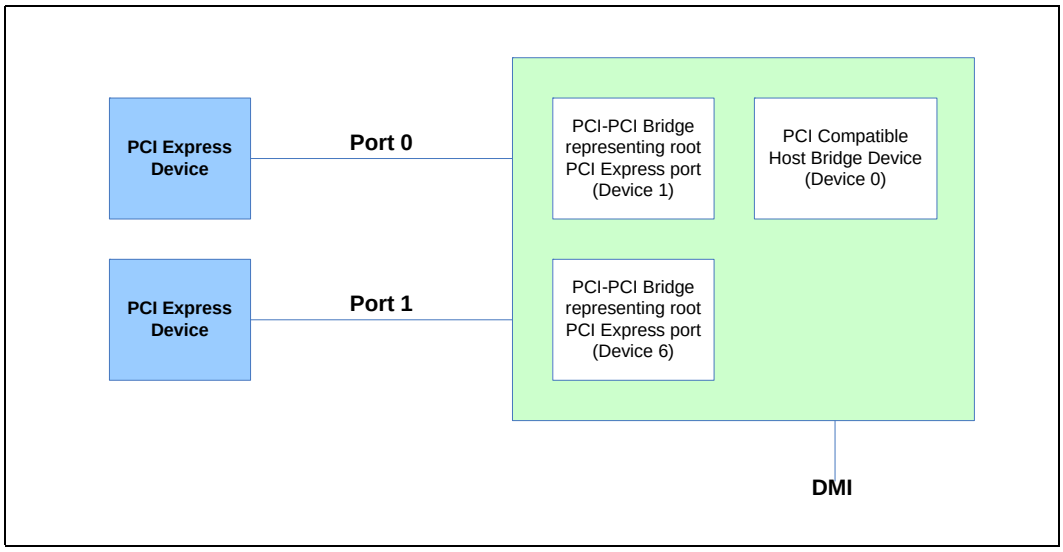
The processor has two options for PCI Express controllers available:

- 1 x16 PCI Express Port
  or
- 2 x8 PCI Express Ports
  - — Enabled with CFG[0] strapping, see Section 2.2.2 and Section 3.2

2.2.1 PCI Express* Configuration Mechanism

The PCI Express* link is mapped through a PCI-to-PCI bridge structure.

Figure 4. PCI Express* Related Register Structures in the Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series



2.2.2 PCI Express Port Bifurcation

When bifurcated, the wires which had previously been assigned to lanes 15:8 of the single x16 primary port (Port 0) are reassigned to lanes 7:0 of the x8 secondary port (Port 1). This assignment applies whether the lane numbering is reversed or not. The controls for the secondary port (Port 1) and the associated virtual PCI-to-PCI bridge can be found in PCI Device 6.

When the primary port is not bifurcated, Device 6 is hidden from the discovery mechanism used in PCI enumeration, such that configuration of the device is neither possible nor necessary.

3 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type:

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal:

Table 6. Signal Description Buffer Types

Signal	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 2.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
FDI	Intel Flexible Display interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3-V tolerant.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3-V tolerant.
CMOS	CMOS buffers. 1.1-V tolerant
DDR3	DDR3 buffers: 1.5-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
GTL	Gunning Transceiver Logic signaling technology.
Ref	Voltage reference signal.
Asynchronous[1]	Signal has no timing relationship with any reference clock.

NOTES:
1. Qualifier for a buffer type.

3.1 System Memory Interface

Table 7. Memory Channel A (Sheet 1 of 2)

Signal Name	Description	Direction/Buffer Type
SA_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SA_WE#	**Write Enable Control Signal:** Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O DDR3

Table 7. Memory Channel A (Sheet 2 of 2)

Signal Name	Description	Direction / Buffer Type
SA_RAS#	**RAS Control Signal:** Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_CAS#	**CAS Control Signal:** Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_DM[7:0]	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane.	O DDR3
SA_DQS[8]	**ECC Data Strobe**: SA_DQS[8] is the data strobe for the ECC check data bits SA_DQ[71:64] **Note**: Not required for non-ECC mode	I/O DDR3
SA_DQS[7:0]	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS#[7:0] during read and write transactions	I/O DDR3
SA_DQS#[8]	**ECC Data Strobe Complement**: SA_DQS#[8] is the complement strobe for the ECC check data bits SA_DQ[71:64] **Note**: Not required for non-ECC mode	I/O DDR3
SA_DQS#[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O DDR3
SA_DQ[71:64]	**ECC Check Data Bits:** SA_DQ[71:64] are the ECC check data bits for Channel A. **Note**: Not required for non-ECC mode	I/O DDR3
SA_DQ[63:0]	**Data Bus:** Channel A data signal interface to the SDRAM data bus.	I/O DDR3
SA_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SA_CK[1:0]	**SDRAM Differential Clock:** Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CK and the negative edge of its complement SA_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SA_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel A SDRAM Differential clock signal-pair complement.	O DDR3
SA_CKE[1:0]	**Clock Enable:** (1 per rank) Used to: - Initialize the SDRAMs during power-up - Power-down SDRAM ranks - Place all SDRAM ranks into and out of self-refresh during STR	O DDR3
SA_CS#[1:0]	**Chip Select:** (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SA_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3

Table 8. Memory Channel B (Sheet 1 of 2)

Signal Name	Description	Direction / Buffer Type
SB_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SB_WE#	**Write Enable Control Signal:** Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O DDR3
SB_RAS#	**RAS Control Signal:** Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_CAS#	**CAS Control Signal:** Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_DM[7:0]	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane.	O DDR3
SB_DQS[8]	**ECC Data Strobe**: SB_DQS[8] is the data strobe for the ECC check data bits SB_DQ[71:64] **Note**: Not required for non-ECC mode	I/O DDR3
SB_DQS[7:0]	**Data Strobes:** SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS#[7:0] during read and write transactions.	I/O DDR3
SB_DQS#[8]	**ECC Data Strobe Complement**: SB_DQS#[8] is the complement strobe for the ECC check data bits SB_DQ[71:64] **Note**: Not required for non-ECC mode	I/O DDR3
SB_DQS#[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O DDR3
SB_DQ[71:64]	**ECC Check Data Bits:** SB_DQ[71:64] are the ECC check data bits for Channel B **Note**: Not required for non-ECC mode	I/O DDR3
SB_DQ[63:0]	**Data Bus:** Channel B data signal interface to the SDRAM data bus.	I/O DDR3
SB_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SB_CK[1:0]	**SDRAM Differential Clock:** Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CK and the negative edge of its complement SB_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SB_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel B SDRAM Differential clock signal-pair complement.	O DDR3
SB_CKE[1:0]	**Clock Enable:** (1 per rank) Used to: - Initialize the SDRAMs during power-up. - Power-down SDRAM ranks. - Place all SDRAM ranks into and out of self-refresh during STR.	O DDR3
SB_CS#[1:0]	**Chip Select:** (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3

Table 8. Memory Channel B (Sheet 2 of 2)

Signal Name	Description	Direction / Buffer Type
SB_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3

3.2 Reset and Miscellaneous Signals

Table 9. Reset and Miscellaneous Signals

Signal Name	Description	Direction / Buffer Type
SM_DRAMRST#	**DDR3 DRAM Reset:** Reset signal from processor to DRAM devices. One for all channels of DIMMs.	O DDR3
CFG[17:0]	**Configuration signals:** The CFG signals have a default value of 1 if not terminated on the board. Refer to the Platform Design Guide for pull-down recommendations when logic low is desired. • **CFG[0]:** PCI Express* Bifurcation: — 1 = 1 x16 PCI Express I/O — 0 = 2 x 8 PCI Express I/O • **CFG[1]:** Reserved • **CFG[2]:** Reserved configuration lands. A test point may be placed on the board for this land. • **CFG[3]:** PCI Express* Static Lane Numbering Reversal. A test point may be placed on the board for this land. Lane reversal will be applied across all 16 lanes. — 1: No Reversal — 0: Reversal In the case of Bifurcation with NO Lane Reversal the physical lane mapping is as follows: — Lanes 15:8 => Port 1 Lanes 7:0 — Lanes 7:0 => Port 0 Lanes 7:0 In the case of Bifurcation with WITH Lane Reversal the physical lane mapping is as follows: — Lanes 15:8 => Port 0 Lanes 0:7 — Lanes 7:0 => Port 1 Lanes 0:7 • **CFG[4]:** Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort. — 1: No Physical Display Port attached to the Embedded Display Port — 0: An external Display Port device is connected to the Embedded Display Port • **CFG[17:5]:** Reserved configuration lands. Intel does not recommend a test point on the board for these lands.	I CMOS

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4 Electrical Specifications

4.1 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Table 10. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR3 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

Table 10. Mobile Signal Groups[1]

Signal Group	Alpha Group	Type	Signals
DDR3 Data Signals[2]			
Single ended	(e)	DDR3 Bi-directional	SA_DQ[71:0], SB_DQ[71:0]
Differential	(f)	DDR3 Bi-directional	SA_DQS[8:0], SA_DQS#[8:0] SB_DQS[8:0], SB_DQS#[8:0]
Power/Ground/Other			
Single Ended	(z)	Other	DBR#, PROC_DETECT, VCAP0, VCAP1, VCAP2

NOTES:
1. Refer to Chapter 3 for signal description details.
2. SA and SB refer to DDR3 Channel A and DDR3 Channel B.

All Control Sideband Asynchronous signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 4.2 for the DC specifications.

4.2 DC Specifications

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise. See Chapter 5 for the processor pin listings and Chapter 3 for signal definitions.

The DC specifications for the DDR3 signals are listed in Table 11.

4.2.1 Voltage and Current Specifications

Table 11. DDR3 Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Alpha Group	Min	Typ	Max	Units	Notes[1,9]
V_{IL}	Input Low Voltage	(e,f)			$0.43*V_{DDQ}$	V	2,4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. R_{VTT_TERM} is the termination on the DIMM and in not controlled by the processor.

Table 11. DDR3 Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Alpha Group	Min	Typ	Max	Units	Notes[1,9]
V_{IH}	Input High Voltage	(e,f)	$0.57*V_{DDQ}$			V	3
V_{OL}	Output Low Voltage	(c,d,e,f)		$(V_{DDQ} / 2)* (R_{ON} / (R_{ON}+R_{VTT\_TERM}))$			5
V_{OH}	Output High Voltage	(c,d,e,f)		$V_{DDQ} - ((V_{DDQ} / 2)* (R_{ON}/ (R_{ON}+R_{VTT\_TERM}))$		V	4,5

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. R_{VTT_TERM} is the termination on the DIMM and in not controlled by the processor.

5 Processor Ball and Signal Information

5.1 Processor Ball Assignments

- Table 12 provides a listing of all processor pins ordered alphabetically by ball name for the Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series package respectively.
- Table 13 provides a listing of all processor pins ordered alphabetically by ball number for the Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series package respectively.
- Figure 5, Figure 6, Figure 7, and Figure 8 show the Top-Down view of the Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series ballmap

Figure 5. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ballmap (Top View, Upper-Left Quadrant)

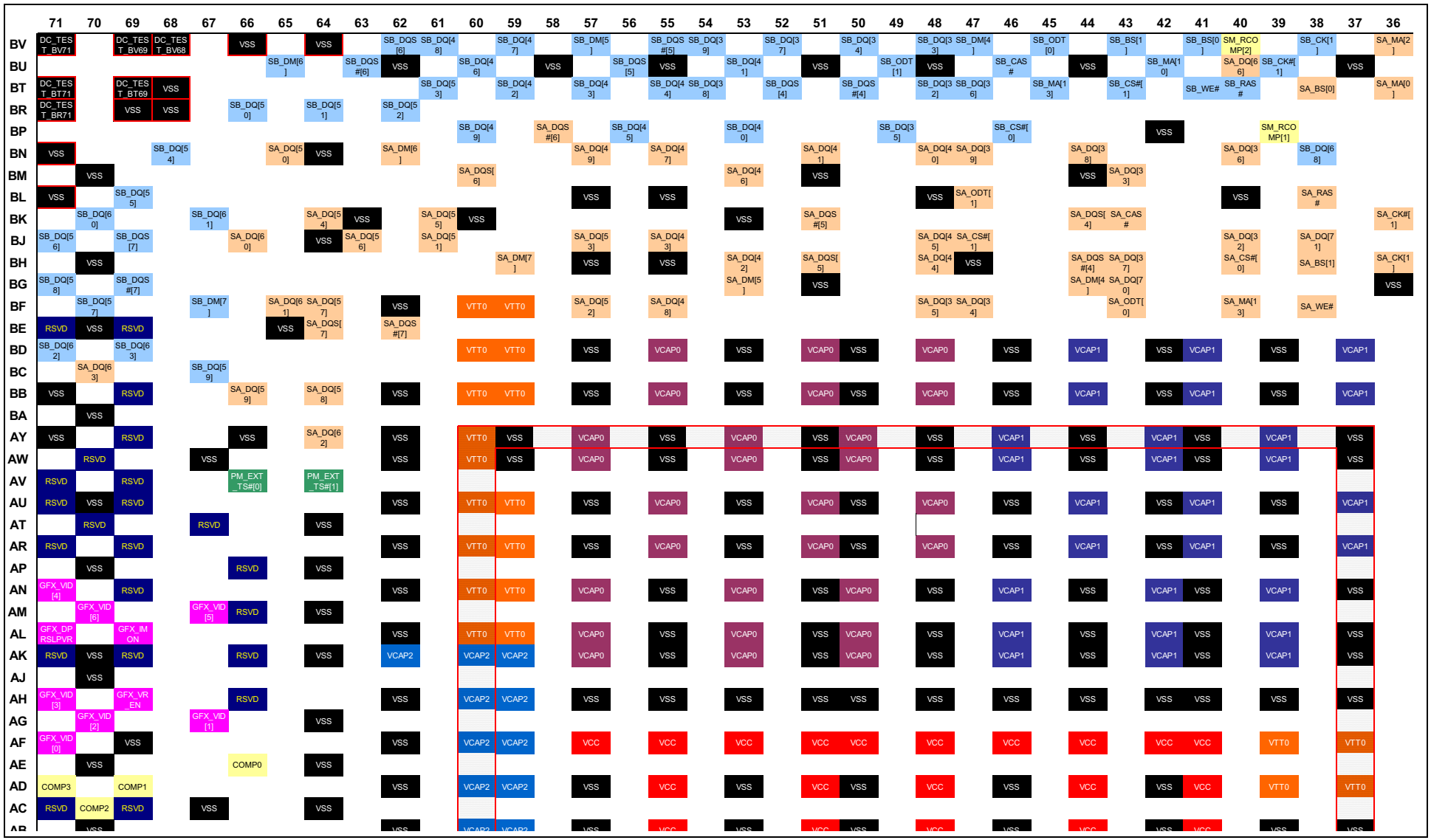


Figure 6. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ballmap (Top View, Upper-Right Quadrant)

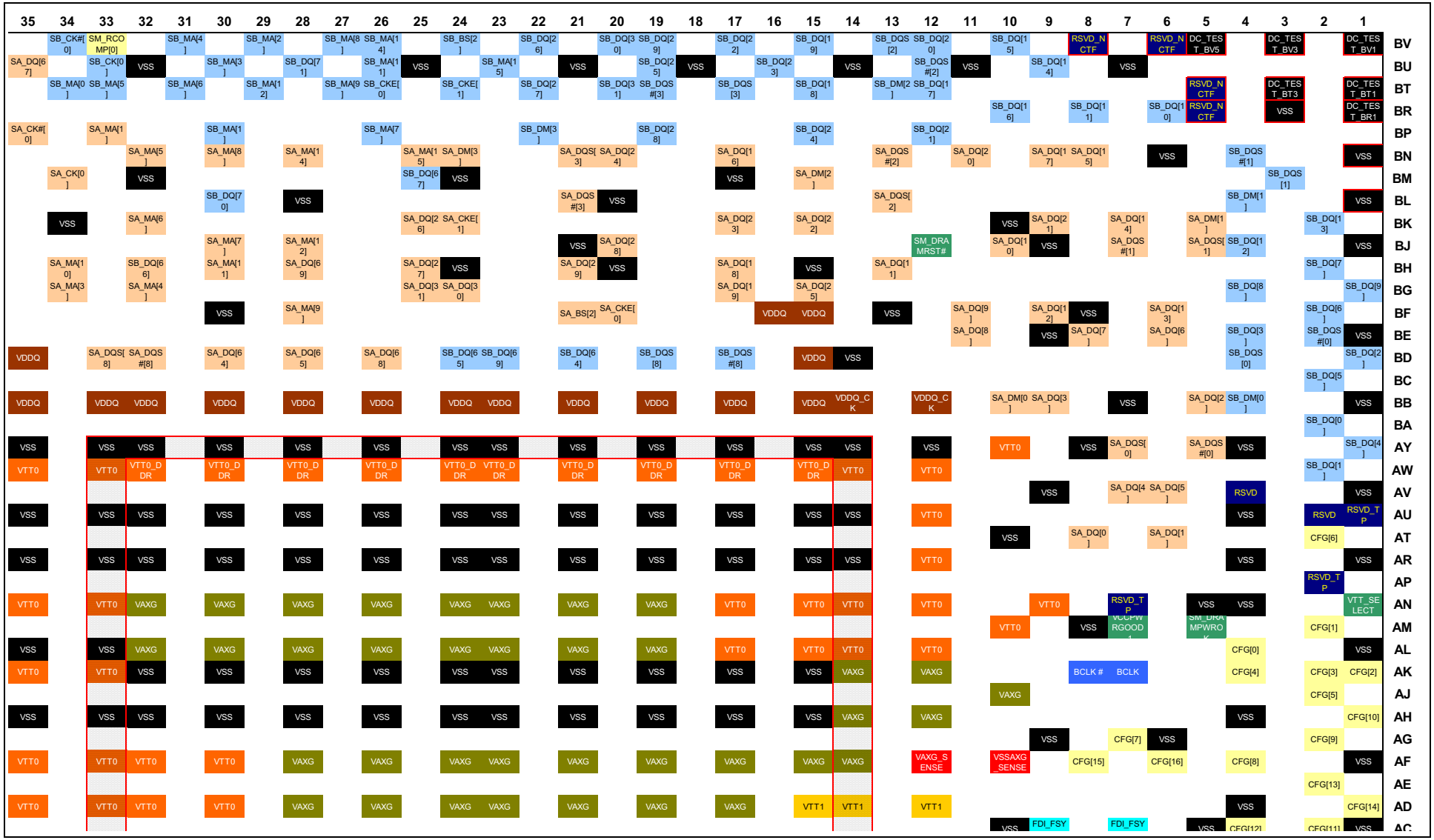


Figure 7. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ballmap (Top View, Lower-Left Quadrant)

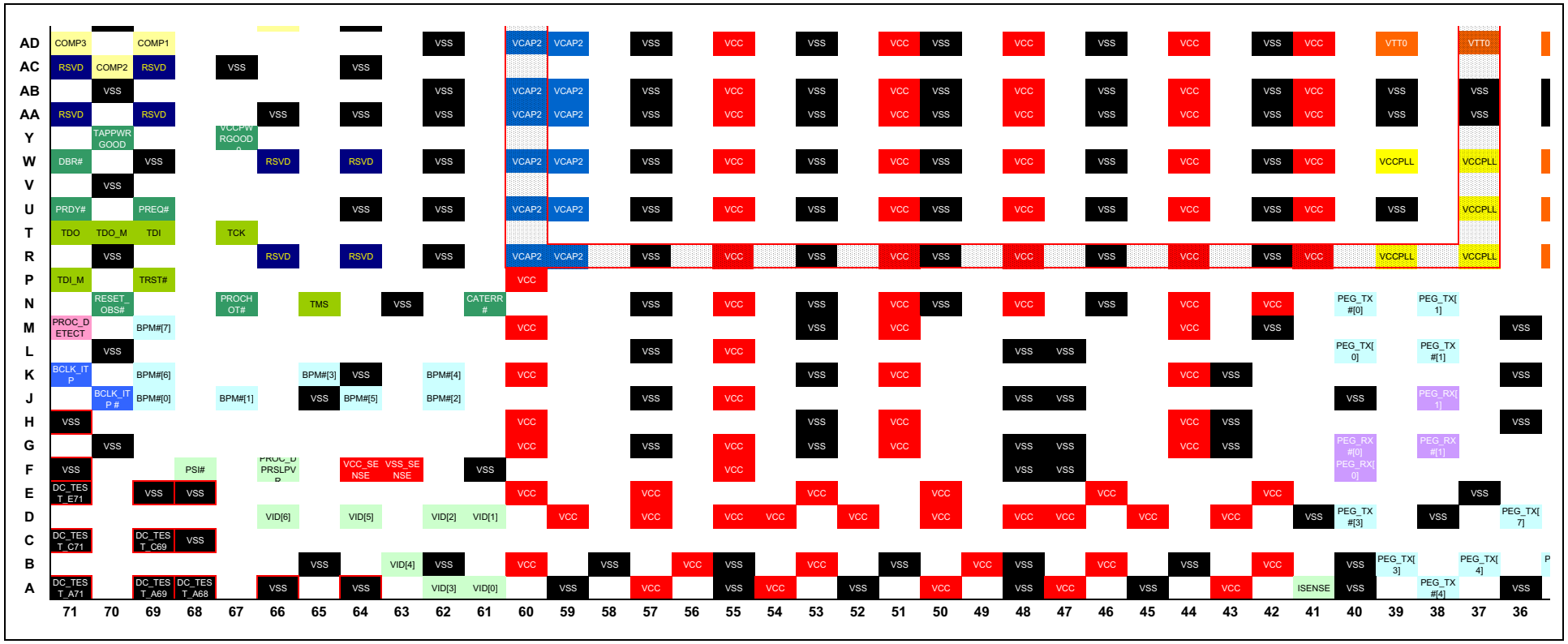
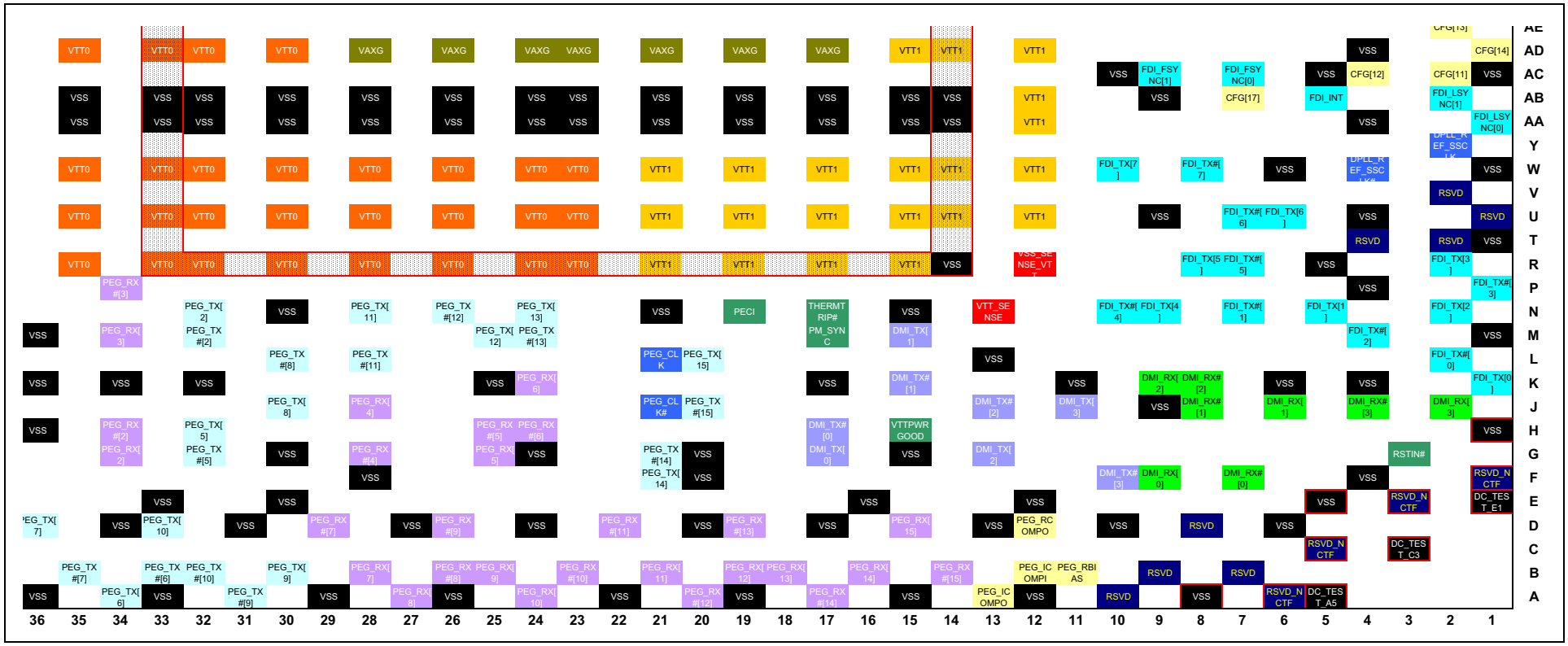


Figure 8. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ballmap (Top View, Lower-Right Quadrant)



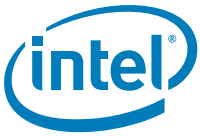


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
BCLK	AK7	DIFF CLK	I
BCLK #	AK8	DIFF CLK	I
BCLK_ITP	K71	DIFF CLK	O
BCLK_ITP #	J70	DIFF CLK	O
BPM#[0]	J69	GTL	I/O
BPM#[1]	J67	GTL	I/O
BPM#[2]	J62	GTL	I/O
BPM#[3]	K65	GTL	I/O
BPM#[4]	K62	GTL	I/O
BPM#[5]	J64	GTL	I/O
BPM#[6]	K69	GTL	I/O
BPM#[7]	M69	GTL	I/O
CATERR#	N61	GTL	I/O
CFG[0]	AL4	CMOS	I
CFG[1]	AM2	CMOS	I
CFG[2]	AK1	CMOS	I
CFG[3]	AK2	CMOS	I
CFG[4]	AK4	CMOS	I
CFG[5]	AJ2	CMOS	I
CFG[6]	AT2	CMOS	I
CFG[7]	AG7	CMOS	I
CFG[8]	AF4	CMOS	I
CFG[9]	AG2	CMOS	I
CFG[10]	AH1	CMOS	I
CFG[11]	AC2	CMOS	I
CFG[12]	AC4	CMOS	I
CFG[13]	AE2	CMOS	I
CFG[14]	AD1	CMOS	I
CFG[15]	AF8	CMOS	I
CFG[16]	AF6	CMOS	I
CFG[17]	AB7	CMOS	I
COMP0	AE66	Analog	I
COMP1	AD69	Analog	I
COMP2	AC70	Analog	I
COMP3	AD71	Analog	I
DBR#	W71		O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
DC_TEST_A5	A5		
DC_TEST_A68	A68		
DC_TEST_A69	A69		
DC_TEST_A71	A71		
DC_TEST_BR1	BR1		
DC_TEST_BR71	BR71		
DC_TEST_BT1	BT1		
DC_TEST_BT3	BT3		
DC_TEST_BT69	BT69		
DC_TEST_BT71	BT71		
DC_TEST_BV1	BV1		
DC_TEST_BV3	BV3		
DC_TEST_BV5	BV5		
DC_TEST_BV68	BV68		
DC_TEST_BV69	BV69		
DC_TEST_BV71	BV71		
DC_TEST_C3	C3		
DC_TEST_C69	C69		
DC_TEST_C71	C71		
DC_TEST_E1	E1		
DC_TEST_E71	E71		
DMI_RX[0]	F9	DMI	I
DMI_RX[1]	J6	DMI	I
DMI_RX[2]	K9	DMI	I
DMI_RX[3]	J2	DMI	I
DMI_RX#[0]	F7	DMI	I
DMI_RX#[1]	J8	DMI	I
DMI_RX#[2]	K8	DMI	I
DMI_RX#[3]	J4	DMI	I
DMI_TX[0]	G17	DMI	O
DMI_TX[1]	M15	DMI	O
DMI_TX[2]	G13	DMI	O
DMI_TX[3]	J11	DMI	O
DMI_TX#[0]	H17	DMI	O
DMI_TX#[1]	K15	DMI	O
DMI_TX#[2]	J13	DMI	O
DMI_TX#[3]	F10	DMI	O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
DPLL_REF_SSCLK	Y2	DIFF CLK	I
DPLL_REF_SSCLK #	W4	DIFF CLK	I
FDI_FSYNC[0]	AC7	CMOS	I
FDI_FSYNC[1]	AC9	CMOS	I
FDI_INT	AB5	CMOS	I
FDI_LSYNC[0]	AA1	CMOS	I
FDI_LSYNC[1]	AB2	CMOS	I
FDI_TX[0]	K1	FDI	O
FDI_TX[1]	N5	FDI	O
FDI_TX[2]	N2	FDI	O
FDI_TX[3]	R2	FDI	O
FDI_TX[4]	N9	FDI	O
FDI_TX[5]	R8	FDI	O
FDI_TX[6]	U6	FDI	O
FDI_TX[7]	W10	FDI	O
FDI_TX#[0]	L2	FDI	O
FDI_TX#[1]	N7	FDI	O
FDI_TX#[2]	M4	FDI	O
FDI_TX#[3]	P1	FDI	O
FDI_TX#[4]	N10	FDI	O
FDI_TX#[5]	R7	FDI	O
FDI_TX#[6]	U7	FDI	O
FDI_TX#[7]	W8	FDI	O
GFX_DPRSLPVR	AL71	CMOS	O
GFX_IMON	AL69	CMOS	I
GFX_VID[0]	AF71	CMOS	O
GFX_VID[1]	AG67	CMOS	O
GFX_VID[2]	AG70	CMOS	O
GFX_VID[3]	AH71	CMOS	O
GFX_VID[4]	AN71	CMOS	O
GFX_VID[5]	AM67	CMOS	O
GFX_VID[6]	AM70	CMOS	O
GFX_VR_EN	AH69	CMOS	O
ISENSE	A41	Analog	I
PECI	N19	Async	I/O
PEG_CLK	L21	Diff CLK	I

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
PEG_CLK#	J21	DIFF CLK	I
PEG_ICOMPI	B12	Analog	I
PEG_ICOMPO	A13	Analog	I
PEG_RBIAS	B11	Analog	I
PEG_RCOMPO	D12	Analog	I
PEG_RX[0]	F40	PCIe	I
PEG_RX[1]	J38	PCIe	I
PEG_RX[2]	G34	PCIe	I
PEG_RX[3]	M34	PCIe	I
PEG_RX[4]	J28	PCIe	I
PEG_RX[5]	G25	PCIe	I
PEG_RX[6]	K24	PCIe	I
PEG_RX[7]	B28	PCIe	I
PEG_RX[8]	A27	PCIe	I
PEG_RX[9]	B25	PCIe	I
PEG_RX[10]	A24	PCIe	I
PEG_RX[11]	B21	PCIe	I
PEG_RX[12]	B19	PCIe	I
PEG_RX[13]	B18	PCIe	I
PEG_RX[14]	B16	PCIe	I
PEG_RX[15]	D15	PCIe	I
PEG_RX#[0]	G40	PCIe	I
PEG_RX#[1]	G38	PCIe	I
PEG_RX#[2]	H34	PCIe	I
PEG_RX#[3]	P34	PCIe	I
PEG_RX#[4]	G28	PCIe	I
PEG_RX#[5]	H25	PCIe	I
PEG_RX#[6]	H24	PCIe	I
PEG_RX#[7]	D29	PCIe	I
PEG_RX#[8]	B26	PCIe	I
PEG_RX#[9]	D26	PCIe	I
PEG_RX#[10]	B23	PCIe	I
PEG_RX#[11]	D22	PCIe	I
PEG_RX#[12]	A20	PCIe	I
PEG_RX#[13]	D19	PCIe	I
PEG_RX#[14]	A17	PCIe	I
PEG_RX#[15]	B14	PCIe	I

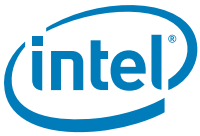


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
PEG_TX[0]	L40	PCIe	O
PEG_TX[1]	N38	PCIe	O
PEG_TX[2]	N32	PCIe	O
PEG_TX[3]	B39	PCIe	O
PEG_TX[4]	B37	PCIe	O
PEG_TX[5]	H32	PCIe	O
PEG_TX[6]	A34	PCIe	O
PEG_TX[7]	D36	PCIe	O
PEG_TX[8]	J30	PCIe	O
PEG_TX[9]	B30	PCIe	O
PEG_TX[10]	D33	PCIe	O
PEG_TX[11]	N28	PCIe	O
PEG_TX[12]	M25	PCIe	O
PEG_TX[13]	N24	PCIe	O
PEG_TX[14]	F21	PCIe	O
PEG_TX[15]	L20	PCIe	O
PEG_TX#[0]	N40	PCIe	O
PEG_TX#[1]	L38	PCIe	O
PEG_TX#[2]	M32	PCIe	O
PEG_TX#[3]	D40	PCIe	O
PEG_TX#[4]	A38	PCIe	O
PEG_TX#[5]	G32	PCIe	O
PEG_TX#[6]	B33	PCIe	O
PEG_TX#[7]	B35	PCIe	O
PEG_TX#[8]	L30	PCIe	O
PEG_TX#[9]	A31	PCIe	O
PEG_TX#[10]	B32	PCIe	O
PEG_TX#[11]	L28	PCIe	O
PEG_TX#[12]	N26	PCIe	O
PEG_TX#[13]	M24	PCIe	O
PEG_TX#[14]	G21	PCIe	O
PEG_TX#[15]	J20	PCIe	O
PM_EXT_TS#[0]	AV66	CMOS	I
PM_EXT_TS#[1]	AV64	CMOS	I
PM_SYNC	M17	CMOS	I
PRDY#	U71	Async GTL	O
PREQ#	U69	Async GTL	I

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
PROC_DETECT	M71		
PROC_DPRSLPVR	F66	CMOS	O
PROCHOT#	N67	Async GTL	I/O
PSI#	F68	Async CMOS	O
RESET_OBS#	N70	Async CMOS	O
RSTIN#	G3	CMOS	I
RSVD	BE71		
RSVD	BE69		
RSVD	BB69		
RSVD	AY69		
RSVD	AW70		
RSVD	A10		
RSVD	AA69		
RSVD	AA71		
RSVD	AC69		
RSVD	AC71		
RSVD	AH66		
RSVD	AK66		
RSVD	AK69		
RSVD	AK71		
RSVD	AM66		
RSVD	AN69		
RSVD	AP66		
RSVD	AR69		
RSVD	AR71		
RSVD	AT67		
RSVD	AT70		
RSVD	AU2		
RSVD	AU69		
RSVD	AU71		
RSVD	AV4		
RSVD	AV69		
RSVD	AV71		
RSVD	B7		
RSVD	B9		
RSVD	D8		

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
RSVD	R64		
RSVD	R66		
RSVD	T2		
RSVD	T4		
RSVD	U1		
RSVD	V2		
RSVD	W64		
RSVD	W66		
RSVD_NCTF	A6		
RSVD_NCTF	BR5		
RSVD_NCTF	BT5		
RSVD_NCTF	BV6		
RSVD_NCTF	BV8		
RSVD_NCTF	C5		
RSVD_NCTF	E3		
RSVD_NCTF	F1		
RSVD_TP	AN7		
RSVD_TP	AP2		
RSVD_TP	AU1		
SA_BS[0]	BT38	DDR3	O
SA_BS[1]	BH38	DDR3	O
SA_BS[2]	BF21	DDR3	O
SA_CAS#	BK43	DDR3	O
SA_CK[0]	BM34	DDR3	O
SA_CK[1]	BH36	DDR3	O
SA_CK#[0]	BP35	DDR3	O
SA_CK#[1]	BK36	DDR3	O
SA_CKE[0]	BF20	DDR3	O
SA_CKE[1]	BK24	DDR3	O
SA_CS#[0]	BH40	DDR3	O
SA_CS#[1]	BJ47	DDR3	O
SA_DM[0]	BB10	DDR3	O
SA_DM[1]	BK5	DDR3	O
SA_DM[2]	BM15	DDR3	O
SA_DM[3]	BN24	DDR3	O
SA_DM[4]	BG44	DDR3	O
SA_DM[5]	BG53	DDR3	O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_DM[6]	BN62	DDR3	O
SA_DM[7]	BH59	DDR3	O
SA_DQ[0]	AT8	DDR3	I/O
SA_DQ[1]	AT6	DDR3	I/O
SA_DQ[2]	BB5	DDR3	I/O
SA_DQ[3]	BB9	DDR3	I/O
SA_DQ[4]	AV7	DDR3	I/O
SA_DQ[5]	AV6	DDR3	I/O
SA_DQ[6]	BE6	DDR3	I/O
SA_DQ[7]	BE8	DDR3	I/O
SA_DQ[8]	BE11	DDR3	I/O
SA_DQ[9]	BF11	DDR3	I/O
SA_DQ[10]	BJ10	DDR3	I/O
SA_DQ[11]	BH13	DDR3	I/O
SA_DQ[12]	BF9	DDR3	I/O
SA_DQ[13]	BF6	DDR3	I/O
SA_DQ[14]	BK7	DDR3	I/O
SA_DQ[15]	BN8	DDR3	I/O
SA_DQ[16]	BN17	DDR3	I/O
SA_DQ[17]	BN9	DDR3	I/O
SA_DQ[18]	BH17	DDR3	I/O
SA_DQ[19]	BG17	DDR3	I/O
SA_DQ[20]	BN11	DDR3	I/O
SA_DQ[21]	BK9	DDR3	I/O
SA_DQ[22]	BK15	DDR3	I/O
SA_DQ[23]	BK17	DDR3	I/O
SA_DQ[24]	BN20	DDR3	I/O
SA_DQ[25]	BG15	DDR3	I/O
SA_DQ[26]	BK25	DDR3	I/O
SA_DQ[27]	BH25	DDR3	I/O
SA_DQ[28]	BJ20	DDR3	I/O
SA_DQ[29]	BH21	DDR3	I/O
SA_DQ[30]	BG24	DDR3	I/O
SA_DQ[31]	BG25	DDR3	I/O
SA_DQ[32]	BJ40	DDR3	I/O
SA_DQ[33]	BM43	DDR3	I/O
SA_DQ[34]	BF47	DDR3	I/O

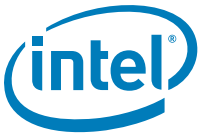


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_DQ[35]	BF48	DDR3	I/O
SA_DQ[36]	BN40	DDR3	I/O
SA_DQ[37]	BH43	DDR3	I/O
SA_DQ[38]	BN44	DDR3	I/O
SA_DQ[39]	BN47	DDR3	I/O
SA_DQ[40]	BN48	DDR3	I/O
SA_DQ[41]	BN51	DDR3	I/O
SA_DQ[42]	BH53	DDR3	I/O
SA_DQ[43]	BJ55	DDR3	I/O
SA_DQ[44]	BH48	DDR3	I/O
SA_DQ[45]	BJ48	DDR3	I/O
SA_DQ[46]	BM53	DDR3	I/O
SA_DQ[47]	BN55	DDR3	I/O
SA_DQ[48]	BF55	DDR3	I/O
SA_DQ[49]	BN57	DDR3	I/O
SA_DQ[50]	BN65	DDR3	I/O
SA_DQ[51]	BJ61	DDR3	I/O
SA_DQ[52]	BF57	DDR3	I/O
SA_DQ[53]	BJ57	DDR3	I/O
SA_DQ[54]	BK64	DDR3	I/O
SA_DQ[55]	BK61	DDR3	I/O
SA_DQ[56]	BJ63	DDR3	I/O
SA_DQ[57]	BF64	DDR3	I/O
SA_DQ[58]	BB64	DDR3	I/O
SA_DQ[59]	BB66	DDR3	I/O
SA_DQ[60]	BJ66	DDR3	I/O
SA_DQ[61]	BF65	DDR3	I/O
SA_DQ[62]	AY64	DDR3	I/O
SA_DQ[63]	BC70	DDR3	I/O
SA_DQ[64]	BD30	DDR3	I/O
SA_DQ[65]	BD28	DDR3	I/O
SA_DQ[66]	BU40	DDR3	I/O
SA_DQ[67]	BU35	DDR3	I/O
SA_DQ[68]	BD26	DDR3	I/O
SA_DQ[69]	BH28	DDR3	I/O
SA_DQ[70]	BG43	DDR3	I/O
SA_DQ[71]	BJ38	DDR3	I/O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_DQS[0]	AY7	DDR3	I/O
SA_DQS[1]	BJ5	DDR3	I/O
SA_DQS[2]	BL13	DDR3	I/O
SA_DQS[3]	BN21	DDR3	I/O
SA_DQS[4]	BK44	DDR3	I/O
SA_DQS[5]	BH51	DDR3	I/O
SA_DQS[6]	BM60	DDR3	I/O
SA_DQS[7]	BE64	DDR3	I/O
SA_DQS[8]	BD33	DDR3	I/O
SA_DQS#[0]	AY5	DDR3	I/O
SA_DQS#[1]	BJ7	DDR3	I/O
SA_DQS#[2]	BN13	DDR3	I/O
SA_DQS#[3]	BL21	DDR3	I/O
SA_DQS#[4]	BH44	DDR3	I/O
SA_DQS#[5]	BK51	DDR3	I/O
SA_DQS#[6]	BP58	DDR3	I/O
SA_DQS#[7]	BE62	DDR3	I/O
SA_DQS#[8]	BD32	DDR3	I/O
SA_MA[0]	BT36	DDR3	O
SA_MA[1]	BP33	DDR3	O
SA_MA[2]	BV36	DDR3	O
SA_MA[3]	BG34	DDR3	O
SA_MA[4]	BG32	DDR3	O
SA_MA[5]	BN32	DDR3	O
SA_MA[6]	BK32	DDR3	O
SA_MA[7]	BJ30	DDR3	O
SA_MA[8]	BN30	DDR3	O
SA_MA[9]	BF28	DDR3	O
SA_MA[10]	BH34	DDR3	O
SA_MA[11]	BH30	DDR3	O
SA_MA[12]	BJ28	DDR3	O
SA_MA[13]	BF40	DDR3	O
SA_MA[14]	BN28	DDR3	O
SA_MA[15]	BN25	DDR3	O
SA_ODT[0]	BF43	DDR3	O
SA_ODT[1]	BL47	DDR3	O
SA_RAS#	BL38	DDR3	O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_WE#	BF38	DDR3	O
SB_BS[0]	BV41	DDR3	O
SB_BS[1]	BV43	DDR3	O
SB_BS[2]	BV24	DDR3	O
SB_CAS#	BU46	DDR3	O
SB_CK[0]	BU33	DDR3	O
SB_CK[1]	BV38	DDR3	O
SB_CK#[0]	BV34	DDR3	O
SB_CK#[1]	BU39	DDR3	O
SB_CKE[0]	BT26	DDR3	O
SB_CKE[1]	BT24	DDR3	O
SB_CS#[0]	BP46	DDR3	O
SB_CS#[1]	BT43	DDR3	O
SB_DM[0]	BB4	DDR3	O
SB_DM[1]	BL4	DDR3	O
SB_DM[2]	BT13	DDR3	O
SB_DM[3]	BP22	DDR3	O
SB_DM[4]	BV47	DDR3	O
SB_DM[5]	BV57	DDR3	O
SB_DM[6]	BU65	DDR3	O
SB_DM[7]	BF67	DDR3	O
SB_DQ[0]	BA2	DDR3	I/O
SB_DQ[1]	AW2	DDR3	I/O
SB_DQ[2]	BD1	DDR3	I/O
SB_DQ[3]	BE4	DDR3	I/O
SB_DQ[4]	AY1	DDR3	I/O
SB_DQ[5]	BC2	DDR3	I/O
SB_DQ[6]	BF2	DDR3	I/O
SB_DQ[7]	BH2	DDR3	I/O
SB_DQ[8]	BG4	DDR3	I/O
SB_DQ[9]	BG1	DDR3	I/O
SB_DQ[10]	BR6	DDR3	I/O
SB_DQ[11]	BR8	DDR3	I/O
SB_DQ[12]	BJ4	DDR3	I/O
SB_DQ[13]	BK2	DDR3	I/O
SB_DQ[14]	BU9	DDR3	I/O
SB_DQ[15]	BV10	DDR3	I/O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_DQ[16]	BR10	DDR3	I/O
SB_DQ[17]	BT12	DDR3	I/O
SB_DQ[18]	BT15	DDR3	I/O
SB_DQ[19]	BV15	DDR3	I/O
SB_DQ[20]	BV12	DDR3	I/O
SB_DQ[21]	BP12	DDR3	I/O
SB_DQ[22]	BV17	DDR3	I/O
SB_DQ[23]	BU16	DDR3	I/O
SB_DQ[24]	BP15	DDR3	I/O
SB_DQ[25]	BU19	DDR3	I/O
SB_DQ[26]	BV22	DDR3	I/O
SB_DQ[27]	BT22	DDR3	I/O
SB_DQ[28]	BP19	DDR3	I/O
SB_DQ[29]	BV19	DDR3	I/O
SB_DQ[30]	BV20	DDR3	I/O
SB_DQ[31]	BT20	DDR3	I/O
SB_DQ[32]	BT48	DDR3	I/O
SB_DQ[33]	BV48	DDR3	I/O
SB_DQ[34]	BV50	DDR3	I/O
SB_DQ[35]	BP49	DDR3	I/O
SB_DQ[36]	BT47	DDR3	I/O
SB_DQ[37]	BV52	DDR3	I/O
SB_DQ[38]	BT54	DDR3	I/O
SB_DQ[39]	BV54	DDR3	I/O
SB_DQ[40]	BP53	DDR3	I/O
SB_DQ[41]	BU53	DDR3	I/O
SB_DQ[42]	BT59	DDR3	I/O
SB_DQ[43]	BT57	DDR3	I/O
SB_DQ[44]	BT55	DDR3	I/O
SB_DQ[45]	BP56	DDR3	I/O
SB_DQ[46]	BU60	DDR3	I/O
SB_DQ[47]	BV59	DDR3	I/O
SB_DQ[48]	BV61	DDR3	I/O
SB_DQ[49]	BP60	DDR3	I/O
SB_DQ[50]	BR66	DDR3	I/O
SB_DQ[51]	BR64	DDR3	I/O
SB_DQ[52]	BR62	DDR3	I/O

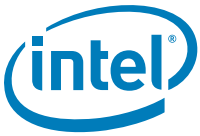


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_DQ[53]	BT61	DDR3	I/O
SB_DQ[54]	BN68	DDR3	I/O
SB_DQ[55]	BL69	DDR3	I/O
SB_DQ[56]	BJ71	DDR3	I/O
SB_DQ[57]	BF70	DDR3	I/O
SB_DQ[58]	BG71	DDR3	I/O
SB_DQ[59]	BC67	DDR3	I/O
SB_DQ[60]	BK70	DDR3	I/O
SB_DQ[61]	BK67	DDR3	I/O
SB_DQ[62]	BD71	DDR3	I/O
SB_DQ[63]	BD69	DDR3	I/O
SB_DQ[64]	BD21	DDR3	I/O
SB_DQ[65]	BD24	DDR3	I/O
SB_DQ[66]	BH32	DDR3	I/O
SB_DQ[67]	BM25	DDR3	I/O
SB_DQ[68]	BN38	DDR3	I/O
SB_DQ[69]	BD23	DDR3	I/O
SB_DQ[70]	BL30	DDR3	I/O
SB_DQ[71]	BU28	DDR3	I/O
SB_DQS[0]	BD4	DDR3	I/O
SB_DQS[1]	BM3	DDR3	I/O
SB_DQS[2]	BV13	DDR3	I/O
SB_DQS[3]	BT17	DDR3	I/O
SB_DQS[4]	BT52	DDR3	I/O
SB_DQS[5]	BU56	DDR3	I/O
SB_DQS[6]	BV62	DDR3	I/O
SB_DQS[7]	BJ69	DDR3	I/O
SB_DQS[8]	BD19	DDR3	I/O
SB_DQS#[0]	BE2	DDR3	I/O
SB_DQS#[1]	BN4	DDR3	I/O
SB_DQS#[2]	BU12	DDR3	I/O
SB_DQS#[3]	BT19	DDR3	I/O
SB_DQS#[4]	BT50	DDR3	I/O
SB_DQS#[5]	BV55	DDR3	I/O
SB_DQS#[6]	BU63	DDR3	I/O
SB_DQS#[7]	BG69	DDR3	I/O
SB_DQS#[8]	BD17	DDR3	I/O

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_MA[0]	BT34	DDR3	O
SB_MA[1]	BP30	DDR3	O
SB_MA[2]	BV29	DDR3	O
SB_MA[3]	BU30	DDR3	O
SB_MA[4]	BV31	DDR3	O
SB_MA[5]	BT33	DDR3	O
SB_MA[6]	BT31	DDR3	O
SB_MA[7]	BP26	DDR3	O
SB_MA[8]	BV27	DDR3	O
SB_MA[9]	BT27	DDR3	O
SB_MA[10]	BU42	DDR3	O
SB_MA[11]	BU26	DDR3	O
SB_MA[12]	BT29	DDR3	O
SB_MA[13]	BT45	DDR3	O
SB_MA[14]	BV26	DDR3	O
SB_MA[15]	BU23	DDR3	O
SB_ODT[0]	BV45	DDR3	O
SB_ODT[1]	BU49	DDR3	O
SB_RAS#	BT40	DDR3	O
SB_WE#	BT41	DDR3	O
SM_DRAMPWROK	AM5	Async CMOS	I
SM_DRAMRST#	BJ12	DDR3	O
SM_RCOMP[0]	BV33	Analog	I
SM_RCOMP[1]	BP39	Analog	
SM_RCOMP[2]	BV40	Analog	I
TAPPWRGOOD	Y70	Async CMOS	O
TCK	T67	CMOS	I
TDI	T69	CMOS	I
TDI_M	P71	CMOS	I
TDO	T71	CMOS	O
TDO_M	T70	CMOS	O
THERMTRIP#	N17	Async GTL	O
TMS	N65	CMOS	I
TRST#	P69	CMOS	I
VAXG	AD17	REF	
VAXG	AD19	REF	
VAXG	AD21	REF	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VAXG	AD23	REF	
VAXG	AD24	REF	
VAXG	AD26	REF	
VAXG	AD28	REF	
VAXG	AF14	REF	
VAXG	AF15	REF	
VAXG	AF17	REF	
VAXG	AF19	REF	
VAXG	AF21	REF	
VAXG	AF23	REF	
VAXG	AF24	REF	
VAXG	AF26	REF	
VAXG	AF28	REF	
VAXG	AH12	REF	
VAXG	AH14	REF	
VAXG	AJ10	REF	
VAXG	AK12	REF	
VAXG	AK14	REF	
VAXG	AL19	REF	
VAXG	AL21	REF	
VAXG	AL23	REF	
VAXG	AL24	REF	
VAXG	AL26	REF	
VAXG	AL28	REF	
VAXG	AL30	REF	
VAXG	AL32	REF	
VAXG	AN19	REF	
VAXG	AN21	REF	
VAXG	AN23	REF	
VAXG	AN24	REF	
VAXG	AN26	REF	
VAXG	AN28	REF	
VAXG	AN30	REF	
VAXG	AN32	REF	
VAXG_SENSE	AF12	Analog	O
VCAP0	AK50	PWR	
VCAP0	AK53	PWR	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCAP0	AK57	PWR	
VCAP0	AL50	PWR	
VCAP0	AL53	PWR	
VCAP0	AL57	PWR	
VCAP0	AN50	PWR	
VCAP0	AN53	PWR	
VCAP0	AN57	PWR	
VCAP0	AR48	PWR	
VCAP0	AR51	PWR	
VCAP0	AR55	PWR	
VCAP0	AU48	PWR	
VCAP0	AU51	PWR	
VCAP0	AU55	PWR	
VCAP0	AW50	PWR	
VCAP0	AW53	PWR	
VCAP0	AW57	PWR	
VCAP0	AY50	PWR	
VCAP0	AY53	PWR	
VCAP0	AY57	PWR	
VCAP0	BB48	PWR	
VCAP0	BB51	PWR	
VCAP0	BB55	PWR	
VCAP0	BD48	PWR	
VCAP0	BD51	PWR	
VCAP0	BD55	PWR	
VCAP1	AK39	PWR	
VCAP1	AK42	PWR	
VCAP1	AK46	PWR	
VCAP1	AL39	PWR	
VCAP1	AL42	PWR	
VCAP1	AL46	PWR	
VCAP1	AN39	PWR	
VCAP1	AN42	PWR	
VCAP1	AN46	PWR	
VCAP1	AR37	PWR	
VCAP1	AR41	PWR	
VCAP1	AR44	PWR	

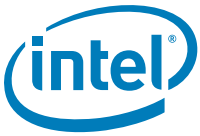


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCAP1	AU37	PWR	
VCAP1	AU41	PWR	
VCAP1	AU44	PWR	
VCAP1	AW39	PWR	
VCAP1	AW42	PWR	
VCAP1	AW46	PWR	
VCAP1	AY39	PWR	
VCAP1	AY42	PWR	
VCAP1	AY46	PWR	
VCAP1	BB37	PWR	
VCAP1	BB41	PWR	
VCAP1	BB44	PWR	
VCAP1	BD37	PWR	
VCAP1	BD41	PWR	
VCAP1	BD44	PWR	
VCAP2	AA59	PWR	
VCAP2	AA60	PWR	
VCAP2	AB59	PWR	
VCAP2	AB60	PWR	
VCAP2	AD59	PWR	
VCAP2	AD60	PWR	
VCAP2	AF59	PWR	
VCAP2	AF60	PWR	
VCAP2	AH59	PWR	
VCAP2	AH60	PWR	
VCAP2	AK59	PWR	
VCAP2	AK60	PWR	
VCAP2	AK62	PWR	
VCAP2	R59	PWR	
VCAP2	R60	PWR	
VCAP2	U59	PWR	
VCAP2	U60	PWR	
VCAP2	W59	PWR	
VCAP2	W60	PWR	
VCC	A43	REF	
VCC	A47	REF	
VCC	A50	REF	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	A54	REF	
VCC	A57	REF	
VCC	AA41	REF	
VCC	AA44	REF	
VCC	AA48	REF	
VCC	AA51	REF	
VCC	AA55	REF	
VCC	AB41	REF	
VCC	AB44	REF	
VCC	AB48	REF	
VCC	AB51	REF	
VCC	AB55	REF	
VCC	AD41	REF	
VCC	AD44	REF	
VCC	AD48	REF	
VCC	AD51	REF	
VCC	AD55	REF	
VCC	AF41	REF	
VCC	AF42	REF	
VCC	AF44	REF	
VCC	AF46	REF	
VCC	AF48	REF	
VCC	AF50	REF	
VCC	AF51	REF	
VCC	AF53	REF	
VCC	AF55	REF	
VCC	AF57	REF	
VCC	B42	REF	
VCC	B46	REF	
VCC	B49	REF	
VCC	B53	REF	
VCC	B56	REF	
VCC	B60	REF	
VCC	D43	REF	
VCC	D45	REF	
VCC	D47	REF	
VCC	D48	REF	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	D50	REF	
VCC	D52	REF	
VCC	D54	REF	
VCC	D55	REF	
VCC	D57	REF	
VCC	D59	REF	
VCC	E42	REF	
VCC	E46	REF	
VCC	E50	REF	
VCC	E53	REF	
VCC	E57	REF	
VCC	E60	REF	
VCC	F55	REF	
VCC	G44	REF	
VCC	G51	REF	
VCC	G55	REF	
VCC	G60	REF	
VCC	H44	REF	
VCC	H51	REF	
VCC	H60	REF	
VCC	J55	REF	
VCC	K44	REF	
VCC	K51	REF	
VCC	K60	REF	
VCC	L55	REF	
VCC	M44	REF	
VCC	M51	REF	
VCC	M60	REF	
VCC	N42	REF	
VCC	N44	REF	
VCC	N48	REF	
VCC	N51	REF	
VCC	N55	REF	
VCC	P60	REF	
VCC	R41	REF	
VCC	R44	REF	
VCC	R48	REF	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	R51	REF	
VCC	R55	REF	
VCC	U41	REF	
VCC	U44	REF	
VCC	U48	REF	
VCC	U51	REF	
VCC	U55	REF	
VCC	W41	REF	
VCC	W44	REF	
VCC	W48	REF	
VCC	W51	REF	
VCC	W55	REF	
VCC_SENSE	F64	Analog	O
VCCPLL	R37	REF	
VCCPLL	R39	REF	
VCCPLL	U37	REF	
VCCPLL	W37	REF	
VCCPLL	W39	REF	
VCCPWRGOOD_0	Y67	Async CMOS	I
VCCPWRGOOD_1	AM7	Async CMOS	I
VDDQ	BB15	REF	
VDDQ	BB17	REF	
VDDQ	BB19	REF	
VDDQ	BB21	REF	
VDDQ	BB23	REF	
VDDQ	BB24	REF	
VDDQ	BB26	REF	
VDDQ	BB28	REF	
VDDQ	BB30	REF	
VDDQ	BB32	REF	
VDDQ	BB33	REF	
VDDQ	BB35	REF	
VDDQ	BD15	REF	
VDDQ	BD35	REF	
VDDQ	BF15	REF	
VDDQ	BF16	REF	
VDDQ_CK	BB12	REF	

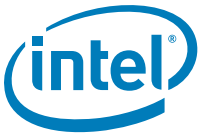


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VDDQ_CK	BB14	REF	
VID[0]	A61	CMOS	O
VID[1]	D61	CMOS	O
VID[2]	D62	CMOS	O
CSC[0]/VID[3]	A62	CMOS	I/O
CSC[1]VID[4]	B63	CMOS	I/O
CSC[2]VID[5]	D64	CMOS	I/O
VID[6]	D66	CMOS	O
VSS	A12	GND	
VSS	A15	GND	
VSS	A19	GND	
VSS	A22	GND	
VSS	A26	GND	
VSS	A29	GND	
VSS	A33	GND	
VSS	A36	GND	
VSS	A40	GND	
VSS	A45	GND	
VSS	A48	GND	
VSS	A52	GND	
VSS	A55	GND	
VSS	A59	GND	
VSS	A64	GND	
VSS	A66	GND	
VSS	A8	GND	
VSS	AA14	GND	
VSS	AA15	GND	
VSS	AA17	GND	
VSS	AA19	GND	
VSS	AA21	GND	
VSS	AA23	GND	
VSS	AA24	GND	
VSS	AA26	GND	
VSS	AA28	GND	
VSS	AA30	GND	
VSS	AA32	GND	
VSS	AA33	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AA35	GND	
VSS	AA37	GND	
VSS	AA39	GND	
VSS	AA4	GND	
VSS	AA42	GND	
VSS	AA46	GND	
VSS	AA50	GND	
VSS	AA53	GND	
VSS	AA57	GND	
VSS	AA62	GND	
VSS	AA64	GND	
VSS	AA66	GND	
VSS	AB14	GND	
VSS	AB15	GND	
VSS	AB17	GND	
VSS	AB19	GND	
VSS	AB21	GND	
VSS	AB23	GND	
VSS	AB24	GND	
VSS	AB26	GND	
VSS	AB28	GND	
VSS	AB30	GND	
VSS	AB32	GND	
VSS	AB33	GND	
VSS	AB35	GND	
VSS	AB37	GND	
VSS	AB39	GND	
VSS	AB42	GND	
VSS	AB46	GND	
VSS	AB50	GND	
VSS	AB53	GND	
VSS	AB57	GND	
VSS	AB62	GND	
VSS	AB70	GND	
VSS	AB9	GND	
VSS	AC1	GND	
VSS	AC10	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AC5	GND	
VSS	AC64	GND	
VSS	AC67	GND	
VSS	AD4	GND	
VSS	AD42	GND	
VSS	AD46	GND	
VSS	AD50	GND	
VSS	AD53	GND	
VSS	AD57	GND	
VSS	AD62	GND	
VSS	AE64	GND	
VSS	AE70	GND	
VSS	AF1	GND	
VSS	AF62	GND	
VSS	AF69	GND	
VSS	AG6	GND	
VSS	AG64	GND	
VSS	AG9	GND	
VSS	AH15	GND	
VSS	AH17	GND	
VSS	AH19	GND	
VSS	AH21	GND	
VSS	AH23	GND	
VSS	AH24	GND	
VSS	AH26	GND	
VSS	AH28	GND	
VSS	AH30	GND	
VSS	AH32	GND	
VSS	AH33	GND	
VSS	AH35	GND	
VSS	AH37	GND	
VSS	AH39	GND	
VSS	AH4	GND	
VSS	AH41	GND	
VSS	AH42	GND	
VSS	AH44	GND	
VSS	AH46	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AH48	GND	
VSS	AH50	GND	
VSS	AH51	GND	
VSS	AH53	GND	
VSS	AH55	GND	
VSS	AH57	GND	
VSS	AH62	GND	
VSS	AJ70	GND	
VSS	AK15	GND	
VSS	AK17	GND	
VSS	AK19	GND	
VSS	AK21	GND	
VSS	AK23	GND	
VSS	AK24	GND	
VSS	AK26	GND	
VSS	AK28	GND	
VSS	AK30	GND	
VSS	AK32	GND	
VSS	AK37	GND	
VSS	AK41	GND	
VSS	AK44	GND	
VSS	AK48	GND	
VSS	AK51	GND	
VSS	AK55	GND	
VSS	AK64	GND	
VSS	AK70	GND	
VSS	AL1	GND	
VSS	AL33	GND	
VSS	AL35	GND	
VSS	AL37	GND	
VSS	AL41	GND	
VSS	AL44	GND	
VSS	AL48	GND	
VSS	AL51	GND	
VSS	AL55	GND	
VSS	AL62	GND	
VSS	AM64	GND	

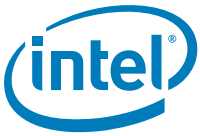


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AM8	GND	
VSS	AN37	GND	
VSS	AN4	GND	
VSS	AN41	GND	
VSS	AN44	GND	
VSS	AN48	GND	
VSS	AN5	GND	
VSS	AN51	GND	
VSS	AN55	GND	
VSS	AN62	GND	
VSS	AP64	GND	
VSS	AP70	GND	
VSS	AR1	GND	
VSS	AR14	GND	
VSS	AR15	GND	
VSS	AR17	GND	
VSS	AR19	GND	
VSS	AR21	GND	
VSS	AR23	GND	
VSS	AR24	GND	
VSS	AR26	GND	
VSS	AR28	GND	
VSS	AR30	GND	
VSS	AR32	GND	
VSS	AR33	GND	
VSS	AR35	GND	
VSS	AR39	GND	
VSS	AR4	GND	
VSS	AR42	GND	
VSS	AR46	GND	
VSS	AR50	GND	
VSS	AR53	GND	
VSS	AR57	GND	
VSS	AR62	GND	
VSS	AT10	GND	
VSS	AT64	GND	
VSS	AU14	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AU15	GND	
VSS	AU17	GND	
VSS	AU19	GND	
VSS	AU21	GND	
VSS	AU23	GND	
VSS	AU24	GND	
VSS	AU26	GND	
VSS	AU28	GND	
VSS	AU30	GND	
VSS	AU32	GND	
VSS	AU33	GND	
VSS	AU35	GND	
VSS	AU39	GND	
VSS	AU4	GND	
VSS	AU42	GND	
VSS	AU46	GND	
VSS	AU50	GND	
VSS	AU53	GND	
VSS	AU57	GND	
VSS	AU62	GND	
VSS	AU70	GND	
VSS	AV1	GND	
VSS	AV9	GND	
VSS	AW37	GND	
VSS	AW41	GND	
VSS	AW44	GND	
VSS	AW48	GND	
VSS	AW51	GND	
VSS	AW55	GND	
VSS	AW59	GND	
VSS	AW62	GND	
VSS	AW67	GND	
VSS	AY12	GND	
VSS	AY14	GND	
VSS	AY15	GND	
VSS	AY17	GND	
VSS	AY19	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AY21	GND	
VSS	AY23	GND	
VSS	AY24	GND	
VSS	AY26	GND	
VSS	AY28	GND	
VSS	AY30	GND	
VSS	AY32	GND	
VSS	AY33	GND	
VSS	AY35	GND	
VSS	AY37	GND	
VSS	AY4	GND	
VSS	AY41	GND	
VSS	AY44	GND	
VSS	AY48	GND	
VSS	AY51	GND	
VSS	AY55	GND	
VSS	AY59	GND	
VSS	AY62	GND	
VSS	AY66	GND	
VSS	AY71	GND	
VSS	AY8	GND	
VSS	B40	GND	
VSS	B44	GND	
VSS	B48	GND	
VSS	B51	GND	
VSS	B55	GND	
VSS	B58	GND	
VSS	B62	GND	
VSS	B65	GND	
VSS	BA70	GND	
VSS	BB1	GND	
VSS	BB39	GND	
VSS	BB42	GND	
VSS	BB46	GND	
VSS	BB50	GND	
VSS	BB53	GND	
VSS	BB57	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BB62	GND	
VSS	BB7	GND	
VSS	BB71	GND	
VSS	BD14	GND	
VSS	BD39	GND	
VSS	BD42	GND	
VSS	BD46	GND	
VSS	BD50	GND	
VSS	BD53	GND	
VSS	BD57	GND	
VSS	BE1	GND	
VSS	BE65	GND	
VSS	BE70	GND	
VSS	BE9	GND	
VSS	BF13	GND	
VSS	BF30	GND	
VSS	BF62	GND	
VSS	BF8	GND	
VSS	BG36	GND	
VSS	BG51	GND	
VSS	BH15	GND	
VSS	BH20	GND	
VSS	BH24	GND	
VSS	BH47	GND	
VSS	BH55	GND	
VSS	BH57	GND	
VSS	BH70	GND	
VSS	BJ1	GND	
VSS	BJ21	GND	
VSS	BJ64	GND	
VSS	BJ9	GND	
VSS	BK10	GND	
VSS	BK34	GND	
VSS	BK53	GND	
VSS	BK60	GND	
VSS	BK63	GND	
VSS	BL1	GND	

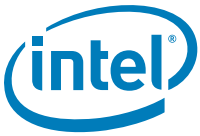


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BL20	GND	
VSS	BL28	GND	
VSS	BL40	GND	
VSS	BL48	GND	
VSS	BL55	GND	
VSS	BL57	GND	
VSS	BL71	GND	
VSS	BM17	GND	
VSS	BM24	GND	
VSS	BM32	GND	
VSS	BM44	GND	
VSS	BM51	GND	
VSS	BM70	GND	
VSS	BN1	GND	
VSS	BN6	GND	
VSS	BN64	GND	
VSS	BN71	GND	
VSS	BP42	GND	
VSS	BR3	GND	
VSS	BR68	GND	
VSS	BR69	GND	
VSS	BT68	GND	
VSS	BU11	GND	
VSS	BU14	GND	
VSS	BU18	GND	
VSS	BU21	GND	
VSS	BU25	GND	
VSS	BU32	GND	
VSS	BU37	GND	
VSS	BU44	GND	
VSS	BU48	GND	
VSS	BU51	GND	
VSS	BU55	GND	
VSS	BU58	GND	
VSS	BU62	GND	
VSS	BU7	GND	
VSS	BV64	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BV66	GND	
VSS	C68	GND	
VSS	D10	GND	
VSS	D13	GND	
VSS	D17	GND	
VSS	D20	GND	
VSS	D24	GND	
VSS	D27	GND	
VSS	D31	GND	
VSS	D34	GND	
VSS	D38	GND	
VSS	D41	GND	
VSS	D6	GND	
VSS	E12	GND	
VSS	E16	GND	
VSS	E30	GND	
VSS	E33	GND	
VSS	E37	GND	
VSS	E5	GND	
VSS	E68	GND	
VSS	E69	GND	
VSS	F20	GND	
VSS	F28	GND	
VSS	F4	GND	
VSS	F47	GND	
VSS	F48	GND	
VSS	F61	GND	
VSS	F71	GND	
VSS	G15	GND	
VSS	G20	GND	
VSS	G24	GND	
VSS	G30	GND	
VSS	G43	GND	
VSS	G47	GND	
VSS	G48	GND	
VSS	G53	GND	
VSS	G57	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	G70	GND	
VSS	H1	GND	
VSS	H36	GND	
VSS	H43	GND	
VSS	H53	GND	
VSS	H71	GND	
VSS	J40	GND	
VSS	J47	GND	
VSS	J48	GND	
VSS	J57	GND	
VSS	J65	GND	
VSS	J9	GND	
VSS	K11	GND	
VSS	K17	GND	
VSS	K25	GND	
VSS	K32	GND	
VSS	K34	GND	
VSS	K36	GND	
VSS	K4	GND	
VSS	K43	GND	
VSS	K53	GND	
VSS	K6	GND	
VSS	K64	GND	
VSS	L13	GND	
VSS	L47	GND	
VSS	L48	GND	
VSS	L57	GND	
VSS	L70	GND	
VSS	M1	GND	
VSS	M36	GND	
VSS	M42	GND	
VSS	M53	GND	
VSS	N15	GND	
VSS	N21	GND	
VSS	N30	GND	
VSS	N46	GND	
VSS	N50	GND	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	N53	GND	
VSS	N57	GND	
VSS	N63	GND	
VSS	P4	GND	
VSS	R14	GND	
VSS	R42	GND	
VSS	R46	GND	
VSS	R5	GND	
VSS	R50	GND	
VSS	R53	GND	
VSS	R57	GND	
VSS	R62	GND	
VSS	R70	GND	
VSS	T1	GND	
VSS	U39	GND	
VSS	U4	GND	
VSS	U42	GND	
VSS	U46	GND	
VSS	U50	GND	
VSS	U53	GND	
VSS	U57	GND	
VSS	U62	GND	
VSS	U64	GND	
VSS	U9	GND	
VSS	V70	GND	
VSS	W1	GND	
VSS	W42	GND	
VSS	W46	GND	
VSS	W50	GND	
VSS	W53	GND	
VSS	W57	GND	
VSS	W6	GND	
VSS	W62	GND	
VSS	W69	GND	
VSS_SENSE	F63	Analog	O
VSS_SENSE_VTT	R12	Analog	O
VSSAXG_SENSE	AF10	Analog	O

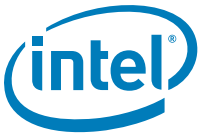


Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VTT_SELECT	AN1	CMOS	O
VTT_SENSE	N13	Analog	O
VTT0	AD30	REF	
VTT0	AD32	REF	
VTT0	AD33	REF	
VTT0	AD35	REF	
VTT0	AD37	REF	
VTT0	AD39	REF	
VTT0	AF30	REF	
VTT0	AF32	REF	
VTT0	AF33	REF	
VTT0	AF35	REF	
VTT0	AF37	REF	
VTT0	AF39	REF	
VTT0	AK33	REF	
VTT0	AK35	REF	
VTT0	AL12	REF	
VTT0	AL14	REF	
VTT0	AL15	REF	
VTT0	AL17	REF	
VTT0	AL59	REF	
VTT0	AL60	REF	
VTT0	AM10	REF	
VTT0	AN12	REF	
VTT0	AN14	REF	
VTT0	AN15	REF	
VTT0	AN17	REF	
VTT0	AN33	REF	
VTT0	AN35	REF	
VTT0	AN59	REF	
VTT0	AN60	REF	
VTT0	AN9	REF	
VTT0	AR12	REF	
VTT0	AR59	REF	
VTT0	AR60	REF	
VTT0	AU12	REF	
VTT0	AU59	REF	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VTT0	AU60	REF	
VTT0	AW12	REF	
VTT0	AW14	REF	
VTT0	AW33	REF	
VTT0	AW35	REF	
VTT0	AW60	REF	
VTT0	AY10	REF	
VTT0	AY60	REF	
VTT0	BB59	REF	
VTT0	BB60	REF	
VTT0	BD59	REF	
VTT0	BD60	REF	
VTT0	BF59	REF	
VTT0	BF60	REF	
VTT0	R23	REF	
VTT0	R24	REF	
VTT0	R26	REF	
VTT0	R28	REF	
VTT0	R30	REF	
VTT0	R32	REF	
VTT0	R33	REF	
VTT0	R35	REF	
VTT0	U23	REF	
VTT0	U24	REF	
VTT0	U26	REF	
VTT0	U28	REF	
VTT0	U30	REF	
VTT0	U32	REF	
VTT0	U33	REF	
VTT0	U35	REF	
VTT0	W23	REF	
VTT0	W24	REF	
VTT0	W26	REF	
VTT0	W28	REF	
VTT0	W30	REF	
VTT0	W32	REF	
VTT0	W33	REF	

Table 12. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VTT0	W35	REF	
VTT0_DDR	AW15	REF	
VTT0_DDR	AW17	REF	
VTT0_DDR	AW19	REF	
VTT0_DDR	AW21	REF	
VTT0_DDR	AW23	REF	
VTT0_DDR	AW24	REF	
VTT0_DDR	AW26	REF	
VTT0_DDR	AW28	REF	
VTT0_DDR	AW30	REF	
VTT0_DDR	AW32	REF	
VTT1	AA12	REF	
VTT1	AB12	REF	
VTT1	AD12	REF	
VTT1	AD14	REF	
VTT1	AD15	REF	
VTT1	R15	REF	
VTT1	R17	REF	
VTT1	R19	REF	
VTT1	R21	REF	
VTT1	U12	REF	
VTT1	U14	REF	
VTT1	U15	REF	
VTT1	U17	REF	
VTT1	U19	REF	
VTT1	U21	REF	
VTT1	W12	REF	
VTT1	W14	REF	
VTT1	W15	REF	
VTT1	W17	REF	
VTT1	W19	REF	
VTT1	W21	REF	
VTTPWRGOOD	H15	Async CMOS	I

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
A5	DC_TEST_A5		
A6	RSVD_NCTF		
A8	VSS	GND	
A10	RSVD		
A12	VSS	GND	
A13	PEG_ICOMPO	Analog	I
A15	VSS	GND	
A17	PEG_RX#[14]	PCIe	I
A19	VSS	GND	
A20	PEG_RX#[12]	PCIe	I
A22	VSS	GND	
A24	PEG_RX[10]	PCIe	I
A26	VSS	GND	
A27	PEG_RX[8]	PCIe	I
A29	VSS	GND	
A31	PEG_TX#[9]	PCIe	O
A33	VSS	GND	
A34	PEG_TX[6]	PCIe	O
A36	VSS	GND	
A38	PEG_TX#[4]	PCIe	O
A40	VSS	GND	
A41	ISENSE	Analog	I
A43	VCC	REF	
A45	VSS	GND	
A47	VCC	REF	
A48	VSS	GND	
A50	VCC	REF	
A52	VSS	GND	
A54	VCC	REF	
A55	VSS	GND	
A57	VCC	REF	
A59	VSS	GND	
A61	VID[0]	CMOS	O
A62	CSC[0]/VID[3]	CMOS	I/O
A64	VSS	GND	

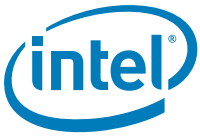


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
A66	VSS	GND	
A68	DC_TEST_A68		
A69	DC_TEST_A69		
A71	DC_TEST_A71		
AA1	FDI_LSYNC[0]	CMOS	I
AA4	VSS	GND	
AA12	VTT1	REF	
AA14	VSS	GND	
AA15	VSS	GND	
AA17	VSS	GND	
AA19	VSS	GND	
AA21	VSS	GND	
AA23	VSS	GND	
AA24	VSS	GND	
AA26	VSS	GND	
AA28	VSS	GND	
AA30	VSS	GND	
AA32	VSS	GND	
AA33	VSS	GND	
AA35	VSS	GND	
AA37	VSS	GND	
AA39	VSS	GND	
AA41	VCC	REF	
AA42	VSS	GND	
AA44	VCC	REF	
AA46	VSS	GND	
AA48	VCC	REF	
AA50	VSS	GND	
AA51	VCC	REF	
AA53	VSS	GND	
AA55	VCC	REF	
AA57	VSS	GND	
AA59	VCAP2	PWR	
AA60	VCAP2	PWR	
AA62	VSS	GND	
AA64	VSS	GND	
AA66	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AA69	RSVD		
AA71	RSVD		
AB2	FDI_LSYNC[1]	CMOS	I
AB5	FDI_INT	CMOS	I
AB7	CFG[17]	CMOS	I
AB9	VSS	GND	
AB12	VTT1	REF	
AB14	VSS	GND	
AB15	VSS	GND	
AB17	VSS	GND	
AB19	VSS	GND	
AB21	VSS	GND	
AB23	VSS	GND	
AB24	VSS	GND	
AB26	VSS	GND	
AB28	VSS	GND	
AB30	VSS	GND	
AB32	VSS	GND	
AB33	VSS	GND	
AB35	VSS	GND	
AB37	VSS	GND	
AB39	VSS	GND	
AB41	VCC	REF	
AB42	VSS	GND	
AB44	VCC	REF	
AB46	VSS	GND	
AB48	VCC	REF	
AB50	VSS	GND	
AB51	VCC	REF	
AB53	VSS	GND	
AB55	VCC	REF	
AB57	VSS	GND	
AB59	VCAP2	PWR	
AB60	VCAP2	PWR	
AB62	VSS	GND	
AB70	VSS	GND	
AC1	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AC2	CFG[11]	CMOS	I
AC4	CFG[12]	CMOS	I
AC5	VSS	GND	
AC7	FDI_FSYNC[0]	CMOS	I
AC9	FDI_FSYNC[1]	CMOS	I
AC10	VSS	GND	
AC64	VSS	GND	
AC67	VSS	GND	
AC69	RSVD		
AC70	COMP2	Analog	I
AC71	RSVD		
AD1	CFG[14]	CMOS	I
AD4	VSS	GND	
AD12	VTT1	REF	
AD14	VTT1	REF	
AD15	VTT1	REF	
AD17	VAXG	REF	
AD19	VAXG	REF	
AD21	VAXG	REF	
AD23	VAXG	REF	
AD24	VAXG	REF	
AD26	VAXG	REF	
AD28	VAXG	REF	
AD30	VTT0	REF	
AD32	VTT0	REF	
AD33	VTT0	REF	
AD35	VTT0	REF	
AD37	VTT0	REF	
AD39	VTT0	REF	
AD41	VCC	REF	
AD42	VSS	GND	
AD44	VCC	REF	
AD46	VSS	GND	
AD48	VCC	REF	
AD50	VSS	GND	
AD51	VCC	REF	
AD53	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AD55	VCC	REF	
AD57	VSS	GND	
AD59	VCAP2	PWR	
AD60	VCAP2	PWR	
AD62	VSS	GND	
AD69	COMP1	Analog	I
AD71	COMP3	Analog	I
AE2	CFG[13]	CMOS	I
AE64	VSS	GND	
AE66	COMP0	Analog	I
AE70	VSS	GND	
AF1	VSS	GND	
AF4	CFG[8]	CMOS	I
AF10	VSSAXG_SENSE	Analog	O
AF12	VAXG_SENSE	Analog	O
AF14	VAXG	REF	
AF15	VAXG	REF	
AF17	VAXG	REF	
AF19	VAXG	REF	
AF21	VAXG	REF	
AF23	VAXG	REF	
AF24	VAXG	REF	
AF26	VAXG	REF	
AF28	VAXG	REF	
AF30	VTT0	REF	
AF32	VTT0	REF	
AF33	VTT0	REF	
AF35	VTT0	REF	
AF37	VTT0	REF	
AF39	VTT0	REF	
AF41	VCC	REF	
AF42	VCC	REF	
AF44	VCC	REF	
AF46	VCC	REF	
AF48	VCC	REF	
AF50	VCC	REF	
AF51	VCC	REF	

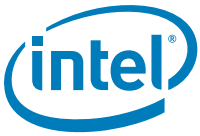


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AF53	VCC	REF	
AF55	VCC	REF	
AF57	VCC	REF	
AF59	VCAP2	PWR	
AF6	CFG[16]	CMOS	I
AF60	VCAP2	PWR	
AF62	VSS	GND	
AF69	VSS	GND	
AF71	GFX_VID[0]	CMOS	O
AF8	CFG[15]	CMOS	I
AG2	CFG[9]	CMOS	I
AG6	VSS	GND	
AG7	CFG[7]	CMOS	I
AG9	VSS	GND	
AG64	VSS	GND	
AG67	GFX_VID[1]	CMOS	O
AG70	GFX_VID[2]	CMOS	O
AH1	CFG[10]	CMOS	I
AH4	VSS	GND	
AH12	VAXG	REF	
AH14	VAXG	REF	
AH15	VSS	GND	
AH17	VSS	GND	
AH19	VSS	GND	
AH21	VSS	GND	
AH23	VSS	GND	
AH24	VSS	GND	
AH26	VSS	GND	
AH28	VSS	GND	
AH30	VSS	GND	
AH32	VSS	GND	
AH33	VSS	GND	
AH35	VSS	GND	
AH37	VSS	GND	
AH39	VSS	GND	
AH41	VSS	GND	
AH42	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AH44	VSS	GND	
AH46	VSS	GND	
AH48	VSS	GND	
AH50	VSS	GND	
AH51	VSS	GND	
AH53	VSS	GND	
AH55	VSS	GND	
AH57	VSS	GND	
AH59	VCAP2	PWR	
AH60	VCAP2	PWR	
AH62	VSS	GND	
AH66	RSVD		
AH69	GFX_VR_EN	CMOS	O
AH71	GFX_VID[3]	CMOS	O
AJ10	VAXG	REF	
AJ2	CFG[5]	CMOS	I
AJ70	VSS	GND	
AK1	CFG[2]	CMOS	I
AK2	CFG[3]	CMOS	I
AK4	CFG[4]	CMOS	I
AK7	BCLK	DIFF CLK	I
AK8	BCLK #	DIFF CLK	I
AK12	VAXG	REF	
AK14	VAXG	REF	
AK15	VSS	GND	
AK17	VSS	GND	
AK19	VSS	GND	
AK21	VSS	GND	
AK23	VSS	GND	
AK24	VSS	GND	
AK26	VSS	GND	
AK28	VSS	GND	
AK30	VSS	GND	
AK32	VSS	GND	
AK33	VTT0	REF	
AK35	VTT0	REF	
AK37	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AK39	VCAP1	PWR	
AK41	VSS	GND	
AK42	VCAP1	PWR	
AK44	VSS	GND	
AK46	VCAP1	PWR	
AK48	VSS	GND	
AK50	VCAP0	PWR	
AK51	VSS	GND	
AK53	VCAP0	PWR	
AK55	VSS	GND	
AK57	VCAP0	PWR	
AK59	VCAP2	PWR	
AK60	VCAP2	PWR	
AK62	VCAP2	PWR	
AK64	VSS	GND	
AK66	RSVD		
AK69	RSVD		
AK70	VSS	GND	
AK71	RSVD		
AL1	VSS	GND	
AL4	CFG[0]	CMOS	I
AL12	VTT0	REF	
AL14	VTT0	REF	
AL15	VTT0	REF	
AL17	VTT0	REF	
AL19	VAXG	REF	
AL21	VAXG	REF	
AL23	VAXG	REF	
AL24	VAXG	REF	
AL26	VAXG	REF	
AL28	VAXG	REF	
AL30	VAXG	REF	
AL32	VAXG	REF	
AL33	VSS	GND	
AL35	VSS	GND	
AL37	VSS	GND	
AL39	VCAP1	PWR	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AL41	VSS	GND	
AL42	VCAP1	PWR	
AL44	VSS	GND	
AL46	VCAP1	PWR	
AL48	VSS	GND	
AL50	VCAP0	PWR	
AL51	VSS	GND	
AL53	VCAP0	PWR	
AL55	VSS	GND	
AL57	VCAP0	PWR	
AL59	VTT0	REF	
AL60	VTT0	REF	
AL62	VSS	GND	
AL69	GFX_IMON	CMOS	I
AL71	GFX_DPRSLPVR	CMOS	O
AM10	VTT0	REF	
AM2	CFG[1]	CMOS	I
AM5	SM_DRAMPWROK	Async CMOS	I
AM7	VCCPWRGOOD_1	Async CMOS	I
AM8	VSS	GND	
AM64	VSS	GND	
AM66	RSVD		
AM67	GFX_VID[5]	CMOS	O
AM70	GFX_VID[6]	CMOS	O
AN1	VTT_SELECT	CMOS	O
AN4	VSS	GND	
AN5	VSS	GND	
AN7	RSVD_TP		
AN9	VTT0	REF	
AN12	VTT0	REF	
AN14	VTT0	REF	
AN15	VTT0	REF	
AN17	VTT0	REF	
AN19	VAXG	REF	
AN21	VAXG	REF	
AN23	VAXG	REF	
AN24	VAXG	REF	

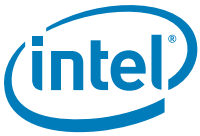


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AN26	VAXG	REF	
AN28	VAXG	REF	
AN30	VAXG	REF	
AN32	VAXG	REF	
AN33	VTT0	REF	
AN35	VTT0	REF	
AN37	VSS	GND	
AN39	VCAP1	PWR	
AN41	VSS	GND	
AN42	VCAP1	PWR	
AN44	VSS	GND	
AN46	VCAP1	PWR	
AN48	VSS	GND	
AN50	VCAP0	PWR	
AN51	VSS	GND	
AN53	VCAP0	PWR	
AN55	VSS	GND	
AN57	VCAP0	PWR	
AN59	VTT0	REF	
AN60	VTT0	REF	
AN62	VSS	GND	
AN69	RSVD		
AN71	GFX_VID[4]	CMOS	O
AP2	RSVD_TP		
AP64	VSS	GND	
AP66	RSVD		
AP70	VSS	GND	
AR1	VSS	GND	
AR4	VSS	GND	
AR12	VTT0	REF	
AR14	VSS	GND	
AR15	VSS	GND	
AR17	VSS	GND	
AR19	VSS	GND	
AR21	VSS	GND	
AR23	VSS	GND	
AR24	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AR26	VSS	GND	
AR28	VSS	GND	
AR30	VSS	GND	
AR32	VSS	GND	
AR33	VSS	GND	
AR35	VSS	GND	
AR37	VCAP1	PWR	
AR39	VSS	GND	
AR41	VCAP1	PWR	
AR42	VSS	GND	
AR44	VCAP1	PWR	
AR46	VSS	GND	
AR48	VCAP0	PWR	
AR50	VSS	GND	
AR51	VCAP0	PWR	
AR53	VSS	GND	
AR55	VCAP0	PWR	
AR57	VSS	GND	
AR59	VTT0	REF	
AR60	VTT0	REF	
AR62	VSS	GND	
AR69	RSVD		
AR71	RSVD		
AT2	CFG[6]	CMOS	I
AT6	SA_DQ[1]	DDR3	I/O
AT8	SA_DQ[0]	DDR3	I/O
AT10	VSS	GND	
AT64	VSS	GND	
AT67	RSVD		
AT70	RSVD		
AU1	RSVD_TP		
AU2	RSVD		
AU4	VSS	GND	
AU12	VTT0	REF	
AU14	VSS	GND	
AU15	VSS	GND	
AU17	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AU19	VSS	GND	
AU21	VSS	GND	
AU23	VSS	GND	
AU24	VSS	GND	
AU26	VSS	GND	
AU28	VSS	GND	
AU30	VSS	GND	
AU32	VSS	GND	
AU33	VSS	GND	
AU35	VSS	GND	
AU37	VCAP1	PWR	
AU39	VSS	GND	
AU41	VCAP1	PWR	
AU42	VSS	GND	
AU44	VCAP1	PWR	
AU46	VSS	GND	
AU48	VCAP0	PWR	
AU50	VSS	GND	
AU51	VCAP0	PWR	
AU53	VSS	GND	
AU55	VCAP0	PWR	
AU57	VSS	GND	
AU59	VTT0	REF	
AU60	VTT0	REF	
AU62	VSS	GND	
AU69	RSVD		
AU70	VSS	GND	
AU71	RSVD		
AV1	VSS	GND	
AV4	RSVD		
AV6	SA_DQ[5]	DDR3	I/O
AV7	SA_DQ[4]	DDR3	I/O
AV9	VSS	GND	
AV64	PM_EXT_TS#[1]	CMOS	I
AV66	PM_EXT_TS#[0]	CMOS	I
AV69	RSVD		
AV71	RSVD		

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AW12	VTT0	REF	
AW14	VTT0	REF	
AW15	VTT0_DDR	REF	
AW17	VTT0_DDR	REF	
AW19	VTT0_DDR	REF	
AW2	SB_DQ[1]	DDR3	I/O
AW21	VTT0_DDR	REF	
AW23	VTT0_DDR	REF	
AW24	VTT0_DDR	REF	
AW26	VTT0_DDR	REF	
AW28	VTT0_DDR	REF	
AW30	VTT0_DDR	REF	
AW32	VTT0_DDR	REF	
AW33	VTT0	REF	
AW35	VTT0	REF	
AW37	VSS	GND	
AW39	VCAP1	PWR	
AW41	VSS	GND	
AW42	VCAP1	PWR	
AW44	VSS	GND	
AW46	VCAP1	PWR	
AW48	VSS	GND	
AW50	VCAP0	PWR	
AW51	VSS	GND	
AW53	VCAP0	PWR	
AW55	VSS	GND	
AW57	VCAP0	PWR	
AW59	VSS	GND	
AW60	VTT0	REF	
AW62	VSS	GND	
AW67	VSS	GND	
AW70	RSVD	DDR3	
AY1	SB_DQ[4]	DDR3	I/O
AY4	VSS	GND	
AY5	SA_DQS#[0]	DDR3	I/O
AY7	SA_DQS[0]	DDR3	I/O
AY8	VSS	GND	

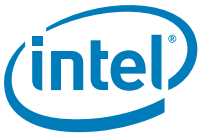


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AY10	VTT0	REF	
AY12	VSS	GND	
AY14	VSS	GND	
AY15	VSS	GND	
AY17	VSS	GND	
AY19	VSS	GND	
AY21	VSS	GND	
AY23	VSS	GND	
AY24	VSS	GND	
AY26	VSS	GND	
AY28	VSS	GND	
AY30	VSS	GND	
AY32	VSS	GND	
AY33	VSS	GND	
AY35	VSS	GND	
AY37	VSS	GND	
AY39	VCAP1	PWR	
AY41	VSS	GND	
AY42	VCAP1	PWR	
AY44	VSS	GND	
AY46	VCAP1	PWR	
AY48	VSS	GND	
AY50	VCAP0	PWR	
AY51	VSS	GND	
AY53	VCAP0	PWR	
AY55	VSS	GND	
AY57	VCAP0	PWR	
AY59	VSS	GND	
AY60	VTT0	REF	
AY62	VSS	GND	
AY64	SA_DQ[62]	DDR3	I/O
AY66	VSS	GND	
AY69	RSVD		
AY71	VSS	GND	
B7	RSVD		
B9	RSVD		
B11	PEG_RBIAS	Analog	I

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
B12	PEG_ICOMPI	Analog	I
B14	PEG_RX#[15]	PCIe	I
B16	PEG_RX[14]	PCIe	I
B18	PEG_RX[13]	PCIe	I
B19	PEG_RX[12]	PCIe	I
B21	PEG_RX[11]	PCIe	I
B23	PEG_RX#[10]	PCIe	I
B25	PEG_RX[9]	PCIe	I
B26	PEG_RX#[8]	PCIe	I
B28	PEG_RX[7]	PCIe	I
B30	PEG_TX[9]	PCIe	O
B32	PEG_TX#[10]	PCIe	O
B33	PEG_TX#[6]	PCIe	O
B35	PEG_TX#[7]	PCIe	O
B37	PEG_TX[4]	PCIe	O
B39	PEG_TX[3]	PCIe	O
B40	VSS	GND	
B42	VCC	REF	
B44	VSS	GND	
B46	VCC	REF	
B48	VSS	GND	
B49	VCC	REF	
B51	VSS	GND	
B53	VCC	REF	
B55	VSS	GND	
B56	VCC	REF	
B58	VSS	GND	
B60	VCC	REF	
B62	VSS	GND	
B63	CSC[1]/VID[4]	CMOS	I/O
B65	VSS	GND	
BA2	SB_DQ[0]	DDR3	I/O
BA70	VSS	GND	
BB1	VSS	GND	
BB4	SB_DM[0]	DDR3	O
BB5	SA_DQ[2]	DDR3	I/O
BB7	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BB9	SA_DQ[3]	DDR3	I/O
BB10	SA_DM[0]	DDR3	O
BB12	VDDQ_CK	REF	
BB14	VDDQ_CK	REF	
BB15	VDDQ	REF	
BB17	VDDQ	REF	
BB19	VDDQ	REF	
BB21	VDDQ	REF	
BB23	VDDQ	REF	
BB24	VDDQ	REF	
BB26	VDDQ	REF	
BB28	VDDQ	REF	
BB30	VDDQ	REF	
BB32	VDDQ	REF	
BB33	VDDQ	REF	
BB35	VDDQ	REF	
BB37	VCAP1	PWR	
BB39	VSS	GND	
BB41	VCAP1	PWR	
BB42	VSS	GND	
BB44	VCAP1	PWR	
BB46	VSS	GND	
BB48	VCAP0	PWR	
BB50	VSS	GND	
BB51	VCAP0	PWR	
BB53	VSS	GND	
BB55	VCAP0	PWR	
BB57	VSS	GND	
BB59	VTT0	REF	
BB60	VTT0	REF	
BB62	VSS	GND	
BB64	SA_DQ[58]	DDR3	I/O
BB66	SA_DQ[59]	DDR3	I/O
BB69	RSVD		
BB71	VSS	GND	
BC2	SB_DQ[5]	DDR3	I/O
BC67	SB_DQ[59]	DDR3	I/O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BC70	SA_DQ[63]	DDR3	I/O
BD1	SB_DQ[2]	DDR3	I/O
BD4	SB_DQS[0]	DDR3	I/O
BD14	VSS	GND	
BD15	VDDQ	REF	
BD17	SB_DQS#[8]	DDR3	I/O
BD19	SB_DQS[8]	DDR3	I/O
BD21	SB_DQ[64]	DDR3	I/O
BD23	SB_DQ[69]	DDR3	I/O
BD24	SB_DQ[65]	DDR3	I/O
BD26	SA_DQ[68]	DDR3	I/O
BD28	SA_DQ[65]	DDR3	I/O
BD30	SA_DQ[64]	DDR3	I/O
BD32	SA_DQS#[8]	DDR3	I/O
BD33	SA_DQS[8]	DDR3	I/O
BD35	VDDQ	REF	
BD37	VCAP1	PWR	
BD39	VSS	GND	
BD41	VCAP1	PWR	
BD42	VSS	GND	
BD44	VCAP1	PWR	
BD46	VSS	GND	
BD48	VCAP0	PWR	
BD50	VSS	GND	
BD51	VCAP0	PWR	
BD53	VSS	GND	
BD55	VCAP0	PWR	
BD57	VSS	GND	
BD59	VTT0	REF	
BD60	VTT0	REF	
BD69	SB_DQ[63]	DDR3	I/O
BD71	SB_DQ[62]	DDR3	I/O
BE1	VSS	GND	
BE2	SB_DQS#[0]	DDR3	I/O
BE4	SB_DQ[3]	DDR3	I/O
BE6	SA_DQ[6]	DDR3	I/O
BE8	SA_DQ[7]	DDR3	I/O

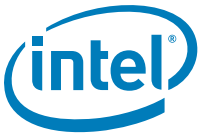


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BE9	VSS	GND	
BE11	SA_DQ[8]	DDR3	I/O
BE62	SA_DQS#[7]	DDR3	I/O
BE64	SA_DQS[7]	DDR3	I/O
BE65	VSS	GND	
BE69	RSVD		
BE70	VSS	GND	
BE71	RSVD		
BF2	SB_DQ[6]	DDR3	I/O
BF6	SA_DQ[13]	DDR3	I/O
BF8	VSS	GND	
BF9	SA_DQ[12]	DDR3	I/O
BF11	SA_DQ[9]	DDR3	I/O
BF13	VSS	GND	
BF15	VDDQ	REF	
BF16	VDDQ	REF	
BF20	SA_CKE[0]	DDR3	O
BF21	SA_BS[2]	DDR3	O
BF28	SA_MA[9]	DDR3	O
BF30	VSS	GND	
BF38	SA_WE#	DDR3	O
BF40	SA_MA[13]	DDR3	O
BF43	SA_ODT[0]	DDR3	O
BF47	SA_DQ[34]	DDR3	I/O
BF48	SA_DQ[35]	DDR3	I/O
BF55	SA_DQ[48]	DDR3	I/O
BF57	SA_DQ[52]	DDR3	I/O
BF59	VTT0	REF	
BF60	VTT0	REF	
BF62	VSS	GND	
BF64	SA_DQ[57]	DDR3	I/O
BF65	SA_DQ[61]	DDR3	I/O
BF67	SB_DM[7]	DDR3	O
BF70	SB_DQ[57]	DDR3	I/O
BG1	SB_DQ[9]	DDR3	I/O
BG4	SB_DQ[8]	DDR3	I/O
BG15	SA_DQ[25]	DDR3	I/O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BG17	SA_DQ[19]	DDR3	I/O
BG24	SA_DQ[30]	DDR3	I/O
BG25	SA_DQ[31]	DDR3	I/O
BG32	SA_MA[4]	DDR3	O
BG34	SA_MA[3]	DDR3	O
BG36	VSS	GND	
BG43	SA_DQ[70]	DDR3	I/O
BG44	SA_DM[4]	DDR3	O
BG51	VSS	GND	
BG53	SA_DM[5]	DDR3	O
BG69	SB_DQS#[7]	DDR3	I/O
BG71	SB_DQ[58]	DDR3	I/O
BH2	SB_DQ[7]	DDR3	I/O
BH13	SA_DQ[11]	DDR3	I/O
BH15	VSS	GND	
BH17	SA_DQ[18]	DDR3	I/O
BH20	VSS	GND	
BH21	SA_DQ[29]	DDR3	I/O
BH24	VSS	GND	
BH25	SA_DQ[27]	DDR3	I/O
BH28	SA_DQ[69]	DDR3	I/O
BH30	SA_MA[11]	DDR3	O
BH32	SB_DQ[66]	DDR3	I/O
BH34	SA_MA[10]	DDR3	O
BH36	SA_CK[1]	DDR3	O
BH38	SA_BS[1]	DDR3	O
BH40	SA_CS#[0]	DDR3	O
BH43	SA_DQ[37]	DDR3	I/O
BH44	SA_DQS#[4]	DDR3	I/O
BH47	VSS	GND	
BH48	SA_DQ[44]	DDR3	I/O
BH51	SA_DQS[5]	DDR3	I/O
BH53	SA_DQ[42]	DDR3+C285	I/O
BH55	VSS	GND	
BH57	VSS	GND	
BH59	SA_DM[7]	DDR3	O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BH70	VSS	GND	
BJ1	VSS	GND	
BJ4	SB_DQ[12]	DDR3	I/O
BJ5	SA_DQS[1]	DDR3	I/O
BJ7	SA_DQS#[1]	DDR3	I/O
BJ9	VSS	GND	
BJ10	SA_DQ[10]	DDR3	I/O
BJ12	SM_DRAMRST#	DDR3	O
BJ20	SA_DQ[28]	DDR3	I/O
BJ21	VSS	GND	
BJ28	SA_MA[12]	DDR3	O
BJ30	SA_MA[7]	DDR3	O
BJ38	SA_DQ[71]	DDR3	I/O
BJ40	SA_DQ[32]	DDR3	I/O
BJ47	SA_CS#[1]	DDR3	O
BJ48	SA_DQ[45]	DDR3	I/O
BJ55	SA_DQ[43]	DDR3	I/O
BJ57	SA_DQ[53]	DDR3	I/O
BJ61	SA_DQ[51]	DDR3	I/O
BJ63	SA_DQ[56]	DDR3	I/O
BJ64	VSS	GND	
BJ66	SA_DQ[60]	DDR3	I/O
BJ69	SB_DQS[7]	DDR3	I/O
BJ71	SB_DQ[56]	DDR3	I/O
BK2	SB_DQ[13]	DDR3	I/O
BK5	SA_DM[1]	DDR3	O
BK7	SA_DQ[14]	DDR3	I/O
BK9	SA_DQ[21]	DDR3	I/O
BK10	VSS	GND	
BK15	SA_DQ[22]	DDR3	I/O
BK17	SA_DQ[23]	DDR3	I/O
BK24	SA_CKE[1]	DDR3	O
BK25	SA_DQ[26]	DDR3	I/O
BK32	SA_MA[6]	DDR3	O
BK34	VSS	GND	
BK36	SA_CK#[1]	DDR3	O
BK43	SA_CAS#	DDR3	O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BK44	SA_DQS[4]	DDR3	I/O
BK51	SA_DQS#[5]	DDR3	I/O
BK53	VSS	GND	
BK60	VSS	GND	
BK61	SA_DQ[55]	DDR3	I/O
BK63	VSS	GND	
BK64	SA_DQ[54]	DDR3	I/O
BK67	SB_DQ[61]	DDR3	I/O
BK70	SB_DQ[60]	DDR3	I/O
BL1	VSS	GND	
BL4	SB_DM[1]	DDR3	O
BL13	SA_DQS[2]	DDR3	I/O
BL20	VSS	GND	
BL21	SA_DQS#[3]	DDR3	I/O
BL28	VSS	GND	
BL30	SB_DQ[70]	DDR3	I/O
BL38	SA_RAS#	DDR3	O
BL40	VSS	GND	
BL47	SA_ODT[1]	DDR3	O
BL48	VSS	GND	
BL55	VSS	GND	
BL57	VSS	GND	
BL69	SB_DQ[55]	DDR3	I/O
BL71	VSS	GND	
BM3	SB_DQS[1]	DDR3	I/O
BM15	SA_DM[2]	DDR3	O
BM17	VSS	GND	
BM24	VSS	GND	
BM25	SB_DQ[67]	DDR3	I/O
BM32	VSS	GND	
BM34	SA_CK[0]	DDR3	O
BM43	SA_DQ[33]	DDR3	I/O
BM44	VSS	GND	
BM51	VSS	GND	
BM53	SA_DQ[46]	DDR3	I/O
BM60	SA_DQS[6]	DDR3	I/O
BM70	VSS	GND	

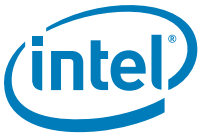


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BN1	VSS	GND	
BN4	SB_DQS#[1]	DDR3	I/O
BN6	VSS	GND	
BN8	SA_DQ[15]	DDR3	I/O
BN9	SA_DQ[17]	DDR3	I/O
BN11	SA_DQ[20]	DDR3	I/O
BN13	SA_DQS#[2]	DDR3	I/O
BN17	SA_DQ[16]	DDR3	I/O
BN20	SA_DQ[24]	DDR3	I/O
BN21	SA_DQS[3]	DDR3	I/O
BN24	SA_DM[3]	DDR3	O
BN25	SA_MA[15]	DDR3	O
BN28	SA_MA[14]	DDR3	O
BN30	SA_MA[8]	DDR3	O
BN32	SA_MA[5]	DDR3	O
BN38	SB_DQ[68]	DDR3	I/O
BN40	SA_DQ[36]	DDR3	I/O
BN44	SA_DQ[38]	DDR3	I/O
BN47	SA_DQ[39]	DDR3	I/O
BN48	SA_DQ[40]	DDR3	I/O
BN51	SA_DQ[41]	DDR3	I/O
BN55	SA_DQ[47]	DDR3	I/O
BN57	SA_DQ[49]	DDR3	I/O
BN62	SA_DM[6]	DDR3	O
BN64	VSS	GND	
BN65	SA_DQ[50]	DDR3	I/O
BN68	SB_DQ[54]	DDR3	I/O
BN71	VSS	GND	
BP12	SB_DQ[21]	DDR3	I/O
BP15	SB_DQ[24]	DDR3	I/O
BP19	SB_DQ[28]	DDR3	I/O
BP22	SB_DM[3]	DDR3	O
BP26	SB_MA[7]	DDR3	O
BP30	SB_MA[1]	DDR3	O
BP33	SA_MA[1]	DDR3	O
BP35	SA_CK#[0]	DDR3	O
BP39	SM_RCOMP[1]	Analog	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BP42	VSS	GND	
BP46	SB_CS#[0]	DDR3	O
BP49	SB_DQ[35]	DDR3	I/O
BP53	SB_DQ[40]	DDR3	I/O
BP56	SB_DQ[45]	DDR3	I/O
BP58	SA_DQS#[6]	DDR3	I/O
BP60	SB_DQ[49]	DDR3	I/O
BR1	DC_TEST_BR1		
BR3	VSS	GND	
BR5	RSVD_NCTF		
BR6	SB_DQ[10]	DDR3	I/O
BR8	SB_DQ[11]	DDR3	I/O
BR10	SB_DQ[16]	DDR3	I/O
BR62	SB_DQ[52]	DDR3	I/O
BR64	SB_DQ[51]	DDR3	I/O
BR66	SB_DQ[50]	DDR3	I/O
BR68	VSS	GND	
BR69	VSS	GND	
BR71	DC_TEST_BR71		
BT1	DC_TEST_BT1		
BT3	DC_TEST_BT3		
BT5	RSVD_NCTF		
BT12	SB_DQ[17]	DDR3	I/O
BT13	SB_DM[2]	DDR3	O
BT15	SB_DQ[18]	DDR3	I/O
BT17	SB_DQS[3]	DDR3	I/O
BT19	SB_DQS#[3]	DDR3	I/O
BT20	SB_DQ[31]	DDR3	I/O
BT22	SB_DQ[27]	DDR3	I/O
BT24	SB_CKE[1]	DDR3	O
BT26	SB_CKE[0]	DDR3	O
BT27	SB_MA[9]	DDR3	O
BT29	SB_MA[12]	DDR3	O
BT31	SB_MA[6]	DDR3	O
BT33	SB_MA[5]	DDR3	O
BT34	SB_MA[0]	DDR3	O
BT36	SA_MA[0]	DDR3	O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BT38	SA_BS[0]	DDR3	O
BT40	SB_RAS#	DDR3	O
BT41	SB_WE#	DDR3	O
BT43	SB_CS#[1]	DDR3	O
BT45	SB_MA[13]	DDR3	O
BT47	SB_DQ[36]	DDR3	I/O
BT48	SB_DQ[32]	DDR3	I/O
BT50	SB_DQS#[4]	DDR3	I/O
BT52	SB_DQS[4]	DDR3	I/O
BT54	SB_DQ[38]	DDR3	I/O
BT55	SB_DQ[44]	DDR3	I/O
BT57	SB_DQ[43]	DDR3	I/O
BT59	SB_DQ[42]	DDR3	I/O
BT61	SB_DQ[53]	DDR3	I/O
BT68	VSS	GND	
BT69	DC_TEST_BT69		
BT71	DC_TEST_BT71		
BU7	VSS	GND	
BU9	SB_DQ[14]	DDR3	I/O
BU11	VSS	GND	
BU12	SB_DQS#[2]	DDR3	I/O
BU14	VSS	GND	
BU16	SB_DQ[23]	DDR3	I/O
BU18	VSS	GND	
BU19	SB_DQ[25]	DDR3	I/O
BU21	VSS	GND	
BU23	SB_MA[15]	DDR3	O
BU25	VSS	GND	
BU26	SB_MA[11]	DDR3	O
BU28	SB_DQ[71]	DDR3	I/O
BU30	SB_MA[3]	DDR3	O
BU32	VSS	GND	
BU33	SB_CK[0]	DDR3	O
BU35	SA_DQ[67]	DDR3	I/O
BU37	VSS	GND	
BU39	SB_CK#[1]	DDR3	O
BU40	SA_DQ[66]	DDR3	I/O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BU42	SB_MA[10]	DDR3	O
BU44	VSS	GND	
BU46	SB_CAS#	DDR3	O
BU48	VSS	GND	
BU49	SB_ODT[1]	DDR3	O
BU51	VSS	GND	
BU53	SB_DQ[41]	DDR3	I/O
BU55	VSS	GND	
BU56	SB_DQS[5]	DDR3	I/O
BU58	VSS	GND	
BU60	SB_DQ[46]	DDR3	I/O
BU62	VSS	GND	
BU63	SB_DQS#[6]	DDR3	I/O
BU65	SB_DM[6]	DDR3	O
BV1	DC_TEST_BV1		
BV3	DC_TEST_BV3		
BV5	DC_TEST_BV5		
BV6	RSVD_NCTF		
BV8	RSVD_NCTF		
BV10	SB_DQ[15]	DDR3	I/O
BV12	SB_DQ[20]	DDR3	I/O
BV13	SB_DQS[2]	DDR3	I/O
BV15	SB_DQ[19]	DDR3	I/O
BV17	SB_DQ[22]	DDR3	I/O
BV19	SB_DQ[29]	DDR3	I/O
BV20	SB_DQ[30]	DDR3	I/O
BV22	SB_DQ[26]	DDR3	I/O
BV24	SB_BS[2]	DDR3	O
BV26	SB_MA[14]	DDR3	O
BV27	SB_MA[8]	DDR3	O
BV29	SB_MA[2]	DDR3	O
BV31	SB_MA[4]	DDR3	O
BV33	SM_RCOMP[0]	Analog	I
BV34	SB_CK#[0]	DDR3	O
BV36	SA_MA[2]	DDR3	O
BV38	SB_CK[1]	DDR3	O
BV40	SM_RCOMP[2]	Analog	I

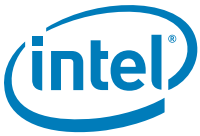


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BV41	SB_BS[0]	DDR3	O
BV43	SB_BS[1]	DDR3	O
BV45	SB_ODT[0]	DDR3	O
BV47	SB_DM[4]	DDR3	O
BV48	SB_DQ[33]	DDR3	I/O
BV50	SB_DQ[34]	DDR3	I/O
BV52	SB_DQ[37]	DDR3	I/O
BV54	SB_DQ[39]	DDR3	I/O
BV55	SB_DQS#[5]	DDR3	I/O
BV57	SB_DM[5]	DDR3	O
BV59	SB_DQ[47]	DDR3	I/O
BV61	SB_DQ[48]	DDR3	I/O
BV62	SB_DQS[6]	DDR3	I/O
BV64	VSS	GND	
BV66	VSS	GND	
BV68	DC_TEST_BV68		
BV69	DC_TEST_BV69		
BV71	DC_TEST_BV71		
C3	DC_TEST_C3		
C5	RSVD_NCTF		
C68	VSS	GND	
C69	DC_TEST_C69		
C71	DC_TEST_C71		
D6	VSS	GND	
D8	RSVD		
D10	VSS	GND	
D12	PEG_RCOMPO	Analog	I
D13	VSS	GND	
D15	PEG_RX[15]	PCIe	I
D17	VSS	GND	
D19	PEG_RX#[13]	PCIe	I
D20	VSS	GND	
D22	PEG_RX#[11]	PCIe	I
D24	VSS	GND	
D26	PEG_RX#[9]	PCIe	I
D27	VSS	GND	
D29	PEG_RX#[7]	PCIe	I

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
D31	VSS	GND	
D33	PEG_TX[10]	PCIe	O
D34	VSS	GND	
D36	PEG_TX[7]	PCIe	O
D38	VSS	GND	
D40	PEG_TX#[3]	PCIe	O
D41	VSS	GND	
D43	VCC	REF	
D45	VCC	REF	
D47	VCC	REF	
D48	VCC	REF	
D50	VCC	REF	
D52	VCC	REF	
D54	VCC	REF	
D55	VCC	REF	
D57	VCC	REF	
D59	VCC	REF	
D61	VID[1]	CMOS	O
D62	VID[2]	CMOS	O
D64	CSC[2]/VID[5]	CMOS	I/O
D66	VID[6]	CMOS	O
E1	DC_TEST_E1		
E3	RSVD_NCTF		
E5	VSS	GND	
E12	VSS	GND	
E16	VSS	GND	
E30	VSS	GND	
E33	VSS	GND	
E37	VSS	GND	
E42	VCC	REF	
E46	VCC	REF	
E50	VCC	REF	
E53	VCC	REF	
E57	VCC	REF	
E60	VCC	REF	
E68	VSS	GND	
E69	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
E71	DC_TEST_E71		
F1	RSVD_NCTF		
F4	VSS	GND	
F7	DMI_RX#[0]	DMI	I
F9	DMI_RX[0]	DMI	I
F10	DMI_TX#[3]	DMI	O
F20	VSS	GND	
F21	PEG_TX[14]	PCIe	O
F28	VSS	GND	
F40	PEG_RX[0]	PCIe	I
F47	VSS	GND	
F48	VSS	GND	
F55	VCC	REF	
F61	VSS	GND	
F63	VSS_SENSE	Analog	O
F64	VCC_SENSE	Analog	O
F66	PROC_DPRSLPVR	CMOS	O
F68	PSI#	Async CMOS	O
F71	VSS	GND	
G3	RSTIN#	CMOS	I
G13	DMI_TX[2]	DMI	O
G15	VSS	GND	
G17	DMI_TX[0]	DMI	O
G20	VSS	GND	
G21	PEG_TX#[14]	PCIe	O
G24	VSS	GND	
G25	PEG_RX[5]	PCIe	I
G28	PEG_RX#[4]	PCIe	I
G30	VSS	GND	
G32	PEG_TX#[5]	PCIe	O
G34	PEG_RX[2]	PCIe	I
G38	PEG_RX#[1]	PCIe	I
G40	PEG_RX#[0]	PCIe	I
G43	VSS	GND	
G44	VCC	REF	
G47	VSS	GND	
G48	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
G51	VCC	REF	
G53	VSS	GND	
G55	VCC	REF	
G57	VSS	GND	
G60	VCC	REF	
G70	VSS	GND	
H1	VSS	GND	
H15	VTTPWRGOOD	Async CMOS	I
H17	DMI_TX#[0]	DMI	O
H24	PEG_RX#[6]	PCIe	I
H25	PEG_RX#[5]	PCIe	I
H32	PEG_TX[5]	PCIe	O
H34	PEG_RX#[2]	PCIe	I
H36	VSS	GND	
H43	VSS	GND	
H44	VCC	REF	
H51	VCC	REF	
H53	VSS	GND	
H60	VCC	REF	
H71	VSS	GND	
J11	DMI_TX[3]	DMI	O
J13	DMI_TX#[2]	DMI	O
J2	DMI_RX[3]	DMI	I
J4	DMI_RX#[3]	DMI	I
J6	DMI_RX[1]	DMI	I
J8	DMI_RX#[1]	DMI	I
J9	VSS	GND	
J20	PEG_TX#[15]	PCIe	O
J21	PEG_CLK#	DIFF CLK	I
J28	PEG_RX[4]	PCIe	I
J30	PEG_TX[8]	PCIe	O
J38	PEG_RX[1]	PCIe	I
J40	VSS	GND	
J47	VSS	GND	
J48	VSS	GND	
J55	VCC	REF	
J57	VSS	GND	

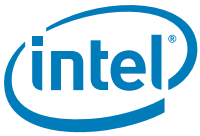


Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
J62	BPM#[2]	GTL	I/O
J64	BPM#[5]	GTL	I/O
J65	VSS	GND	
J67	BPM#[1]	GTL	I/O
J69	BPM#[0]	GTL	I/O
J70	BCLK_ITP #	DIFF CLK	O
K1	FDI_TX[0]	FDI	O
K4	VSS	GND	
K6	VSS	GND	
K8	DMI_RX#[2]	DMI	I
K9	DMI_RX[2]	DMI	I
K11	VSS	GND	
K15	DMI_TX#[1]	DMI	O
K17	VSS	GND	
K24	PEG_RX[6]	PCIe	I
K25	VSS	GND	
K32	VSS	GND	
K34	VSS	GND	
K36	VSS	GND	
K43	VSS	GND	
K44	VCC	REF	
K51	VCC	REF	
K53	VSS	GND	
K60	VCC	REF	
K62	BPM#[4]	GTL	I/O
K64	VSS	GND	
K65	BPM#[3]	GTL	I/O
K69	BPM#[6]	GTL	I/O
K71	BCLK_ITP	DIFF CLK	O
L2	FDI_TX#[0]	FDI	O
L13	VSS	GND	
L20	PEG_TX[15]	PCIe	O
L21	PEG_CLK	Diff CLK	I
L28	PEG_TX#[11]	PCIe	O
L30	PEG_TX#[8]	PCIe	O
L38	PEG_TX#[1]	PCIe	O
L40	PEG_TX[0]	PCIe	O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
L47	VSS	GND	
L48	VSS	GND	
L55	VCC	REF	
L57	VSS	GND	
L70	VSS	GND	
M1	VSS	GND	
M4	FDI_TX#[2]	FDI	O
M15	DMI_TX[1]	DMI	O
M17	PM_SYNC	CMOS	I
M24	PEG_TX#[13]	PCIe	O
M25	PEG_TX[12]	PCIe	O
M32	PEG_TX#[2]	PCIe	O
M34	PEG_RX[3]	PCIe	I
M36	VSS	GND	
M42	VSS	GND	
M44	VCC	REF	
M51	VCC	REF	
M53	VSS	GND	
M60	VCC	REF	
M69	BPM#[7]	GTL	I/O
M71	PROC_DETECT		
N2	FDI_TX[2]	FDI	O
N5	FDI_TX[1]	FDI	O
N7	FDI_TX#[1]	FDI	O
N9	FDI_TX[4]	FDI	O
N10	FDI_TX#[4]	FDI	O
N13	VTT_SENSE	Analog	O
N15	VSS	GND	
N17	THERMTRIP#	Async GTL	O
N19	PECI	Async	I/O
N21	VSS	GND	
N24	PEG_TX[13]	PCIe	O
N26	PEG_TX#[12]	PCIe	O
N28	PEG_TX[11]	PCIe	O
N30	VSS	GND	
N32	PEG_TX[2]	PCIe	O

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
N38	PEG_TX[1]	PCIe	O
N40	PEG_TX#[0]	PCIe	O
N42	VCC	REF	
N44	VCC	REF	
N46	VSS	GND	
N48	VCC	REF	
N50	VSS	GND	
N51	VCC	REF	
N53	VSS	GND	
N55	VCC	REF	
N57	VSS	GND	
N61	CATERR#	GTL	I/O
N63	VSS	GND	
N65	TMS	CMOS	I
N67	PROCHOT#	Async GTL	I/O
N70	RESET_OBS#	Async CMOS	O
P1	FDI_TX#[3]	FDI	O
P4	VSS	GND	
P34	PEG_RX#[3]	PCIe	I
P60	VCC	REF	
P69	TRST#	CMOS	I
P71	TDI_M	CMOS	I
R2	FDI_TX[3]	FDI	O
R5	VSS	GND	
R7	FDI_TX#[5]	FDI	O
R8	FDI_TX[5]	FDI	O
R12	VSS_SENSE_VTT	Analog	O
R14	VSS	GND	
R15	VTT1	REF	
R17	VTT1	REF	
R19	VTT1	REF	
R21	VTT1	REF	
R23	VTT0	REF	
R24	VTT0	REF	
R26	VTT0	REF	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
R28	VTT0	REF	
R30	VTT0	REF	
R32	VTT0	REF	
R33	VTT0	REF	
R35	VTT0	REF	
R37	VCCPLL	REF	
R39	VCCPLL	REF	
R41	VCC	REF	
R42	VSS	GND	
R44	VCC	REF	
R46	VSS	GND	
R48	VCC	REF	
R50	VSS	GND	
R51	VCC	REF	
R53	VSS	GND	
R55	VCC	REF	
R57	VSS	GND	
R59	VCAP2	PWR	
R60	VCAP2	PWR	
R62	VSS	GND	
R64	RSVD		
R66	RSVD		
R70	VSS	GND	
T1	VSS	GND	
T2	RSVD		
T4	RSVD		
U6	FDI_TX[6]	FDI	O
U7	FDI_TX#[6]	FDI	O
U9	VSS	GND	
T67	TCK	CMOS	I
T69	TDI	CMOS	I
T70	TDO_M	CMOS	O
T71	TDO	CMOS	O
U1	RSVD		
U4	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
U12	VTT1	REF	
U14	VTT1	REF	
U15	VTT1	REF	
U17	VTT1	REF	
U19	VTT1	REF	
U21	VTT1	REF	
U23	VTT0	REF	
U24	VTT0	REF	
U26	VTT0	REF	
U28	VTT0	REF	
U30	VTT0	REF	
U32	VTT0	REF	
U33	VTT0	REF	
U35	VTT0	REF	
U37	VCCPLL	REF	
U39	VSS	GND	
U41	VCC	REF	
U42	VSS	GND	
U44	VCC	REF	
U46	VSS	GND	
U48	VCC	REF	
U50	VSS	GND	
U51	VCC	REF	
U53	VSS	GND	
U55	VCC	REF	
U57	VSS	GND	
U59	VCAP2	PWR	
U60	VCAP2	PWR	
U62	VSS	GND	
U64	VSS	GND	
U69	PREQ#	Async GTL	I
U71	PRDY#	Async GTL	O
V2	RSVD		
V70	VSS	GND	
W1	VSS	GND	

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
W4	DPLL_REF_SSCLK#	DIFF CLK	I
W6	VSS	GND	
W8	FDI_TX#[7]	FDI	O
W10	FDI_TX[7]	FDI	O
W12	VTT1	REF	
W14	VTT1	REF	
W15	VTT1	REF	
W17	VTT1	REF	
W19	VTT1	REF	
W21	VTT1	REF	
W23	VTT0	REF	
W24	VTT0	REF	
W26	VTT0	REF	
W28	VTT0	REF	
W30	VTT0	REF	
W32	VTT0	REF	
W33	VTT0	REF	
W35	VTT0	REF	
W37	VCCPLL	REF	
W39	VCCPLL	REF	
W41	VCC	REF	
W42	VSS	GND	
W44	VCC	REF	
W46	VSS	GND	
W48	VCC	REF	
W50	VSS	GND	
W51	VCC	REF	
W53	VSS	GND	
W55	VCC	REF	
W57	VSS	GND	
W59	VCAP2	PWR	
W60	VCAP2	PWR	
W62	VSS	GND	
W64	RSVD		
W66	RSVD		

Table 13. Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
W69	VSS	GND	
W71	DBR#		O
Y2	DPLL_REF_SSCLK	DIFF CLK	I
Y67	VCCPWRGOOD_0	Async CMOS	I
Y70	TAPPWRGOOD	Async CMOS	O

§ §

6 Processor Configuration Registers

This chapter is an Addendum to the *Intel® Core™ i7-600, i5-500 and i3-300 Mobile Processor Series Datasheet.* Contained in this chapter is any register information that is specific to the Intel® Core™ i7-660UE, i7-620LE/UE, i7-610E, i5-520E, i3-330E and Intel® Celeron® Processor P4505, U3405 Series. For all other register information not contained in this chapter please refer to the *Intel® Core™ i7-600, i5-500 and i3-300 Mobile Processor Series Datasheet*.

6.1 Register Terminology

The following table shows the register-related terminology that is used in this document.

Table 14. Register Terminology (Sheet 1 of 2)

Item	Description
RO	**Read Only bit(s).** Writes to these bits have no effect. These are static values only.
RO-V	**Read Only/Volatile bit(s).** Writes to these bits have no effect. These are status bits only. The value to be read may change based on internal events.
RO-V-S	**Read Only/Volatile/Sticky bit(s).** Writes to these bits have no effect. These are status bits only. The value to be read may change based on internal events. Bits are not returned to their default values by "warm" reset, but is reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the *PCI Express Base Specification*).
AF	**Atomic Flag bit(s).** The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect. Conceptually, this is "Read to Set, Write 1 to Clear."
RW	**Read/Write bit(s).** These bits can be read and written by software. Hardware may only change the state of this bit by reset.
RW1C	**Read/Write 1 to Clear bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to '0') the corresponding bit(s) and a write of 0 has no effect.
RW1C-L-S	**Read/Write 1 to Clear/Lockable/Sticky bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to '0') the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but is reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express Base spec). Additionally there is a Key bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only/Volatile).

Table 14. Register Terminology (Sheet 2 of 2)

Item	Description
RW1C-S	**Read / Write 1 to Clear / Sticky bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but is reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express Base spec).
RW-K	**Read / Write / Key bit(s).** These bits can be read and written by software. Additionally this bit, when set, prohibits some other target bit field from being writable (bit fields become Read Only).
RW-L	**Read / Write / Lockable bit(s).** These bits can be read and written by software. Additionally there is a Key bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only).
RW-L-K	**Read / Write / Lockable / Key bit(s).** These bits can be read and written by software. This bit, when set, prohibits some other bit field(s) from being writable (bit fields become Read Only). Additionally there is a Key bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only). Conceptually, this may be a cascaded lock, or it may be self-locking when in its non-default state. When self-locking, it differs from RW-O in that writing back the default value will not set the lock.
RW-V	**Write / Volatile bit(s).** These bits can be read and written by software. Hardware may set or clear the bit based on internal events, possibly sooner than any subsequent software read could retrieve the value written.
RW-V-L	**Read / Write / Volatile / Lockable bit(s).** These bits can be read and written by software. Hardware may set or clear the bit based upon internal events, possibly sooner than any subsequent software read could retrieve the value written Additionally there is a bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only).
RW-V-L-S	**Read / Write / Volatile / Lockable / Sticky bit(s).** These bits can be read and written by software. Hardware may set or clear the bit based upon internal events, possibly sooner than any subsequent software read could retrieve the value written Additionally there is a bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only). These bits return to their default values on cold reset.
RW-S	**Read / Write / Sticky bit(s).** These bits can be read and written by software. Bits are not returned to their default values by “warm” reset, but will return to default values with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
RW-O	**Read / Write Once bit(s).** Reads prior to the first write return the default value. The first write after warm reset stores any value written. Any subsequent write to this bit field is ignored. All subsequent reads return the first value written. The value returns to default on warm reset. If there are multiple RW-O or RW-O-S fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.
RW-O-S	**Read / Write Once / Sticky bit(s).** Reads prior to the first write return the default value. The first write after cold reset stores any value written. Any subsequent write to this bit field is ignored. All subsequent reads return the first value written. The value returns to default on cold reset. If there are multiple RW-O or RW-O-S fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.
W	**Write-only.** These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.
W1C	**Write 1 to Clear-only.** These bits may be cleared by software by writing a 1. Writing a 0 has no effect. The state of the bits cannot be read directly. The states of such bits are tracked outside the CPU and all read transactions to the address of such bits are routed to the other agent. Write transactions to these bits go to both agents.

6.1.1 DEVEN - Device Enable

B/D/F/Type: 0/0/0/PCI
Address Offset: 54-57h
Default Value: 0000010Bh
Access: RW-L; RO; RW
Size: 32 bits
BIOS Optimal Default 000000h

Allows for enabling/disabling of PCI devices and functions that are within the processor. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Table 15. DEVEN - Device Enable Register

Bit	Access	Default Value	RST/ PWR	Description
31:15	RO	0h		**Reserved**
14	RW-L	0b	Core	**Reserved**
13	RW-L	0b	Core	**PEG1 Enable (D6EN)** 0 = Bus 0 Device 6 Function 0 is disabled and hidden. 1 = Bus 0 Device 6 Function 0 is enabled and visible.
12:12	RO	0h		**Reserved**
11	RW-L	0b	Core	**Reserved**
10	RW-L	0b	Core	**Reserved**
9:9	RO	0h		**Reserved**
8	RW-L	1b	Core	**Reserved**
7:4	RO	0h		**Reserved**
3	RW-L	1b	Core	**Internal Graphics Engine Function 0 (D2F0EN)** 0 = Bus 0 Device 2 Function 0 is disabled and hidden 1 = Bus 0 Device 2 Function 0 is enabled and visible
2:2	RO	0h		**Reserved**
1	RW-L	1b	Core	**PCI Express Port (D1EN)** 0 = Bus 0 Device 1 Function 0 is disabled and hidden. 1 = Bus 0 Device 1 Function 0 is enabled and visible.
0	RO	1b	Core	**Host Bridge (D0EN)** Bus 0 Device 0 Function 0 may not be disabled and is therefore hard wired to 1.

6.1.2 ERRSTS - Error Status

B/D/F/Type: 0/0/0/PCI

Address Offset: C8-C9h

Default Value: 0000h

Access: RO; RW1C-S;

Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a '1' to it.

Table 16. Error Status Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:13	RO	000b	Core	**Reserved**
12	RW1C-S	0b	Core	**Processor Software Generated Event for SMI (GSGESMI):** This indicates the source of the SMI was a Device 2 Software Event.
11	RW1C-S	0b	Core	**Processor Thermal Sensor Event for SMI / SCI / SERR (GTSE):** Indicates that a Processor Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event
10	RO	0b	Core	**Reserved**
9	RW1C-S	0b	Core	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the Processor has detected a lock operation to memory space that did not map into DRAM
8	RO	0b	Core	**Reserved**
7	RW1C-S	0b	Core	**DRAM Throttle Flag (DTF):** 1: Indicates that a DRAM Throttling condition occurred. 0: Software has cleared this flag since the most recent throttling event.
6:2	RO	00h	Core	Reserved

Table 16. Error Status Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
1	RW1C-S	0b	Core	**Multiple-bit DRAM ECC Error Flag (DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set, the column, row, bank, and rank that caused the error, and the error syndrome, are logged in the ECC Error Log register in the channel where the error occurred. Once this bit is set, the CxECCERRLOG fields are locked until the CPU clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for a Single-bit or a Multiple-bit error. This bit is reset on PWROK.
0	RW1C-S	0b	Core	**Single-bit DRAM ECC Error Flag (DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was returned to the requesting agent. When this bit is set the column, row, bank, and rank where the error occurred and the syndrome of the error are logged in the ECC Error Log register in the channel where the error occurred. Once this bit is set the CxECCERRLOG fields are locked to further single-bit error updates until the CPU clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the CxECCERRLOG fields with the multiple-bit error signature and the DMERR bit will also be set. A single bit error that occurs after a multibit error will set this bit but will not overwrite the other fields. This bit is reset on PWROK.

6.1.3 ERRCMD - Error Command

B/D/F/Type: 0/0/0/PCI

Address Offset: CA-CBh

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

This register controls the Processor responses to various system errors. Since the Processor does not have an SERRB signal, SERR messages are passed from the Processor to the PCH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Table 17. Error Command Registers

Bit	Access	Default Value	RST / PWR	Description
15:12	RO	000b	Core	**Reserved**
11	RW	0b	Core	**SERR on Processor Thermal Sensor Event (TSESERR):** 1: The Processor generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0: Reporting of this condition via SERR messaging is disabled.
10	RO	0b	Core	**Reserved**
9	RW	0b	Core	**SERR on LOCK to non-DRAM Memory (LCKERR):** 1: The Processor will generate a DMI SERR special cycle whenever a CPU lock cycle is detected that does not hit DRAM. 0: Reporting of this condition via SERR messaging is disabled
8	RW	0b	Core	**Reserved**
7	RW	0b	Core	**SERR on DRAM Throttle Condition (ERR):** 0 = Reporting of this condition via SERR messaging is disabled. 1 = The memory controller generates a DMI SERR special cycle when a DRAM Read or Write Throttle condition occurs.
6:2	RO	00h	Core	**Reserved**
1	RW	0b	Core	**SERR Multiple-Bit DRAM ECC Error (DMERR):** 1: The Processor generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	RW	0b	Core	**SERR on Single-bit ECC Error (DSERR):** 1: The Processor generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0: Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.

6.1.4 SMICMD - SMI Command

B/D/F/Type: 0/0/0/PCI

Address Offset: CC-CDh

Default Value: 0000h

Access: RO, RW;

Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively. Note that one and only one message type can be enabled.

Table 18. SMI Command Registers

Bit	Access	Default Value	RST/ PWR	Description
15:12	RO	0h	Core	**Reserved**
11	RW	0b	Core	**SMI on Processor Thermal Sensor Trip (TSTSMI):** 1: A SMI DMI special cycle is generated by Processor when the thermal sensor trip requires an SMI. A thermal sensor trip point cannot generate more than one special cycle. 0: Reporting of this condition via SMI messaging is disabled.
10:2	RO	000h	Core	**Reserved**
1	RW	0b	Core	**SMI on Multiple-Bit DRAM ECC Error (DMESMI):** 1: The Processor generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	RW	0b	Core	**SMI on Single-bit ECC Error (DSESMI):** 1: The Processor generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.

6.1.5 C0WRDATACTRL - Channel 0 Write Data Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 24D-24Fh

Default Value: 004111h

Access: RW

Size: 24 bits

BIOS Optimal Default 00h

Table 19. Channel 0 Write Data Control Registers

Bit	Access	Default Value	RST/ PWR	Description
23:16	RW	00h	Core	**ECC bit invert vector (C0sd_cr_eccbitinv):** This vector operates individually for every ECC bit in the selected 64b ECC block, during write to DRAM. For all k between 0 and 7, when bit(k) is set to 1, the value for the k ECC bit (which corresponds with k data byte lane) is inverted. Otherwise, the value for the k ECC bit is not affected.
15	RW	0b	Core	**ECC Diagnostic Enable (C0sd_cr_eccdiagen):** 1: The ECC bit invert vector is used to invert selected ECC bits, during writes to DRAM. 0: The diagnostic feature is turned off.
14:0	RW	4110h	Core	**Reserved**

6.1.6 COECCERRLOG - Channel 0 ECC Error Log

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 280-287h

Default Value: 0000000000000000h

Access: RO-P; RO

Size: 64 bits

This register is used to store the error status information in ECC enabled configurations, along with the error syndrome and the rank/bank/row/column address information of the address block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the address fields represent the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and doesn't change as a result of a new error until the error flag is cleared by software. Same is the case with error syndrome field, but the following priority needs to be followed if more than one error occurs on one or more of the 4 QWs. MERR on QW0 MERR on QW1 MERR on QW2 MERR on QW3 CERR on QW0 CERR on QW1 CERR on QW2 CERR on QW3.

Table 20. Channel 0 ECC Error Registers (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
63:48	RO-P	0000h	Core	**Error Column Address (ERRCOL):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
47:32	RO-P	0000h	Core	**Error Row Address (ERRROW):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred
31:29	RO-P	000b	Core	**Error Bank Address (ERRBANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred
28:27	RO-P	00b	Core	**Error Rank Address (ERRRANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
26:24	RO	000b	Core	**Reserved**
23:16	RO-P	00b	Core	**Error Syndrome (ERRSYND):** Syndrome that describes the set of bits associated with the first failing quadword
15:2	RO	0000h	Core	**Reserved**
1	RO-P	0b	Core	**Multiple Bit Error Status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This bit is cleared when it receives an indication that the CPU has cleared the corresponding bit in the ERRSTS register.

Table 20. Channel 0 ECC Error Registers (Sheet 2 of 2)

Bit	Access	Default Value	RST / PWR	Description
0	RO-P	0b	Core	**Correctable Error Status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. But, a multiple bit error that occurs after this bit is set will over-write the address/error syndrome info. This bit is cleared when it receives an indication that the CPU has cleared the corresponding bit in the ERRSTS register.

6.1.7 C1WRDATACTRL - Channel 1 Write Data Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 64D-64Fh

Default Value: 004111h

Access: RW

Size: 24 bits

BIOS Optimal Default 00h

Table 21. Channel 1 Write Data Control Registers

Bit	Access	Default Value	RST/ PWR	Description
23:16	RW	00h	Core	**ECC bit invert vector (C1sd_cr_eccbitinv):** This vector operates individually for every ECC bit in the selected 64b ECC block, during write to DRAM. For all k between 0 and 7, when bit(k) is set to 1, the value for the k ECC bit (which corresponds with k data byte lane) is inverted. Otherwise, the value for the k ECC bit is not affected.
15	RW	0b	Core	**ECC Diagnostic Enable (C1sd_cr_eccdiagen):** 1: The ECC bit invert vector is used to invert selected ECC bits, during writes to DRAM. 0: The diagnostic feature is turned off.
14:0	RW	4110h	Core	**Reserved**

6.1.8 C1ECCERRLOG - Channel 1 ECC Error Log

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 680 -687h

Default Value: 0000000000000000h

Access: RO; RO-V-S

Size: 64 bits

This register is used to store the error status information in ECC enabled configurations, along with the error syndrome and the rank/bank/row/column address information of the address block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the address fields represent the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and doesn't change as a result of a new error until the error flag is cleared by software. Same is the case with error syndrome field, but the following priority needs to be followed if more than one error occurs on one or more of the 4 QWs. MERR on QW0 MERR on QW1 MERR on QW2 MERR on QW3 CERR on QW0 CERR on QW1 CERR on QW2 CERR on QW3.

Table 22. Channel 1 ECC Error Registers

Bit	Access	Default Value	RST/ PWR	Description
63:48	RO-V-S	0000h	Core	**Error Column Address (ERRCOL):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
47:32	RO-V-S	0000h	Core	**Error Row Address (ERRROW):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred
31:29	RO-V-S	000b	Core	**Error Bank Address (ERRBANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred
28:27	RO-V-S	00b	Core	**Error Rank Address (ERRRANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
26:24	RO	000b	Core	**Reserved**
23:16	RO-V-S	00b	Core	**Error Syndrome (ERRSYND):** Syndrome that describes the set of bits associated with the first failing quadword
15:2	RO	0000h	Core	**Reserved**
1	RO-V-S	0b	Core	**Multiple Bit Error Status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This bit is cleared when it receives an indication that the CPU has cleared the corresponding bit in the ERRSTS register.
0	RO-V-S	0b	Core	**Correctable Error Status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. But, a multiple bit error that occurs after this bit is set will over-write the address/error syndrome info. This bit is cleared when it receives an indication that the CPU has cleared the corresponding bit in the ERRSTS register.

6.2 PCI Device 6

Device 6 contains the controls associated with the PCI Express x8 port (Port 1) that is enabled with bifurcation of the PCI Express x16 root port.

Warning: When reading the PCI Express “conceptual” registers such as this, you may not get a valid value unless the register value is stable.

The PCI Express based specification defines two types of reserved bits.

Reserved and Preserved:

1. Reserved for future RW implementations; software must preserve value read for writes to bits.
2. Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

It is important to note that most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 23. PCI Device 6 Register (Sheet 1 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID6	0	1	8086h	RO
Device Identification	DID6	2	3	0047h	RO
PCI Command	PCICMD6	4	5	0000h	RO; RW
PCI Status	PCISTS6	6	7	0010h	RO; RWC
Revision Identification	RID6	8	8	10h	RO
Class Code	CC6	9	B	060400h	RO
Cache Line Size	CL6	C	C	00h	RW
Header Type	HDR6	E	E	01h	RO
Primary Bus Number	PBUSN6	18	18	00h	RO
Secondary Bus Number	SBUSN6	19	19	00h	RW
Subordinate Bus Number	SUBUSN6	1A	1A	00h	RW
I/O Base Address	IOBASE6	1C	1C	F0h	RO; RW
I/O Limit Address	IOLIMIT6	1D	1D	00h	RO; RW
Secondary Status	SSTS6	1E	1F	0000h	RWC; RO
Memory Base Address	MBASE6	20	21	FFF0h	RO; RW
Memory Limit Address	MLIMIT6	22	23	0000h	RO; RW
Prefetchable Memory Base Address	PMBASE6	24	25	FFF1h	RO; RW

Table 23. PCI Device 6 Register (Sheet 2 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Prefetchable Memory Limit Address	PMLIMIT6	26	27	0001h	RO; RW
Prefetchable Memory Base Address Upper	PMBASEU6	28	2B	00000000h	RW
Prefetchable Memory Limit Address Upper	PMLIMITU6	2C	2F	00000000h	RW
Capabilities Pointer	CAPPTR6	34	34	88h	RO
Interrupt Line	INTRLINE6	3C	3C	00h	RW
Interrupt Pin	INTRPIN6	3D	3D	01h	RO
Bridge Control	BCTRL6	3E	3F	0000h	RO; RW
Capabilities List Control	CAPL	7F	7F	02h	RO; RW
Power Management Capabilities	PM_CAPID6	80	83	C8039001h	RO
Power Management Control/Status	PM_CS6	84	87	00000008h	RO; RW-S; RW
Subsystem ID and Vendor ID Capabilities	SS_CAPID	88	8B	0000800Dh	RO
Subsystem ID and Subsystem Vendor ID	SS	8C	8F	00008086h	RW-O
Message Signaled Interrupts Capability ID	MSI_CAPID	90	91	A005h	RO
Message Control	MC	92	93	0000h	RO; RW
Message Address	MA	94	97	00000000h	RO; RW
Message Data	MD	98	99	0000h	RW
PCI Express-G Capability List	PEG_CAPL	A0	A1	0010h	RO
PCI Express-G Capabilities	PEG_CAP	A2	A3	0142h	RO; RW-O
Device Capabilities	DCAP	A4	A7	00008000h	RO
Device Control	DCTL	A8	A9	0000h	RO; RW
Device Status	DSTS	AA	AB	0000h	RO; RWC
Link Capabilities	LCAP	AC	AF	03214C81h	RO; RW-O
Link Control	LCTL	B0	B1	0000h	RO; RW; RW-SC
Link Status	LSTS	B2	B3	1000h	RWC; RO

Table 23. PCI Device 6 Register (Sheet 3 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Slot Capabilities	SLOTCAP	B4	B7	00040000h	RW-O; RO
Slot Control	SLOTCTL	B8	B9	0000h	RO; RW
Slot Status	SLOTSTS	BA	BB	0000h	RO; RWC
Root Control	RCTL	BC	BD	0000h	RO; RW
Root Status	RSTS	C0	C3	00000000h	RO; RWC
Link Control 2	LCTL2	D0	D1	0001h	RO; RW-S; RW
Link Status 2	LSTS2	D2	D3	0000h	RO
PCI Express-G Legacy Control	PEGLC	EC	EF	00000000h	RO; RW

6.2.1 VID6 - Vendor Identification

B/D/F/Type: 0/6/0/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identify any PCI device.

Table 24. VID6 - Vendor Identification Register

Bit	Access	Default Value	RST/ PWR	Description
15:0	RO	8086h	Core	**Vendor Identification (VID6)** PCI standard identification for Intel.

6.2.2 DID6 - Device Identification

B/D/F/Type: 0/6/0/PCI
Address Offset: 2-3h
Default Value: 0047h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Table 25. DID6 - Device Identification Register

Bit	Access	Default Value	RST/ PWR	Description
15:4	RO	004h	Core	**Device Identification Number (DID6(UB))** Identifier assigned to the processor Device 6 (virtual PCI-to-PCI bridge, PCI Express Graphics port).
3:2	RO	00b	Core	**Device Identification Number (DID6(HW))** Identifier assigned to the processor Device 6 (virtual PCI-to-PCI bridge, PCI Express Graphics port).
1:0	RO	01b	Core	**Device Identification Number (DID6(LB))** Identifier assigned to the processor Device 6 (virtual PCI-to-PCI bridge, PCI Express Graphics port).

6.2.3 PCICMD6 - PCI Command

B/D/F/Type: 0/6/0/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

Table 26. PCICMD6 - PCI Command Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:11	RO	00h	Core	**Reserved**
10	RW	0b	Core	**INTA Assertion Disable (INTAAD)** 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and deassert messages.
9	RO	0b	Core	**Fast Back-to-Back Enable (FB2B)** Not Applicable or Implemented. hard wired to 0.
8	RW	0b	Core	**SERR# Message Enable (SERRE1)** Controls Device 6 SERR# messaging. The processor communicates the SERR# condition by sending an SERR message to the PCH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control Register. In addition, for Type 1 configuration space header devices, this bit, when set, enables transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error messages forwarded from the secondary interface. This bit does not affect the transmission of forwarded ERR_COR messages. 0 = The SERR message is generated by the processor for Device 6 only under conditions enabled individually through the Device Control Register. 1 = The processor is enabled to generate SERR messages which is sent to the PCH for specific Device 6 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS6 register.
7	RO	0b	Core	**Reserved** Not Applicable or Implemented. Hard wired to 0.

Table 26. PCICMD6 - PCI Command Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
6	RW	0b	Core	**Parity Error Response Enable (PERRE)** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register CANNOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5	RO	0b	Core	**VGA Palette Snoop (VGAPS)** Not Applicable or Implemented. Hard wired to 0.
4	RO	0b	Core	**Memory Write and Invalidate Enable (MWIE)** Not Applicable or Implemented. Hard wired to 0.
3	RO	0b	Core	**Special Cycle Enable (SCE)** Not Applicable or Implemented. hard wired to 0.
2	RW	0b	Core	**Bus Master Enable (BME)** Controls the ability of the PEG port to forward Memory and IO Read/Write Requests in the upstream direction. 0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to the *PCI Local Bus Specificatio*n, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/ reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address C0000h with byte enables deasserted. Reads is forwarded to memory address C0000h and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus is issued when the data is available. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.
1	RW	0b	Core	**Memory Access Enable (MAE)** 0 = All of Device 6's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE6, MLIMIT6, PMBASE6, and PMLIMIT6 registers.
0	RW	0b	Core	IO Access Enable (IOAE) 0 = All of Device 6's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE6, and IOLIMIT6 registers.

6.2.4 PCISTS6 - PCI Status

B/D/F/Type: 0/6/0/PCI
Address Offset: 6-7h
Default Value: 0010h
Access: RO; RWC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the processor.

Table 27. PCISTS6 - PCI Status Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15	RO	0b	Core	**Detected Parity Error (DPE)** Not Applicable or Implemented. Hard wired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (we don't do error forwarding).
14	RWC	0b	Core	**Signaled System Error (SSE)** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL6[1]) and internally detected error messages do not affect this field.
13	RO	0b	Core	**Received Master Abort Status (RMAS)** Not Applicable or Implemented. Hard wired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO	0b	Core	**Received Target Abort Status (RTAS)** Not Applicable or Implemented. Hard wired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO	0b	Core	**Signaled Target Abort Status (STAS)** Not Applicable or Implemented. Hard wired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	00b	Core	**DEVSELB Timing (DEVT)** This device is not the subtractively decoded device on bus 0. This bit field is therefore hard wired to 00 to indicate that the device uses the fastest possible decode.
8	RO	0b	Core	**Master Data Parity Error (PMDPE)** Because the primary side of the PCIe graphic's virtual P2P bridge is integrated with the PROCESSOR functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The *PCI Local Bus Specification* defines it as a R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	0b	Core	**Fast Back-to-Back (FB2B)** Not Applicable or Implemented. Hard wired to 0.
6	RO	0b	Core	**Reserved**

Table 27. PCISTS6 - PCI Status Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
5	RO	0b	Core	**66-/60-MHz Capability (CAP66)** Not Applicable or Implemented. Hard wired to 0.
4	RO	1b	Core	**Capabilities List (CAPL)** Indicates that a capabilities list is present. Hard wired to 1.
3	RO	0b	Core	**INTA Status (INTAS)** Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and deassert messages). The INTA Assertion Disable bit, PCICMD6[10], has no effect on this bit. Note that INTA emulation interrupts received across the link are not reflected in this bit.
2:0	RO	000b	Core	**Reserved**

6.2.5 RID6 - Revision Identification

B/D/F/Type: 0/6/0/PCI
Address Offset: 8h
Default Value: 10h
Access: RO
Size: 8 bits

This register contains the revision number of the processor Device 6. These bits are read only and writes to this register have no effect.

Table 28. RID6 - Revision Identification Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	10h	Core	**Revision Identification Number (RID6)** This is an 8-bit value that indicates the revision identification number for the processor Device 0. For the C-0 Stepping, this value is 10h.

6.2.6 CC6 - Class Code

B/D/F/Type: 0/6/0/PCI
Address Offset: 9-Bh
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register- specific programming interface.

Table 29. CC6 - Class Code Register

Bit	Access	Default Value	RST/ PWR	Description
23:16	RO	06h	Core	**Base Class Code (BCC)** Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO	04h	Core	**Sub-Class Code (SUBCC)** Indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO	00h	Core	**Programming Interface (PI)** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

6.2.7 CL6 - Cache Line Size

B/D/F/Type: 0/6/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RW
Size: 8 bits

Table 30. CL6 - Cache Line Size Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RW	00h	Core	**Cache Line Size (Scratch pad)** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

6.2.8 HDR6 - Header Type

B/D/F/Type: 0/6/0/PCI
Address Offset: Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Regist

Table 31. HDR6 - Header Type Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	01h	Core	**Header Type Register (HDR)** Returns 01 to indicate that this is a single function device with bridge header layout.

6.2.9 PBUSN6 - Primary Bus Number

B/D/F/Type: 0/6/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this “virtual” Host-PCI Express bridge is connected to PCI Bus 0.

Table 32. PBUSN6 - Primary Bus Number Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	00h	Core	**Primary Bus Number (BUSN)** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device 6 is an internal device and its primary bus is always 0, these bits are read only and are hard wired to 0.

6.2.10 SBUSN6 - Secondary Bus Number

B/D/F/Type: 0/6/0/PCI
Address Offset: 19h
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” bridge, i.e., to PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Table 33. SBUSN6 - Secondary Bus Number Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RW	00h	Core	**Secondary Bus Number (BUSN)** This field is programmed by configuration software with the bus number assigned to PCI Express-G.

6.2.11 SUBUSN6 - Subordinate Bus Number

B/D/F/Type: 0/6/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Table 34. SUBUSN6 - Subordinate Bus Number Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RW	00h	Core	**Subordinate Bus Number (BUSN)** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device 6 bridge. When only a single PCI device resides on the PCI Express-G segment, this register will contain the same value as the SBUSN6 register.

6.2.12 IOBASE6 - I/O Base Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 1Ch
Default Value: F0h
Access: RO; RW
Size: 8 bits

This register controls the CPU to PCI Express-G I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range is aligned to a 4-KB boundary.

Table 35. IOBASE6 - I/O Base Address Register

Bit	Access	Default Value	RST/ PWR	Description
7:4	RW	Fh	Core	**I/O Address Base (IOBASE)** Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express-G. BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses is forwarded to the PCI Express hierarchy associated with this device.
3:0	RO	0h	Core	**Reserved**

6.2.13 IOLIMIT6 - I/O Limit Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 1Dh
Default Value: 00h
Access: RO; RW
Size: 8 bits

This register controls the CPU to PCI Express-G I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range is at the top of a 4-KB aligned address block.

Table 36. IOLIMIT6 - I/O Limit Address Register

Bit	Access	Default Value	RST/ PWR	Description
7:4	RW	0h	Core	**I/O Address Limit (IOLIMIT)** Corresponds to A[15:12] of the I/O address limit of Device 6. Devices between this upper limit and IOBASE6 is passed to the PCI Express hierarchy associated with this device.
3:0	RO	0h	Core	**Reserved**

6.2.14 SSTS6 - Secondary Status

B/D/F/Type: 0/6/0/PCI
Address Offset: 1E-1Fh
Default Value: 0000h
Access: RWC; RO
Size: 16 bits

SSTS6 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express-G side) of the "virtual" PCI-to-PCI bridge embedded within processor.

Table 37. SSTS6 - Secondary Status Register

Bit	Access	Default Value	RST/ PWR	Description
15	RWC	0b	Core	**Detected Parity Error (DPE)** This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned TLP, regardless of the state of the Parity Error Response Enable bit in the Bridge Control Register.
14	RWC	0b	Core	**Received System Error (RSE)** This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL.
13	RWC	0b	Core	**Received Master Abort (RMA)** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	RWC	0b	Core	**Received Target Abort (RTA)** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO	0b	Core	**Signaled Target Abort (STA)** Not Applicable or Implemented. Hard wired to 0. The processor does not generate Target Aborts (the processor will never complete a request using the Completer Abort Completion status).
10:9	RO	00b	Core	**DEVSELB Timing (DEVT)** Not Applicable or Implemented. Hard wired to 0.
8	RWC	0b	Core	**Master Data Parity Error (SMDPE)** When set indicates that the PROCESSOR received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO	0b	Core	**Fast Back-to-Back (FB2B)** Not Applicable or Implemented. Hard wired to 0.
6	RO	0b	Core	**Reserved**
5	RO	0b	Core	**66-/60-MHz Capability (CAP66)** Not Applicable or Implemented. Hard wired to 0.
4:0	RO	00h	Core	**Reserved**

6.2.15 MBASE6 - Memory Base Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 20-21h
Default Value: FFF0h
Access: RO; RW
Size: 16 bits

This register controls the CPU to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range is aligned to a 1-MB boundary.

Table 38. MBASE6 - Memory Base Address Register

Bit	Access	Default Value	RST/ PWR	Description
15:4	RW	FFFh	Core	**Memory Address Base (MBASE)** Corresponds to A[31:20] of the lower limit of the memory range that is passed to PCI Express-G.
3:0	RO	0h	Core	**Reserved**

6.2.16 MLIMIT6 - Memory Limit Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 22-23h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

This register controls the CPU to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range is at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express-G address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-PCI Express memory access performance.

Note also that configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges, i.e., prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the processor hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Table 39. MLIMIT6 - Memory Limit Address Register

Bit	Access	Default Value	RST/ PWR	Description
15:4	RW	000h	Core	**Memory Address Limit (MLIMIT)** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express-G.
3:0	RO	0h	Core	**Reserved**

6.2.17 PMBASE6 - Prefetchable Memory Base Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 24-25h
Default Value: FFF1h
Access: RO; RW
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range is aligned to a 1-MB boundary.

Table 40. PMBASE6 - Prefetchable Memory Base Address Register

Bit	Access	Default Value	RST/ PWR	Description
15:4	RW	FFFh	Core	**Prefetchable Memory Base Address (MBASE)** Corresponds to A[31:20] of the lower limit of the memory range that is passed to PCI Express-G.
3:0	RO	1h	Core	**64-bit Address Support (64-bit Address Support)** Indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.

6.2.18 PMLIMIT6 - Prefetchable Memory Limit Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 26-27h
Default Value: 0001h
Access: RO; RW
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range is at the top of a 1-MB aligned memory block.

Note: Prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Table 41. PMLIMIT6 - Prefetchable Memory Limit Address Register

Bit	Access	Default Value	RST/ PWR	Description
15:4	RW	000h	Core	**Prefetchable Memory Address Limit (PMLIMIT)** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express-G.
3:0	RO	1h	Core	**64-bit Address Support (RSVD)** Indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch

6.2.19 PMBASEU6 - Prefetchable Memory Base Address Upper

B/D/F/Type: 0/6/0/PCI
Address Offset: 28-2Bh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range is aligned to a 1-MB boundary.

Table 42. PMBASEU6 - Prefetchable Memory Base Address Upper Register

Bit	Access	Default Value	RST/ PWR	Description
31:0	RW	00000000h	Core	**Prefetchable Memory Base Address (MBASEU)** Corresponds to A[63:32] of the lower limit of the prefetchable memory range that is passed to PCI Express-G.

6.2.20 PMLIMITU6 - Prefetchable Memory Limit Address Upper

B/D/F/Type: 0/6/0/PCI
Address Offset: 2C-2Fh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40- bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range is at the top of a 1-MB aligned memory block.

Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Table 43. PMLIMITU6 - Prefetchable Memory Limit Address Upper Register

Bit	Access	Default Value	RST/ PWR	Description
31:0	RW	00000000h	Core	**Prefetchable Memory Address Limit (MLIMITU)** Corresponds to A[63:32] of the upper limit of the prefetchable Memory range that is passed to PCI Express-G.

6.2.21 CAPPTR6 - Capabilities Pointer

B/D/F/Type: 0/6/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Table 44. CAPPTR6 - Capabilities Pointer Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	88h	Core	**First Capability (CAPPTR6)** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

6.2.22 INTRLINE6 - Interrupt Line

B/D/F/Type: 0/6/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: RW
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Table 45. INTRLINE6 - Interrupt Line Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RW	00h	Core	**Interrupt Connection (INTCON)** Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected.

6.2.23 INTRPIN6 - Interrupt Pin

B/D/F/Type: 0/6/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits
This register specifies which interrupt pin this device uses.

Table 46. INTRPIN6 - Interrupt Pin Register

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	01h	Core	**Interrupt Pin (INTPIN)** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

6.2.24 BCTRL6 - Bridge Control

B/D/F/Type: 0/6/0/PCI
Address Offset: 3E-3Fh
Default Value: 0000h
Access: RO; RW
Size: 16 bits
This register provides extensions to the PCICMD6 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express-G) as well as some bits that affect the overall behavior of the “virtual” Host-PCI Express bridge embedded within processor, e.g., VGA compatible address ranges mapping.

Table 47. BCTRL6 - Bridge Control Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:12	RO	0h	Core	**Reserved**
11	RO	0b	Core	**Discard Timer SERR# Enable (DTSERRE)** Not Applicable or Implemented. Hard wired to 0.
10	RO	0b	Core	**Discard Timer Status (DTSTS)** Not Applicable or Implemented. Hard wired to 0.
9	RO	0b	Core	**Secondary Discard Timer (SDT)** Not Applicable or Implemented. Hard wired to 0.
8	RO	0b	Core	**Primary Discard Timer (PDT)** Not Applicable or Implemented. Hard wired to 0.
7	RO	0b	Core	**Fast Back-to-Back Enable (FB2BEN)** Not Applicable or Implemented. Hard wired to 0.
6	RW	0b	Core	**Secondary Bus Reset (SRESET)** Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.

Table 47. BCTRL6 - Bridge Control Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
5	RO	0b	Core	**Master Abort Mode (MAMODE)** Does not apply to PCI Express. Hard wired to 0.
4	RW	0b	Core	**VGA 16-bit Decode (VGA16D)** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if Bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	RW	0b	Core	**VGA Enable (VGAEN)** Controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/ MDAP table in device 0, offset 97h[0].
2	RW	0b	Core	**ISA Enable (ISAEN)** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the processor to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions is mapped to PCI Express-G. 1 = Processor will not forward to PCI Express-G any I/O transactions addressing the last 768 bytes in each 1-KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers.
1	RW	0b	Core	**SERR Enable (SERREN)** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RW	0b	Core	**Parity Error Response Enable (PEREN)** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the PROCESSOR receives across the link (upstream) a Read Data Completion Poisoned TLP 0 = Master Data Parity Error bit in Secondary Status register CANNOT be set. 1 = Master Data Parity Error bit in Secondary Status register CAN be set.

6.2.25 PM_CAPID6 - Power Management Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: 80-83h
Default Value: C8039001h
Access: RO
Size: 32 bits

Table 48. PM_CAPID6 - Power Management Capabilities Register

Bit	Access	Default Value	RST/ PWR	Description
31:27	RO	19h	Core	**PME Support (PMES)** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold, it simply must report that those states are supported. Refer to the latest *PCI Power Management Specification* for encoding explanation and other power management details.
26	RO	0b	Core	**D2 Power State Support (D2PSS)** hard wired to 0 to indicate that the D2 power management state is NOT supported.
25	RO	0b	Core	**D1 Power State Support (D1PSS)** hard wired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO	000b	Core	**Auxiliary Current (AUXC)** hard wired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO	0b	Core	**Device Specific Initialization (DSI)** hard wired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO	0b	Core	**Auxiliary Power Source (APS)** hard wired to 0.
19	RO	0b	Core	**PME Clock (PMECLK)** hard wired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO	011b	Core	**PCI PM CAP Version (PCIPMCV)** Version - A value of 011b indicates that this function complies with the latest revision of the *PCI Power Management Interface Specification*.
15:8	RO	90h	Core	**Pointer to Next Capability (PNC)** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO	01h	Core	**Capability ID (CID)** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

6.2.26 PM_CS6 - Power Management Control/Status

B/D/F/Type: 0/6/0/PCI
Address Offset: 84-87h
Default Value: 00000008h
Access: RO; RW-S; RW
Size: 32 bits

Table 49. PM_CS6 - Power Management Control/Status Register

Bit	Access	Default Value	RST/ PWR	Description
31:16	RO	0000h	Core	**Reserved** Not Applicable or Implemented. Hard wired to 0.
15	RO	0b	Core	**PME Status (PMESTS)** Indicates that this device does not support PMEB generation from D3cold.
14:13	RO	00b	Core	**Data Scale (DSCALE)** Indicates that this device does not support the power management data register.
12:9	RO	0h	Core	**Data Select (DSEL)** Indicates that this device does not support the power management data register.
8	RW-S	0b	Core	**PME Enable (PMEE)** Indicates that this device does not generate PMEB assertion from any D-state.0:PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware.See PM_CAP[15:11]
7:4	RO	0000b	Core	**Reserved**
3	RO	1b	Core	**No Soft Reset (NSR)** When set to 1 this bit indicates that the device is transitioning from D3hot to D0 because the power state commands do not perform an internal reset. Config context is preserved. Upon transition no additional operating sys intervention is required to preserve configuration context beyond writing the power state bits. When clear the devices do not perform an internal reset upon transitioning from D3hot to D0 via software control of the power state bits. Regardless of this bit, the devices that transition from a D3hot to D0 by a system or bus segment reset will return to the device state D0 un-initialized with only PME context preserved if PME is supported and enabled.
2	RO	0b	Core	**Reserved**

Table 49. PM_CS6 - Power Management Control/Status Register

Bit	Access	Default Value	RST/ PWR	Description
1:0	RW	00b	Core	**Power State (PS)** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of type 0 config cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the PROCESSOR logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

6.2.27 SS_CAPID - Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: 88-8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Table 50. SS_CAPID - Subsystem ID and Vendor ID Capabilities Register

Bit	Access	Default Value	RST/ PWR	Description
31:16	RO	0000h	Core	**Reserved**
15:8	RO	80h	Core	**Pointer to Next Capability (PNC)** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO	0Dh	Core	**Capability ID (CID)** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

6.2.28 SS - Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/6/0/PCI
Address Offset: 8C-8Fh
Default Value: 00008086h
Access: RW-O
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Table 51. SS - Subsystem ID and Subsystem Vendor ID Register

Bit	Access	Default Value	RST/ PWR	Description
31:16	RW-O	0000h	Core	**Subsystem ID (SSID)** Identifies the particular subsystem and is assigned by the vendor.
15:0	RW-O	8086h	Core	**Subsystem Vendor ID (SSVID)** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

6.2.29 MSI_CAPID - Message Signaled Interrupts Capability ID

B/D/F/Type: 0/6/0/PCI
Address Offset: 90-91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case walking this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Table 52. MSI_CAPID - Message Signaled Interrupts Capability ID Register

Bit	Access	Default Value	RST/ PWR	Description
15:8	RO	A0h	Core	**Pointer to Next Capability (PNC)** This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO	05h	Core	**Capability ID (CID)** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

6.2.30 MC - Message Control

B/D/F/Type: 0/6/0/PCI
Address Offset: 92-93h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Table 53. MC - Message Control Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:8	RO	00h	Core	**Reserved**
7	RO	0b	Core	**64-bit Address Capable (64AC)** hard wired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32-b/4-GB limit.

Table 53. MC - Message Control Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
6:4	RW	000b	Core	**Multiple Message Enable (MME)** System software programs this field to indicate the actual number of messages allocated to this device. This number is equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	Core	**Multiple Message Capable (MMC)** System software reads this field to determine the number of messages being requested by this device. Value:Number of Messages Requested 000: 1 All of the following are reserved in this implementation: 001:2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
0	RW	0b	Core	**MSI Enable (MSIEN)** Controls the ability of this device to generate MSIs. 0 = MSI will not be generated. 1 = MSI is generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS6[3]) will not be set.

6.2.31 MA - Message Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 94-97h
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Table 54. MA - Message Address Register

Bit	Access	Default Value	RST/ PWR	Description
31:2	RW	00000000h	Core	**Message Address (MA)** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	Core	**Force DWord Align (FDWA)** hard wired to 0 so that addresses assigned by system software are always aligned on a dword address boundary.

6.2.32 MD - Message Data

B/D/F/Type: 0/6/0/PCI
Address Offset: 98-99h
Default Value: 0000h
Access: RW
Size: 16 bits

Table 55. MD - Message Data Register

Bit	Access	Default Value	RST/ PWR	Description
15:0	RW	0000h	Core	**Message Data (MD)** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

6.2.33 PEG_CAPL - PCI Express-G Capability List

B/D/F/Type: 0/6/0/PCI
Address Offset: A0-A1h
Default Value: 0010h
Access: RO
Size: 16 bits

Enumerates the PCI Express capability structure.

Table 56. PEG_CAPL - PCI Express-G Capability List Register

Bit	Access	Default Value	RST/ PWR	Description
15:8	RO	00h	Core	**Pointer to Next Capability (PNC)** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO	10h	Core	**Capability ID (CID)** Identifies this linked list item (capability structure) as being for PCI Express registers.

6.2.34 PEG_CAP - PCI Express-G Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: A2-A3h
Default Value: 0142h
Access: RO; RW-O
Size: 16 bits

Indicates PCI Express device capabilities.

Table 57. PEG_CAP - PCI Express-G Capabilities Register

Bit	Access	Default Value	RST/ PWR	Description
15	RO	0b	Core	**Reserved**
14	RO	0b	Core	**Reserved** Reserved for TCS Routing Supported.
13:9	RO	00h	Core	**Interrupt Message Number (IMN)** Not Applicable or Implemented. Hard wired to 0.
8	RW-O	1b	Core	**Slot Implemented (SI)** 0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot. **BIOS Requirement:** This field must be initialized appropriately if a slot connection is not implemented.
7:4	RO	4h	Core	**Device/Port Type (DPT)** hard wired to 4h to indicate root port of PCI Express Root Complex.

Table 57. PEG_CAP - PCI Express-G Capabilities Register

Bit	Access	Default Value	RST/ PWR	Description
3:0	RO	2h	Core	**PCI Express Capability Version (PCIECV)** hard wired to 2h to indicate compliance to the PCI Express Capabilities Register Expansion ECN.

6.2.35 DCAP - Device Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: A4-A7h
Default Value: 00008000h
Access: RO
Size: 32 bits

Indicates PCI Express device capabilities.

Table 58. DCAP - Device Capabilities Register

Bit	Access	Default Value	RST/ PWR	Description
31:16	RO	0000h	Core	**Reserved** Not Applicable or Implemented. Hard wired to 0.
15	RO	1b	Core	**Role-Based Error Reporting (RBER)** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express Base spec.
14:6	RO	000h	Core	**Reserved** Not Applicable or Implemented. Hard wired to 0.
5	RO	0b	Core	**Extended Tag Field Supported (ETFS)** hard wired to indicate support for 5-bit Tags as a Requestor.
4:3	RO	00b	Core	**Phantom Functions Supported (PFS)** Not Applicable or Implemented. Hard wired to 0.
2:0	RO	000b	Core	**Max Payload Size (MPS)** hard wired to indicate 128B max supported payload for Transaction Layer Packets (TLP).

6.2.36 DCTL - Device Control

B/D/F/Type: 0/6/0/PCI
Address Offset: A8-A9h
Default Value: 0000h
Access: RO; RW
Size: 16 bits
Provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Table 59. DCTL - Device Control Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15	RO	0h	Core	**Reserved**
14:12	RO	000b	Core	**Reserved for Max Read Request Size (MRRS)**
11	RO	0b	Core	**Reserved for Enable No Snoop (RSVD)**
10	RO	0b	Core	**Reserved** Reserved for Auxiliary (AUX) PM Enable ()
9	RO	0b	Core	**Reserved** Reserved for Phantom Functions Enable ()
8	RO	0b	Core	**Reserved** Reserved for Extended Tag Field Enable ()
7:5	RW	000b	Core	**Max Payload Size (MPS)** 000:128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO	0b	Core	**Reserved for Enable Relaxed Ordering (RSVD)**
3	RW	0b	Core	**Unsupported Request Reporting Enable (URRE)** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_CORR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_CORR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL or ERR_NONFATAL is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity bit set in the Uncorrectable Error Severity register.
2	RW	0b	Core	**Fatal Error Reporting Enable (FERE)** When set, enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

Table 59. DCTL - Device Control Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
1	RW	0b	Core	**Non-Fatal Error Reporting Enable (NERE)** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	RW	0b	Core	**Correctable Error Reporting Enable (CERE)** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

6.2.37 DSTS - Device Status

B/D/F/Type: 0/6/0/PCI
Address Offset: AA-ABh
Default Value: 0000h
Access: RO; RWC
Size: 16 bits

Reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Table 60. DSTS - Device Status Register

Bit	Access	Default Value	RST/ PWR	Description
15:6	RO	000h	Core	**Reserved and Zero (RSVD)** For future R/WC/S implementations; software must use 0 for writes to bits.
5	RO	0b	Core	**Transactions Pending (TP)** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO	0b	Core	**Reserved**
3	RWC	0b	Core	**Unsupported Request Detected (URD)** When set this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.

Table 60. DSTS - Device Status Register

Bit	Access	Default Value	RST/ PWR	Description
2	RWC	0b	Core	**Fatal Error Detected (FED)** When set this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	RWC	0b	Core	**Non-Fatal Error Detected (NFED)** When set this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
0	RWC	0b	Core	**Correctable Error Detected (CED)** When set this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

6.2.38 LCAP - Link Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: AC-AFh
Default Value: 03214C81h
Access: RO; RW-O
Size: 32 bits

Indicates PCI Express device specific capabilities.

Table 61. LCAP - Link Capabilities Register (Sheet 1 of 3)

Bit	Access	Default Value	RST/ PWR	Description
31:24	RO	03h	Core	**Port Number (PN)** Indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:22	RO	00b	Core	**Reserved**

Table 61. LCAP - Link Capabilities Register (Sheet 2 of 3)

Bit	Access	Default Value	RST/ PWR	Description
21	RO	1b	Core	**Link Bandwidth Notification Capability (LBNC)** A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch downstream ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Devices that do not implement the Link Bandwidth Notification capability must hardwire this bit to 0b.
20	RO	0b	Core	**Data Link Layer Link Active Reporting Capable (DLLLARC)** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable field of the Slot Capabilities register), this bit must be set to 1b. For Upstream Ports and components that do not support this optional capability, this bit must be hard wired to 0b.
19	RO	0b	Core	**Surprise Down Error Reporting Capable (SDERC)** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hard wired to 0b.
18	RO	0b	Core	**Clock Power Management (CPM)** A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states. This capability is applicable only in form factors that support “clock request” (CLKREQ#) capability. For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.

Table 61. LCAP - Link Capabilities Register (Sheet 3 of 3)

Bit	Access	Default Value	RST/ PWR	Description
17:15	RW-O	010b	Core	**L1 Exit Latency (L1ELAT)** Indicates the length of time this Port requires to complete the transition from L1 to L0. 000: Less than 1us 001: 1 us to less than 2 us 010: 2 us to less than 4 us 011: 4 us to less than 8 us 100: 8 us to less than 16 us 101: 16 us to less than 32 us 110: 32 us-64 us 111: More than 64 us BIOS Requirement: If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RO	100b	Core	**L0s Exit Latency (L0SELAT)** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000:Less than 64 ns 001:64 ns to less than 128 ns 010:128 ns to less than 256 ns 011:256 ns to less than 512 ns 100:512 ns to less than 1 µs 101:1 µs to less than 2 µs 110:2 µs - 4 µs 111:More than 4 µs The actual value of this field depends on the common Clock Configuration bit (LCTL[6]) register.
11:10	RW-O	11b	Core	**Active State Link PM Support (ASLPMS)** ASPM L0s and L1 supported.
9:4	RW-O	08h	Core	**Max Link Width (MLW)** Indicates the maximum number of lanes supported for this link.
3:0	RW-O	1h	Core	**Max Link Speed (MLS)** Supported Link Speed – This field indicates the supported Link speed(s) of the associated Port. Defined encodings are: 0001b2.5-GT/s Link speed supported All other encodings are reserved.

6.2.39 LCTL - Link Control

B/D/F/Type: 0/6/0/PCI
Address Offset: B0-B1h
Default Value: 0000h
Access: RO; RW; RW-SC
Size: 16 bits
Allows control of PCI Express link.

Table 62. LCTL - Link Control Register (Sheet 1 of 3)

Bit	Access	Default Value	RST/ PWR	Description
15:12	RO	0000b	Core	**Reserved**
11	RW	0b	Core	**Link Autonomous Bandwidth Interrupt Enable (LABIE)** When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. This bit is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Devices that do not implement the Link Bandwidth Notification capability must hardwire this bit to 0b.
10	RW	0b	Core	**Link Bandwidth Management Interrupt Enable (LBMIE)** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches.
9	RW	0b	Core	**Hardware Autonomous Width Disable (HAWD)** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Devices that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b.
8	RO	0b	Core	**Enable Clock Power Management (ECPM)** Applicable only for form factors that support a “Clock Request” (CLKREQ#) mechanism, this enable functions as follows: 0b – Clock power management is disabled and device must hold CLKREQ# signal low. 1b - When this bit is set to 1 the device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification. Default value of this field is 0b. Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.

Table 62. LCTL - Link Control Register (Sheet 2 of 3)

Bit	Access	Default Value	RST/ PWR	Description
7	RW	0b	Core	**Extended Synch (ES)** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication.This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	RW	0b	Core	**Common Clock Configuration (CCC)** 0 = Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training.
5	RW-SC	0b	Core	**Retrain Link (RL)** 0 = Normal operation. 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4	RW	0b	Core	**Link Disable (LD)** 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO	0b	Core	**Read Completion Boundary (RCB)** hard wired to 0 to indicate 64 byte.
2	RO	0b	Core	**Reserved (FEDLB)**

Table 62. LCTL - Link Control Register (Sheet 3 of 3)

Bit	Access	Default Value	RST/ PWR	Description
1:0	RW	00b	Core	**Active State PM (ASPM)** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: L1 Entry Enabled 11: L0s and L1 Entry Supported **Note:** "L0s Entry Enabled" indicates the Transmitter entering L0s is supported. The Receiver must be capable of entering L0s even when the field is disabled (00b). ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1.

6.2.40 LSTS - Link Status

B/D/F/Type: 0/6/0/PCI
Address Offset: B2-B3h
Default Value: 1000h
Access: RWC; RO
Size: 16 bits
Indicates PCI Express link status.

Table 63. LSTS - Link Status Register (Sheet 1 of 3)

Bit	Access	Default Value	RST/ PWR	Description
15	RWC	0b	Core	**Link Autonomous Bandwidth Status (LABWS)** This bit is set to 1b by hardware to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the downstream component that was indicated as an autonomous change. This bit must be set when the upstream component receives eight consecutive TS1 or TS2 ordered sets with the Autonomous Change bit set.

Table 63. LSTS - Link Status Register (Sheet 2 of 3)

Bit	Access	Default Value	RST/ PWR	Description
14	RWC	0b	Core	**Link Bandwidth Management Status (LBWMS)** This bit is set to 1b by hardware to indicate that either of the following has occurred without the port transitioning through DL_Down status: A link retraining initiated by a write of 1b to the Retrain Link bit has completed. **Note:** This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has autonomously changed link speed or width to attempt to correct unreliable link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the downstream component that was not indicated as an autonomous change.
13	RO	0b	Core	**Data Link Layer Link Active (Optional) (DLLLA)** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Active Capability bit is implemented. Otherwise, this bit must be hard wired to 0b.
12	RO	1b	Core	**Slot Clock Configuration (SCC)** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO	0b	Core	**Link Training (LTRN)** Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO	0b	Core	**Undefined (Undefined)** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
9:4	RO	00h	Core	**Negotiated Link Width (NLW)** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h: Reserved 01h: X1 02h: X2 04h: X4 08h: X8 10h: X16 All other encodings are reserved.

Table 63. LSTS - Link Status Register (Sheet 3 of 3)

Bit	Access	Default Value	RST/ PWR	Description
3:0	RO	0h	Core	**Current Link Speed (CLS)** This field indicates the negotiated Link speed of the given PCI Express Link.Defined encodings are: 0001b 2.5 GT/s PCI Express Link All other encodings are reserved. The value in this field is undefined when the Link is not up.

6.2.41 SLOTCAP - Slot Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: B4-B7h
Default Value: 00040000h
Access: RW-O; RO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Table 64. SLOTCAP - Slot Capabilities Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
31:19	RW-O	0000h	Core	**Physical Slot Number (PSN)** Indicates the physical slot number attached to this Port. BIOS Requirement: This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.
18	RW-O	1b	Core	**No Command Completed Support (NCCS)** When set to 1b, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set to 1b if the hotplug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
17	RO	0b	Core	**Reserved for Electromechanical Interlock Present (EIP)** When set to 1b, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot.
16:15	RW-O	00b	Core	**Slot Power Limit Scale (SPLS)** Specifies the scale used for the Slot Power Limit Value. 00: 1.0x 01: 0.1x 10: 0.01x 11: 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.

Table 64. SLOTCAP - Slot Capabilities Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
14:7	RW-O	00h	Core	**Slot Power Limit Value (SPLV)** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	RO	0b	Core	**Reserved for Hot-plug Capable (HPC)** When set to 1b, this bit indicates that this slot is capable of supporting hot-lug operations.
5	RO	0b	Core	**Reserved for Hot-plug Surprise (HPS)** When set to 1b, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.
4	RO	0b	Core	**Reserved for Power Indicator Present (PIP)** When set to 1b, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.
3	RO	0b	Core	**Reserved for Attention Indicator Present (AIP)** When set to 1b, this bit indicates that an Attention Indicator is electrically controlled by the chassis.
2	RO	0b	Core	**Reserved for MRL Sensor Present (MSP)** When set to 1b, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.
1	RO	0b	Core	**Reserved for Power Controller Present (PCP)** When set to 1b, this bit indicates that a software programmable Power Controller is implemented for this slot/ adapter (depending on form factor).
0	RO	0b	Core	**Reserved for Attention Button Present (ABP)** When set to 1b, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.

6.2.42 SLOTCTL - Slot Control

B/D/F/Type: 0/6/0/PCI
Address Offset: B8-B9h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Table 65. SLOTCTL - Slot Control Register (Sheet 1 of 3)

Bit	Access	Default Value	RST/ PWR	Description
15:13	RO	000b	Core	**Reserved**

Table 65. SLOTCTL - Slot Control Register (Sheet 2 of 3)

Bit	Access	Default Value	RST/ PWR	Description
12	RO	0b	Core	**Reserved for Data Link Layer State Changed Enable (DLLSCE)** If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. If the Data Link Layer Link Active capability is not implemented, this bit is permitted to be read-only with a value of 0b.
11	RO	0b	Core	**Reserved for Electromechanical Interlock Control (EIC)** If an Electromechanical Interlock is implemented, a write of 1b to this field causes the state of the interlock to toggle. A write of 0b to this field has no effect. A read to this register always returns a 0.
10	RO	0b	Core	**Reserved for Power Controller Control (PCC)** If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. Depending on the form factor, the power is turned on/off either to the slot or within the adapter. Note that in some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. The defined encodings are: 0b Power On 1b Power Off If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined.
9:8	RO	00b	Core	**Reserved Power Indicator Control (PIC)** If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00:Reserved 01:On 10:Blink 11:Off If the Power Indicator Present bit in the Slot Capabilities register is 0b, this field is permitted to be read-only with a value of 00b.

Table 65. SLOTCTL - Slot Control Register (Sheet 3 of 3)

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved for Attention Indicator Control (AIC)** If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. If the indicator is electrically controlled by chassis, the indicator is controlled directly by the downstream port through implementation specific mechanisms. 00:Reserved 01:On 10:Blink 11:Off If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this field is permitted to be read only with a value of 00b.
5	RO	0b	Core	**Reserved for Hot-Plug Interrupt Enable (HPIE)** When set to 1b, this bit enables generation of an interrupt on enabled hot-plug events Default value of this field is 0b. If the Hot Plug Capable field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
4	RO	0b	Core	**Reserved for Command Completed Interrupt Enable (CCI)** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), when set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. Default value of this field is 0b. If Command Completed notification is not supported, this bit must be hard wired to 0b.
3	RW	0b	Core	**Presence Detect Changed Enable (PDCE)** When set to 1b, this bit enables software notification on a presence detect changed event.
2	RO	0b	Core	**Reserved for MRL Sensor Changed Enable (MSCE)** When set to 1b, this bit enables software notification on a MRL sensor changed event. Default value of this field is 0b. If the MRL Sensor Present field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
1	RO	0b	Core	**Reserved for Power Fault Detected Enable (PFDE)** When set to 1b, this bit enables software notification on a power fault event. Default value of this field is 0b. If Power Fault detection is not supported, this bit is permitted to be read-only with a value of 0b
0	RO	0b	Core	**Reserved for Attention Button Pressed Enable (ABPE)** When set to 1b, this bit enables software notification on an attention button pressed event.

6.2.43 SLOTSTS - Slot Status

B/D/F/Type: 0/6/0/PCI
Address Offset: BA-BBh
Default Value: 0000h
Access: RO; RWC
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Table 66. SLOTSTS - Slot Status Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:9	RO	0000000b	Core	**Reserved and Zero** For future R/WC/S implementations; software must use 0 for writes to bits.
8	RO	0b	Core	**Reserved for Data Link Layer State Changed (DLLSC)** This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
7	RO	0b	Core	**Reserved for Electromechanical Interlock Status (EIS)** If an Electromechanical Interlock is implemented, this bit indicates the current status of the Electromechanical Interlock. Defined encodings are: 0b Electromechanical Interlock Disengaged 1b Electromechanical Interlock Engaged
6	RO	0b	Core	**Presence Detect State (PDS)** In band presence detect state: 0b: Slot Empty 1b: Card present in slot This bit indicates the presence of an adapter in the slot, reflected by the logical “OR” of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. Defined encodings are: 0b Slot Empty 1b Card Present in slot This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.

Table 66. SLOTSTS - Slot Status Register (Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
5	RO	0b	Core	**Reserved for MRL Sensor State (MSS)** This register reports the status of the MRL sensor if it is implemented. Defined encodings are: 0b MRL Closed 1b MRL Open
4	RO	0b	Core	**Reserved for Command Completed (CC)** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, this bit must be hard wired to 0b.
3	RWC	0b	Core	**Presence Detect Changed (PDC)** A pulse indication that the inband presence detect state has changed. This bit is set when the value reported in Presence Detect State is changed.
2	RO	0b	Core	**Reserved for MRL Sensor Changed (MSC)** If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.
1	RO	0b	Core	**Reserved for Power Fault Detected (PFD)** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
0	RO	0b	Core	**Reserved for Attention Button Pressed (ABP)** If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.

6.2.44 RCTL - Root Control

B/D/F/Type: 0/6/0/PCI
Address Offset: BC-BDh
Default Value: 0000h
Access: RO; RW
Size: 16 bits

Allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Table 67. RCTL - Root Control Register

Bit	Access	Default Value	RST/ PWR	Description
15:5	RO	000h	Core	**Reserved**
4	RO	0b	Core	**Reserved for CRS Software Visibility Enable (CSVE)** This bit, when set, enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software. Root Ports that do not implement this capability must hardwire this bit to 0b.
3	RW	0b	Core	**PME Interrupt Enable (PMEIE)** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	RW	0b	Core	**System Error on Fatal Error Enable (SEFEE)** 0 = Controls the Root Complex's response to fatal errors.No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	RW	0b	Core	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE)** Controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	RW	0b	Core	**System Error on Correctable Error Enable (SECEE)** Controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

6.2.45 RSTS - Root Status

B/D/F/Type: 0/6/0/PCI
Address Offset: C0-C3h
Default Value: 00000000h
Access: RO; RWC
Size: 32 bits

Provides information about PCI Express Root Complex specific parameters.

Table 68. RSTS - Root Status Register

Bit	Access	Default Value	RST/ PWR	Description
31:18	RO	0000h	Core	**Reserved and Zero (RSVD)** For future R/WC/S implementations; software must use 0 for writes to bits.
17	RO	0b	Core	**PME Pending (PMEP)** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	RWC	0b	Core	**PME Status (PMES)** Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO	0000h	Core	**PME Requestor ID (PMERID)** Indicates the PCI requestor ID of the last PME requestor.

6.2.46 LCTL2 - Link Control 2

B/D/F/Type: 0/6/0/PCI
Address Offset: D0-D1h
Default Value: 0001h
Access: RO; RW-S; RW;
Size: 16 bits

Table 69. LCTL2 - Link Control 2 Register (Sheet 1 of 3)

Bit	Access	Default Value	RST/ PWR	Description
15:13	RO	000b	Core	Reserved (RSVD):

Table 69. LCTL2 - Link Control 2 Register (Sheet 2 of 3)

Bit	Access	Default Value	RST/ PWR	Description
12	RW-S	0b	Core	**Compliance De-emphasis (ComplianceDeemphasis):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this bit to 0b. For a Multi-Function device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing.
11	RW-S	0b	Core	**Compliance SOS (compsos):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. For a Multi-Function device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. The default value of this bit is 0b. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0b.
10	RW-S	0b	Core	**Enter Modified Compliance (entermodcompliance):** When this bit is set to 1b, the device transmits modified compliance pattern if the LTSSM enters Polling.Compliance state. Components that support only the 2.5GT/s speed are permitted to hardwire this bit to 0b. Default value of this field is 0b.
9:7	RW-S	000b	Core	**Transmit Margin (txmargin):** This field controls the value of the non-de-emphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 for details of how the transmitter voltage level is determined in various states). Encodings: 000: Normal operating range 001: 800-1200 mV for full swing and 400-700 mV for half-swing 010 - (n-1): Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range 200-400 mV for full-swing and 100-200 mV for half-swing - 111: reserved Default value is 000b. Components that support only the 2.5GT/s speed are permitted to hardwire this bit to 0b.

Table 69. LCTL2 - Link Control 2 Register (Sheet 3 of 3)

Bit	Access	Default Value	RST/ PWR	Description
6	RW-S	0b	Core	**Selectable De-emphasis (selectabledeemphasis):** Encodings: 1b) -3.5dB 0b -6 dB Default value is implementation specific, unless a specific value is required for a selected form factor or platform. When the Link is operating at 2.5GT/s speed, the setting of this bit has no effect. Components that support only the 2.5GT/s speed are permitted to hardwire this bit to 0b.
5	RW	0b	Core	**Hardware Autonomous Speed Disable (HASD):** When set to 1b this bit disables hardware from changing the link speed for reasons other than attempting to correct unreliable link operation by reducing link speed.
4	RW-S	0b	Core	**Enter Compliance (EC):** Software is permitted to force a link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a link and then initiating a hot reset on the link.
3:0	RW	1h	Core	**Target Link Speed (TLS):** For Downstream ports, this field sets an upper limit on link operational speed by restricting the values advertised by the upstream component in its training sequences. Defined encodings are: 0001b 2.5Gb/s Target Link Speed All other encodings are reserved. If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities Register) unless the corresponding platform / form factor requires a different default value. For both Upstream and Downstream ports, this field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a link into compliance mode.

6.2.47 LSTS2 - Link Status 2

B/D/F/Type: 0/6/0/PCI
Address Offset: D2-D3h
Default Value: 0000h
Access: RO;
Size: 16 bits

Table 70. LSTS2 - Link Status 2 Register (Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:1	RO	0000h	Core	**Reserved (Rsvd):**

Table 70. LSTS2 - Link Status 2 Register (Sheet 2 of 2)

0	RO	0b	Core	**Current De-emphasis Level (CURDELVL):** Current De-emphasis Level – 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, this bit is 0b.

6.2.48 PEGLC - PCI Express-G Legacy Control

B/D/F/Type: 0/6/0/PCI
Address Offset: EC-EFh
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Controls functionality that is needed by Legacy (non-PCI Express aware) OS's during run time.

Table 71. PEGLC - PCI Express-G Legacy Control Register

Bit	Access	Default Value	RST/ PWR	Description
31:3	RO	00000000h	Core	**Reserved**
2	RW	0b	Core	**PME GPE Enable (PMEGPE)** 0 = Do not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received. This enables the processor to support PMEs on the PEG port under legacy OSs.
1	RW	0b	Core	**Hot-Plug GPE Enable (HPGPE)** 0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Generate a GPE Hot-Plug message when Hot-Plug Event is received. This enables the processor to support Hot-Plug on the PEG port under legacy OSs
0	RW	0b	Core	**General Message GPE Enable (GENGPE)** 0 = Do not forward received GPE assert/deassert messages. 1 = Forward received GPE assert/deassert messages.

6.3 PCI Device 6 - Extended Configuration

Table 72. PCI Device 6 - Extended Configuration

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Virtual Channel Enhanced Capability Header	VCECH	100	103	00010002h	RW-O; RO;
Port VC Capability Register 1	PVCCAP1	104	107	00000000h	RO;
Port VC Capability Register 2	PVCCAP2	108	10B	00000000h	RO;
Port VC Control	PVCCTL	10C	10D	0000h	RO; RW;
VC0 Resource Capability	VC0RCAP	110	113	00000001h	RO;
VC0 Resource Control	VC0RCTL	114	117	800000FFh	RO; RW;
VC0 Resource Status	VC0RSTS	11A	11B	0002h	RO;

6.3.1 VCECH - Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/6/0/MMR
Address Offset: 100-103h
Default Value: 00010002h
Access: RW-O; RO;
Size: 32 bits

Indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Table 73. VCECH - Virtual Channel Enhanced Capability Header

Bit	Access	Default Value	RST/ PWR	Description
31:20	RW-O	000h	Core	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO	1h	Core	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** hard wired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance
15:0	RO	0002h	Core	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

6.3.2 PVCCAP1 - Port VC Capability Register 1

B/D/F/Type: 0/6/0/MMR
Address Offset: 104-107h
Default Value: 00000000h
Access: RO;

Size: 32 bits
Describes the configuration of PCI Express Virtual Channels associated with this port.

Table 74. PVCCAP1 - Port VC Capability Register 1

Bit	Access	Default Value	RST/ PWR	Description
31:12	RO	00000h	Core	**Reserved**
11:10	RO	00b	Core	**Reserved** Reserved for Port Arbitration Table Entry Size ():
9:8	RO	00b	Core	**Reserved** Reserved for Reference Clock ():
7	RO	0b	Core	Reserved
6:4	RO	000b	Core	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	Core	**Reserved**
2:0	RO	000b	Core	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

6.3.3 PVCCAP2 - Port VC Capability Register 2

B/D/F/Type: 0/6/0/MMR
Address Offset: 108-10Bh
Default Value:00000000h
Access: RO;
Size:32 bits
Describes the configuration of PCI Express Virtual Channels associated with this port.

Table 75. PVCCAP2 - Port VC Capability Register 2

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8	RO	0000h	Core	**Reserved**
7:0	RO	00h	Core	**Reserved for VC Arbitration Capability (VCAC)**

6.3.4PVCCTL - Port VC Control

B/D/F/Type:0/6/0/MMR
Address Offset:10C-10Dh
Default Value:0000h
Access: RO; RW;
Size:16 bits

Table 76. PVCCTL - Port VC Control

Bit	Access	Default Value	RST/PWR	Description
15:4	RO	000h	Core	**Reserved**
3:1	RW	000b	Core	**VC Arbitration Select (VCAS)** This field is programmed by software to the only possible value as indicated in the VC Arbitration Capability field. Since there is no other VC supported than the default, this field is reserved.
0	RO	0b	Core	**Reserved for Load VC Arbitration Table** Used for software to update the VC Arbitration Table when VC arbitration uses the VC Arbitration Table. As a VC Arbitration Table is never used by this component this field will never be used.

6.3.5VC0RCAP - VC0 Resource Capability

B/D/F/Type:0/6/0/MMR
Address Offset:110-113h
Default Value:00000001h
Access: RO;
Size:32 bits

Table 77. VC0RCAP - VC0 Resource Capability (Sheet 1 of 2)

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Reserved for Port Arbitration Table Offset**
23	RO	0b	Core	**Reserved**

Table 77. VC0RCAP - VC0 Resource Capability (Sheet 2 of 2)

Bit	Access	Default Value	RST/PWR	Description
22:16	RO	00h	Core	**Reserved for Maximum Time Slots**
15	RO	0b	Core	**Reject Snoop Transactions (RSNPT):** Reject Snoop Transactions (RSNPT): 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header is rejected as an Unsupported Request
14:8	RO	00h	Core	**Reserved**
7:0	RO	01h	Core	**Port Arbitration Capability (PAC)** Port Arbitration Capability – Indicates types of Port Arbitration supported by the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to to-peer traffic, and RCRBs, but not for PCI Express Endpoint devices or Root Ports that do not support peer to peer traffic. Each bit location within this field corresponds to a Port Arbitration Capability defined below. When more than one bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Port Arbitration Select field (see below). Defined bit positions are: Bit 0 Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) Bit 1 Weighted Round Robin (WRR) arbitration with 32 phases Bit 2 WRR arbitration with 64 phases Bit 3 WRR arbitration with 128 phases Bit 4 Time-based WRR with 128 phases Bit 5 WRR arbitration with 256 phases Bits 6-7 Reserved MCH default indicates “Non-configurable hardware-fixed arbitration scheme”.

6.3.6 VC0RCTL - VC0 Resource Control

B/D/F/Type: 0/6/0/MMR
Address Offset: 114-117h
Default Value: 800000FFh
Access: RO; RW;
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Table 78. VC0RCTL - VC0 Resource Control

Bit	Access	Default Value	RST/PWR	Description
31	RO	1b	Core	**VC0 Enable (VC0E):** For VC0 this is hard wired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	Core	**Reserved**
26:24	RO	000b	Core	**VC0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hard wired to 0 and read only.
23:20	RO	0h	Core	**Reserved**
19:17	RW	000b	Core	**Port Arbitration Select (PAS):** Port Arbitration Select – This field configures the VC resource to provide a particular Port Arbitration service. This field is valid for RCRBs, Root Ports that support peer to peer traffic, and Switch Ports, but not for PCI Express Endpoint devices or Root Ports that do not support peer to peer traffic. The permissible value of this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16	RO	0b	Core	**Reserved** Reserved for Load Port Arbitration Table ():
15:8	RO	00h	Core	**Reserved**
7:1	RW	7Fh	Core	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	Core	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

6.3.7 VC0RSTS - VC0 Resource Status

B/D/F/Type: 0/6/0/MMR
Address Offset: 11A-11Bh
Default Value: 0002h
Access: RO;
Size: 16 bits
Reports the Virtual Channel specific status.

Table 79. VC0RSTS - VC0 Resource Status

Bit	Access	Default Value	RST/PWR	Description
15:2	RO	0000h	Core	**Reserved and Zero**
1	RO	1b	Core	**VC0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	Core	**Reserved** Reserved for Port Arbitration Table Status ():

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