Single Chip 12V Wireless Power Transmitter IC for TX-A6

IDTP9036

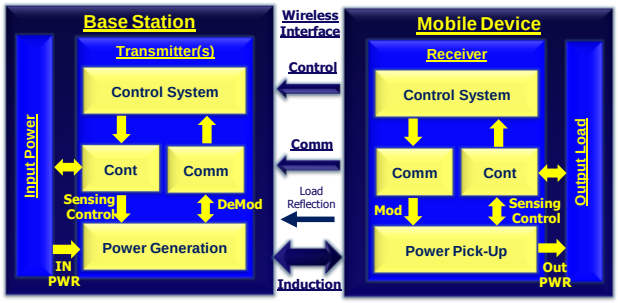
Product Datasheet

Features

- **Single-Chip 5W Solution for Wireless Power Consortium (WPC)-Compliant Power Transmitter Design TX-A6**
- **Conforms to WPC Specification Version 1.1 Specifications**
- **12V±5% Operating Input Voltage**
- **Integrated Half-Bridge Inverter**
- **Closed-Loop Power Transfer Control between Base Station and Mobile Device**
- **Demodulates and Decodes WPC-Compliant Message Packets**
- **5V Regulated DC/DC Converter**
- **Integrated RESET Function**
- **Proprietary Back-Channel Communication**
- **I²C Interface**
- **Open-Drain LED Indicator Outputs**
- **Over-Temperature/Current Protection**
- **Security and Encryption up to 64 bits**
- **Foreign Object Detection (FOD)**

Applications

- **WPC-Compliant Wireless Charging Base Stations**



Package: 6x6-48 TQFN (See page 27)
Ordering Information (See page 28)

Description

The IDTP9036 is a highly-integrated single-chip WPC-compliant wireless power transmitter IC for power transmitter design A6. The device operates with a 12V (±5%) adaptor, and supplies an integrated half-bridge inverter for DC/AC conversion. It controls the transferred power by modulating the switching frequency of the half-bridge inverter from 115kHz to 205kHz at a fixed 50% duty cycle as specified by the WPC specification for an "A6" transmitter. It contains logic circuits required to demodulate and decode WPC-compliant message packets sent by the mobile device to adjust the transferred power.

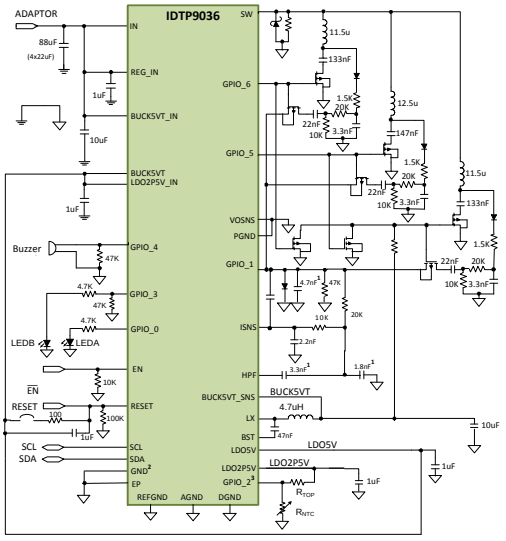
The IDTP9036 is an intelligent device that periodically pings the area surrounding the base station to detect a mobile device for charging while minimizing idle power. Once the mobile device is detected and authenticated, the IDTP9036 continuously monitors all communications from the mobile device, and adjusts the transmitted power accordingly by varying the switching frequency of the half-bridge inverter.

The IDTP9036 features a proprietary back-channel communication mode which enables the device to communicate with IDT's wireless power receiver solutions (e.g. IDTP9020). This feature enables additional layers of capabilities beyond the standard WPC requirements.

This device also features optional security and encryptions to securely authenticate the receiver before transferring power. This feature is available when an IDTP9020 is used for the receiver.

The IDTP9036 includes over-temperature/current protection and a Foreign Object Detection (FOD) method to protect the base station and mobile device from overheating in the presence of a metallic foreign object. It manages fault conditions associated with power transfer and controls status LEDs to indicate operating modes.

Typical Application Circuit



SIMPLIFIED APPLICATION DIAGRAM

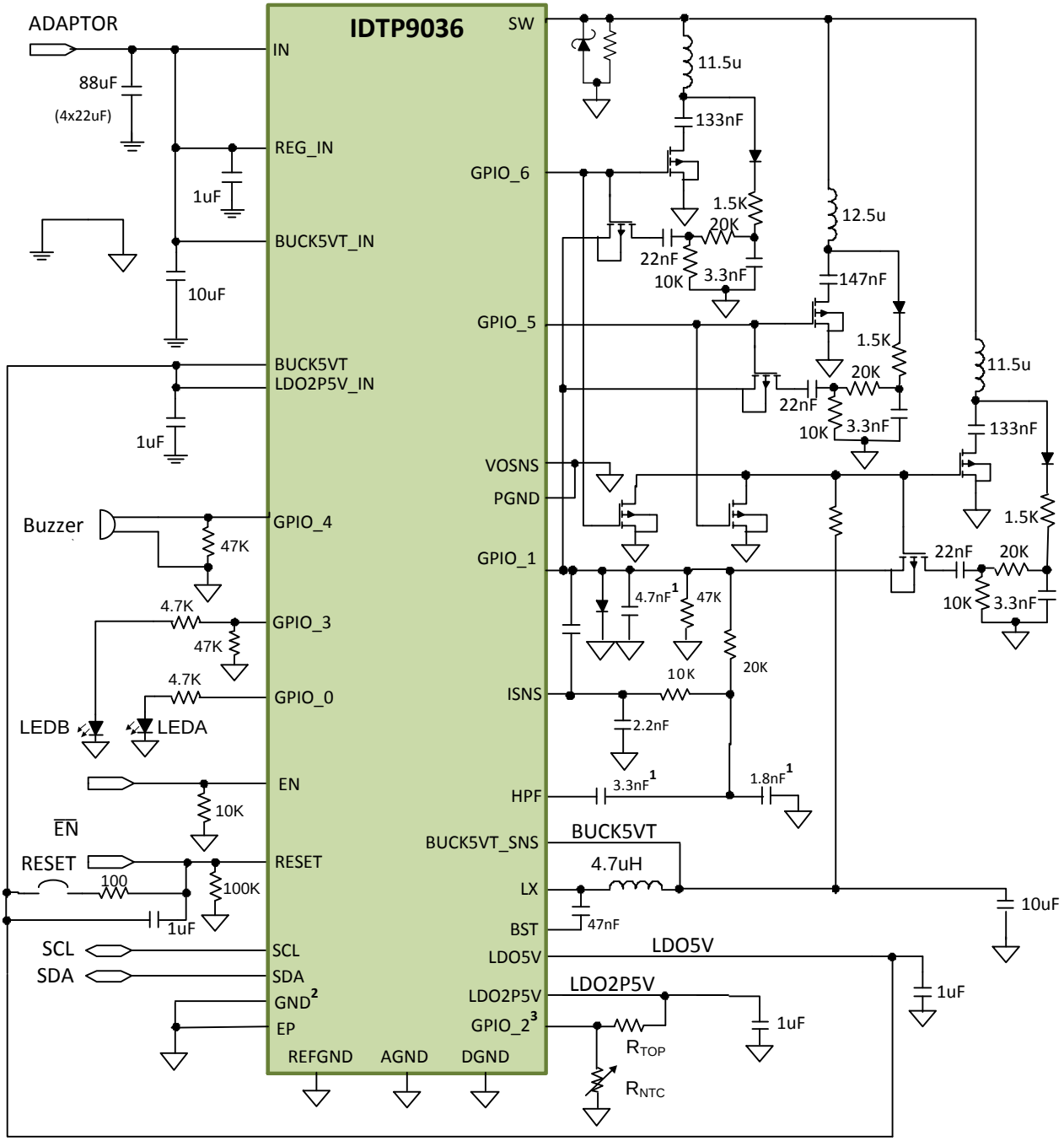


Figure 1. IDTP9036 Simplified Application Schematic

Note 1: NPO/C0G-type ceramic capacitor.
Note 2: For PCB layout, use single-point reference ("star" ground), refer to design schematic in Figure 8.
Note 3: In circuit at GPIO_2, R_{TOP} is required to linearize the temperature range of the thermistor, R_{NTC}. Please contact IDT for a spreadsheet calculator to guide thermistor selection.

ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9036 at absolute maximum ratings is not implied. Application of the absolute maximum rating conditions affects device reliability.

Table 1. Absolute Maximum Ratings Summary. All voltages are referred to ground, unless otherwise noted.

PINS	MAXIMUM RATING	UNITS
BUCK5VT_IN, IN, REG_IN **(THESE PINS MUST BE CONNECTED TOGETHER AT ALL TIMES.)**	-0.3 to 24	V
$\overline{EN}$, LX, SW	-0.3 to VIN+0.3	V
BST	-0.3 to VIN+5	V
LDO2P5V	-0.3 to 2.75	V
AGND, DGND, PGND, REFGND	-0.3 to +0.3	V
BUCK5VT_SNS, BUCK5VT, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_6, HPF, ISNS, LDO2P5V_IN, LDO5V, RESET, SCL, SDA, VOSNS	-0.3 to +6.0	V

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	MAXIMUM RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient (NTG48 - TQFN)	30.8	°C/W
θ_{JC}	Thermal Resistance Junction to Case (NTG48 - TQFN)	14.6	°C/W
θ_{JB}[2]	Thermal Resistance Junction to Board (NTG48 - TQFN)	0.75	°C/W
T_J	Junction Temperature	-40 to +150	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Note 4: For the NTG48 package, connecting the 4.1 mm X 4.1 mm EP to internal/external ground planes with a 5x5 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

Table 3. ESD Information

TEST MODEL	PINS	MAXIMUM RATINGS	UNITS
HBM	All	±2000	V
CDM	All	±500	V

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, IN = REG_IN = BUCK5VT_IN = 12V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Half-Bridge Inverter						
V_{IN}	Input Supply Operating Voltage Range[1]		11.4	12	12.6	V
I_{IN}[2] I_{IN_A}	Standby Input Current	After power-up sequence complete, average including pinging.		24		mA
I_{IN}[2] I_{IN_S}	Sleep Mode Input Current	$\overline{EN}$ = 5V to V_{IN}		460	600	µA
F_{SW_LOW}	Switching Frequency at SW	WPC-compliant Operating Range	115			kHz
F_{SW_HIGH}					205	kHz
$R_{DS(ON)\_HS}$		Between IN and SW		165		mΩ
$R_{DS(ON)\_LS}$		Between SW and PGND		130		mΩ
UVLO and Inverter OCP						
V_{IN_UVLO}	Under-Voltage Protection Trip Point	V_{IN} rising			10.3	V
		V_{IN} falling	9.0			
		Hysteresis		625		mV
I_{IN_OCP}	Over-Current Protection Trip Point	V_{IN} = 12.6V, cycle-by-cycle protection.	4		6	A
DC-DC Converter (For Biasing Internal Circuitry Only)[3]						
$V_{BUCK5VT\_IN}$	Input Voltage Range[1]		11.4		12.6	V
$V_{BUCK5VT}$	Output Voltage	External I_{Load} = 8mA	4.5	5	5.5	V
I_{OUT}[5]	External Load				8	mA
F_{SW}	Switching Frequency at LX			1.5		MHz
Low Drop Out Regulators (For Biasing Internal Circuitry Only)[3]						
LDO2P5V[3]						
$V_{LDO2P5V\_IN}$	Input Voltage Range	Supplied from BUCK5VT		5		V
$V_{LDO2P5V}$	Output Voltage	I_{Load} = 2mA		2.5		V
I_{OUT}	External Load				8	mA
LDO5V[3]						
V_{REG_IN}	Input Voltage Range	See Note 1.	11.4		12.6	V
V_{LDO5V}	Output Voltage	I_{Load} = 2mA		5		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Temperature Rising Threshold		140		°C
		Temperature Falling Threshold		110		

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, IN = REG_IN = BUCK5VT_IN = 12V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{EN}$						
V_{IH}				900		mV
V_{IL}				550		mV
$I_{\overline{EN}}$	$\overline{EN}$ input current	$V_{\overline{EN}}$ = 5V		7.5		µA
		$V_{\overline{EN}}$ = V_{IN} = 12.6V		35		µA
General Purpose Inputs / Outputs (GPIO)						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
V_{OH}	Output Logic High	I_{OH}=-8mA	4			V
V_{OL}	Output Logic Low	I_{OL}=8mA			0.5	V
I_{OH}	Output Current High		-8			mA
I_{OL}	Output Current Low				8	mA
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
SCL, SDA (I^2C Interface)						
f_{SCL}	Clock Frequency	EEPROM loading, Step 1, IDTP9036 as Master		100		kHz
f_{SCL}	Clock Frequency	EEPROM loading, Step 2, IDTP9036 as Master		300		kHz
f_{SCL}	Clock Frequency	IDTP9036 as Slave	0		400	kHz
$t_{HD;STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD;DAT}$	Data Hold Time	I^2C-bus devices	10			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition		100			ns

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, IN = REG_IN = BUCK5VT_IN = 12V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance[5]			5		pF
V_{IL}	Input Threshold Low	When powered by device 5V			1.5	V
V_{IH}	Input Threshold High		3.5			V
I_{LKG}	Leakage Current		-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I_{PD}= 2mA (Note 1)			0.5	V
I_{OH}	Output Current High		-2			mA
I_{OL}	Output Current Low				2	mA
Analog-to-Digital Converter						
N	ADC Conversion Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			62.5		kSPS
Channel	Number of Channels at ADC MUX input			8		
ADC_{CLK}	ADC Clock Frequency			1		MHz
V_{IN_FS}	Full-Scale Input Voltage			2.39		V
Microcontroller						
F_{CLOCK}	Clock Frequency			40		MHz
V_{MCU}	MCU Supply Voltage from internal 2.5V LDO			2.5		V

Note 1: BUCK5VT_IN, IN, REG_IN. These pins must be connected together at all times.

Note 2: This current is the sum of the input currents for IN, REG_IN and BUCK5VT_IN.

Note 3: DC-DC BUCK5VT, LDO2P5V and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, thermistor, LED, buzzer and pull-up resistor loads (up to an absolute maximum of 8mA), as recommended in Figure 8 WPC "Qi" Compliance Schematic and Table 7 WPC "Qi" Compliance Bill of Materials. If any of these outputs is used to power external loads, the performance of the IDTP9036 is not guaranteed.

Note 4: Any of the GPIO pins is capable of supplying 8mA, but if more than one is sourcing current, the total current available is 8mA.

Note 5: The 2.5V LDO is powered by the 5V DC/DC converter, so the LDO's output current must be counted in the output current budget of the DC/DC converter.

PIN CONFIGURATION

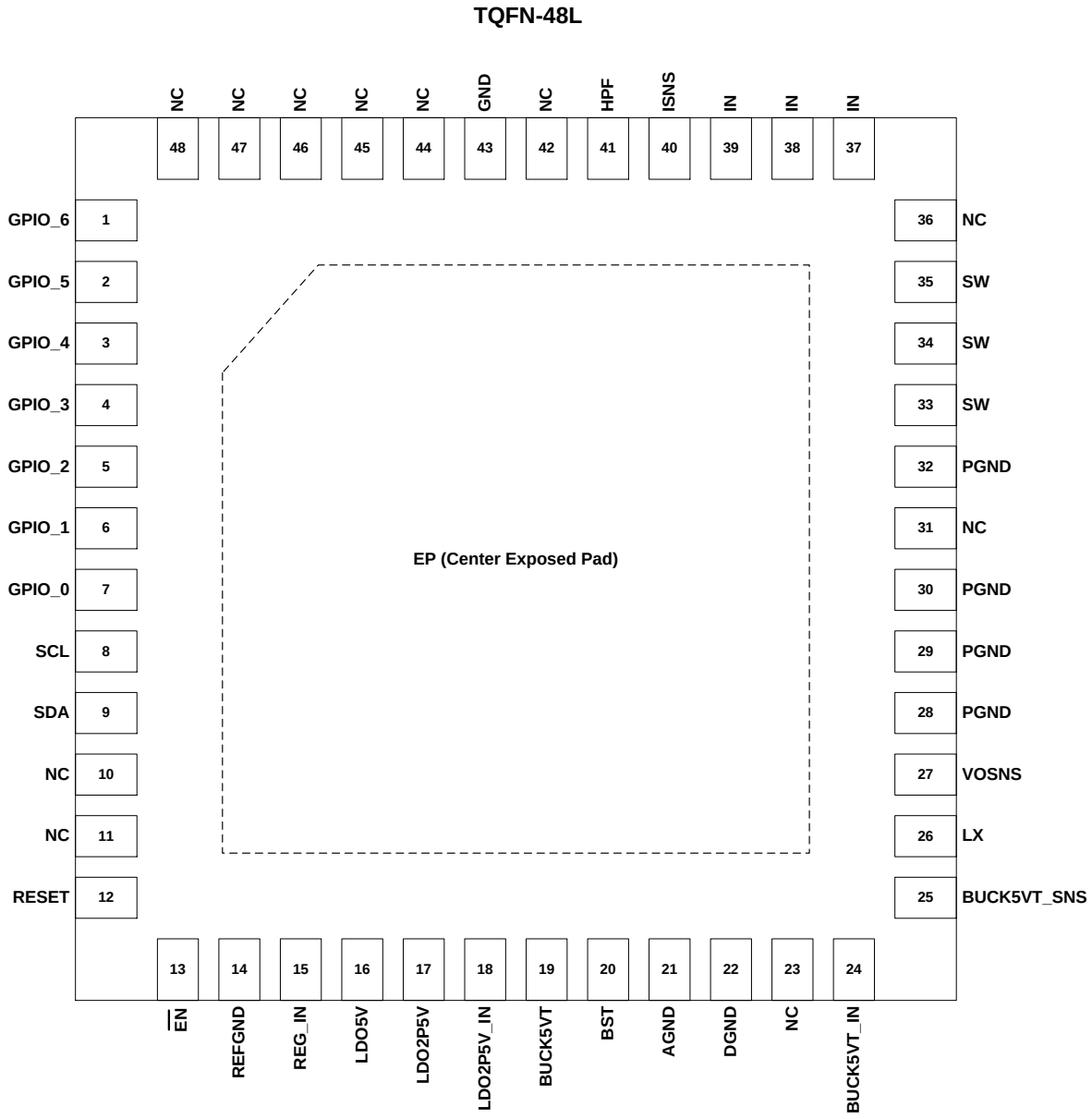


Figure 2. IDTP9036 Pin Configuration (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm, 0.4mm pitch)

PIN DESCRIPTION

Table 5. IDTP9036 NTG48 Package Pin Functions by Pin Number ()

1	GPIO_6	I/O	General purpose input/output 6
2	GPIO_5	I/O	General purpose input/output 5
3	GPIO_4	I/O	General purpose input/output 4
4	GPIO_3	I/O	General purpose input/output 3
5	GPIO_2	I/O	General purpose input/output 2
6	GPIO_1	I/O	General purpose input/output 1
7	GPIO_0	I/O	General purpose input/output 0
8	SCL	I/O	I^2C clock
9	SDA	I/O	I^2C data
10	NC	NC	Must be connected to GND.
11	NC	NC	Must be left unconnected.
12	RESET	I	Active-high chip reset pin. A 1µF ceramic capacitor must be connected between this pin and LDO5V, and a 100kΩ resistor to GND.
13	$\overline{EN}$	I	Active-low enable pin. Device is suspended and placed in low current (sleep) mode when pulled high. Tie to GND for stand-alone operation.
14	REFGND	-	Signal ground connection. Must be connected to AGND.
15	REG_IN[1]	I	LDO5V power supply input. A 1µF ceramic capacitor must be connected between this pin and GND. This pin must be connected to pins 37, 38, and 39.
16	LDO5V[2]	O	5V LDO output. A 1µF ceramic capacitor must be connected between this pin and GND.
17	LDO2P5V[2]	O	2.5V LDO output. A 1µF ceramic capacitor must be connected between this pin and GND.
18	LDO2P5V_IN	I	2.5V LDO input. The LDO2P5V_IN input must be connected to BUCK5VT. A 1µF ceramic capacitor must be connected between this pin and GND.
19	BUCK5VT[2]	I	Power and digital supply input to internal circuitry.

Table 5. IDTP9036 NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
20	BST	I	Bootstrap pin for BUCK converter top switch gate drive supply.
21	AGND	-	Analog ground connection. Connect to signal ground. Must be connected to REFGND.
22	DGND	-	Digital ground connection. Must be connected to GND.
23	NC	NC	Not internally connected. Must be left unconnected.
24	BUCK5VT_IN[1]	I	Buck converter power supply input. Connect 0.1µF and 1µF ceramic capacitors between this pin and PGND.. This pin must be connected to pins 37, 38, and 39.
25	BUCK5VT_SNS	I	Buck regulator feedback. Connect to the high side of the buck converter output capacitor.
26	LX	O	Switch Node of BUCK converter. Connects to one of the inductor's terminals.
27	VOSNS	I	Coil voltage sense input. Not used. Connect to ground.
28	PGND	-	Power ground.
29	PGND	-	Power ground.
30	PGND	-	Power ground.
31	NC	NC	Not internally connected. Must be left unconnected.
32	PGND	-	Power ground.
33	SW	O	Inverter switch node. Pins 33, 34, and 35 must be connected together. Must be connected to TX-A6 coils.
34	SW	O	
35	SW	O	
36	NC	NC	Not internally connected. Must be left unconnected.
37	IN[1]	I	Inverter power supply input. Connect at least four 22µF x 25V ceramic capacitors and a 0.1µF capacitor between this pin and ground, as close to the pin as possible. Connect all three pins (37, 38, 39) in parallel.
38	IN[1]	I	
39	IN[1]	I	
40	ISNS	O	ISNS output signal

Table 5. IDTP9036 NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
41	HPF	I	High pass filter input
42	NC		Internal connection, must be connected to GND.
43	GND	-	Ground
44	NC		Internal connection, must be connected to GND.
45	NC		Internal connection, must be connected to GND.
46	NC		Internal connection, must be connected to GND.
47	NC		Internal connection, must be connected to GND.
48	NC		Internal connection. Must be left unconnected.
EP	Center Exposed Pad	Thermal	EP is on the bottom of the package and must be electrically tied to GND. For good thermal performance, solder to a large copper pad embedded with a pattern of plated through-hole vias. The die is not electrically bonded to the EP, and the EP must not be used as a current-carrying electrical connection.

Note 1: IN, REG_IN, BUCK5VT_IN. These pins must be connected together at all times.

Note 2: DC-DC BUCK5VT, LDO2P5V and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, thermistor, LED, buzzer and pull up resistor loads (up to an absolute maximum of 8mA), as recommended in Figure 8 WPC "Qi" Compliance Schematic and Table 7 WPC "Qi" Compliance Bill of Materials.

TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{EN}$ = RESET = 0, IN = REG_IN = BUCK5VT_IN = 12V, TA = 25°C, unless otherwise noted.

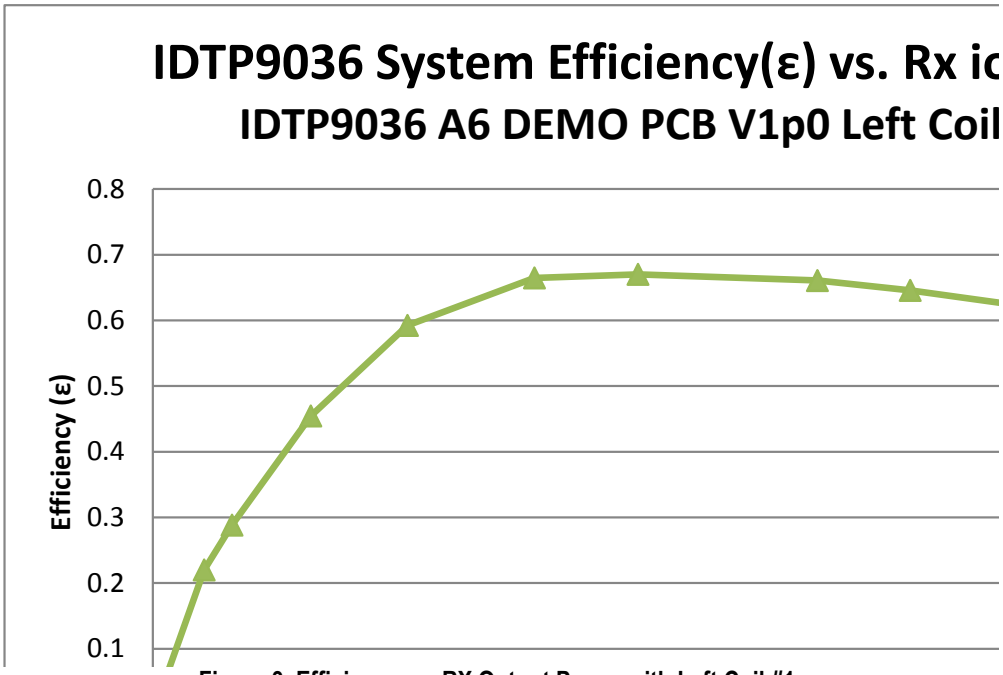


Figure 3. Efficiency vs. RX Output Power with Left Coil #1

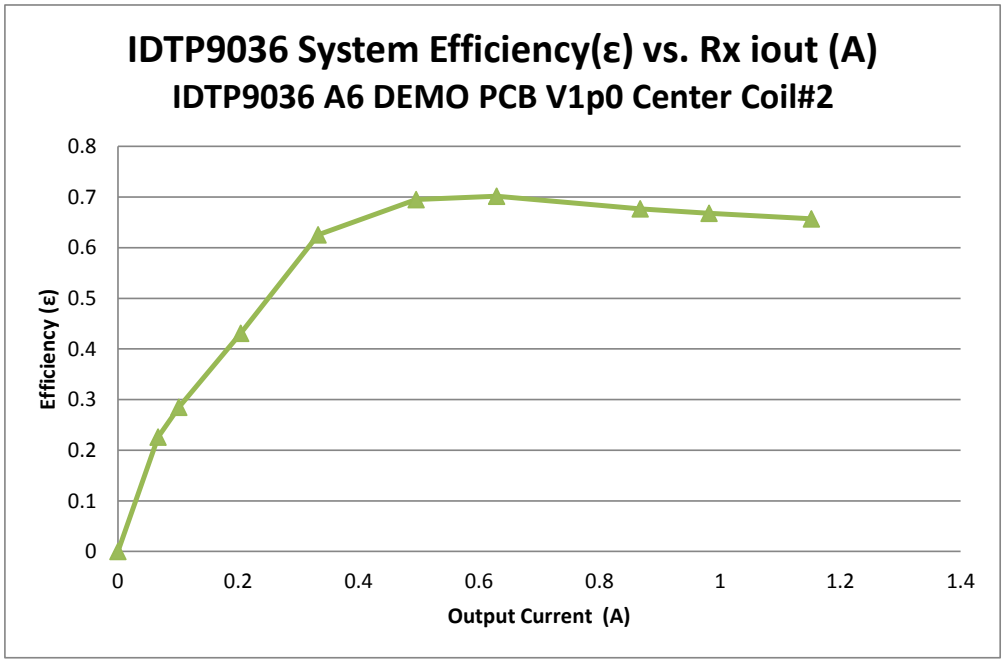


Figure 4. Efficiency vs. RX Output Power with Center Coil #2

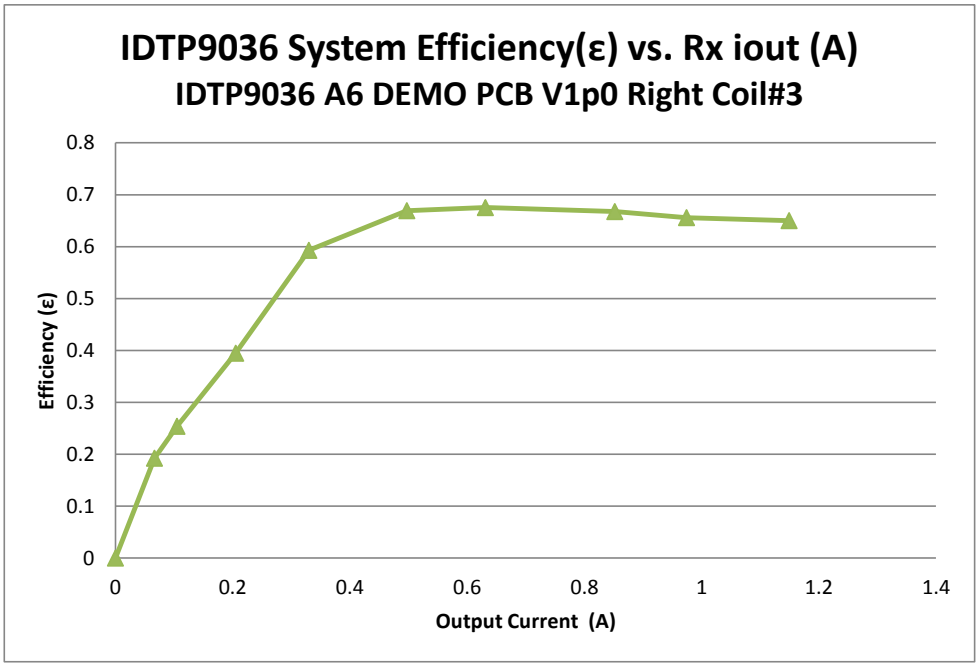


Figure 5. Efficiency vs. RX Output Power with Right Coil #3

SIMPLIFIED SYSTEMS APPLICATIONS DIAGRAM

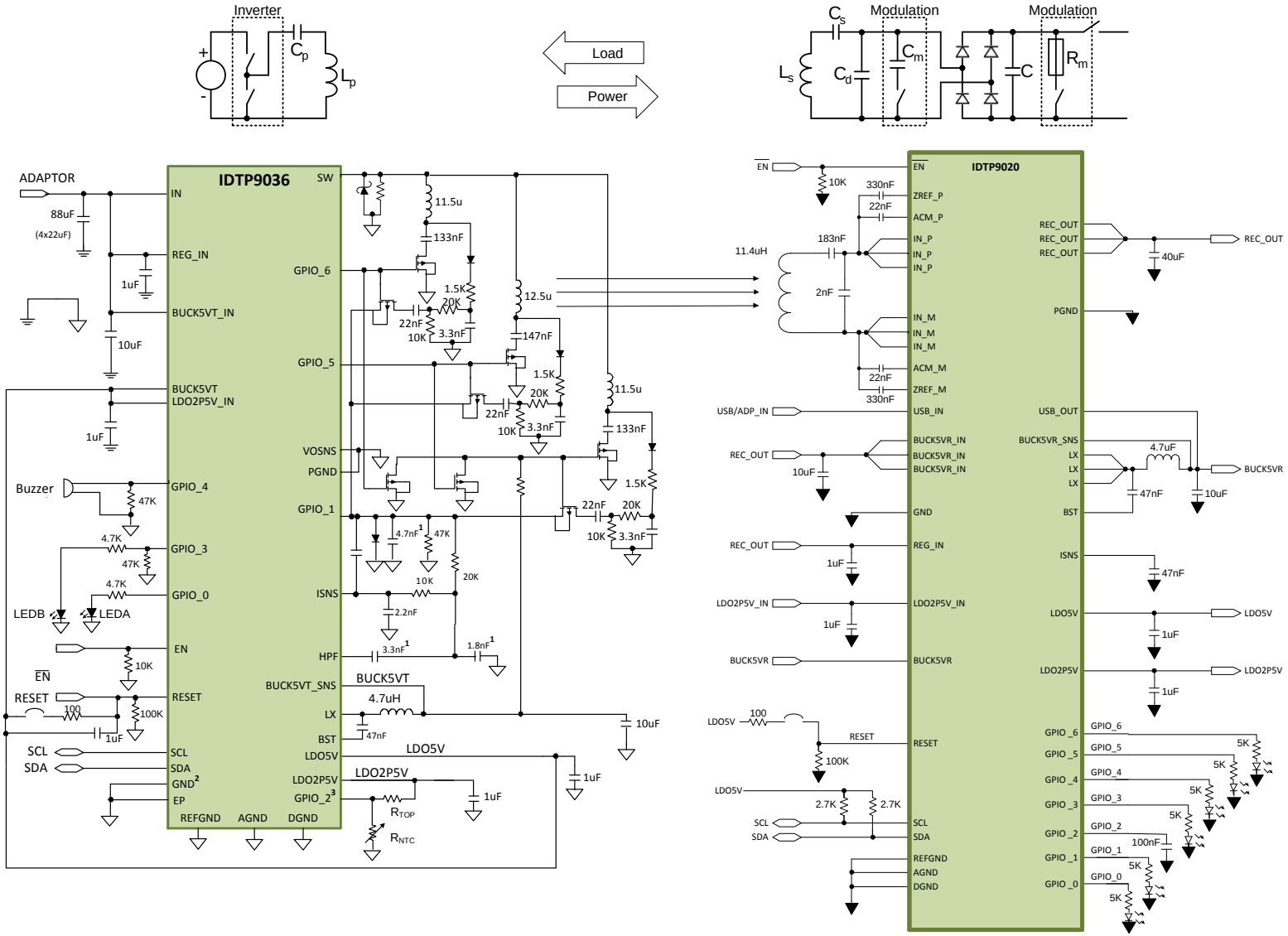


Figure 3. IDTP9036/IDTP9020 Simplified Systems Application Diagram

BLOCK DIAGRAM

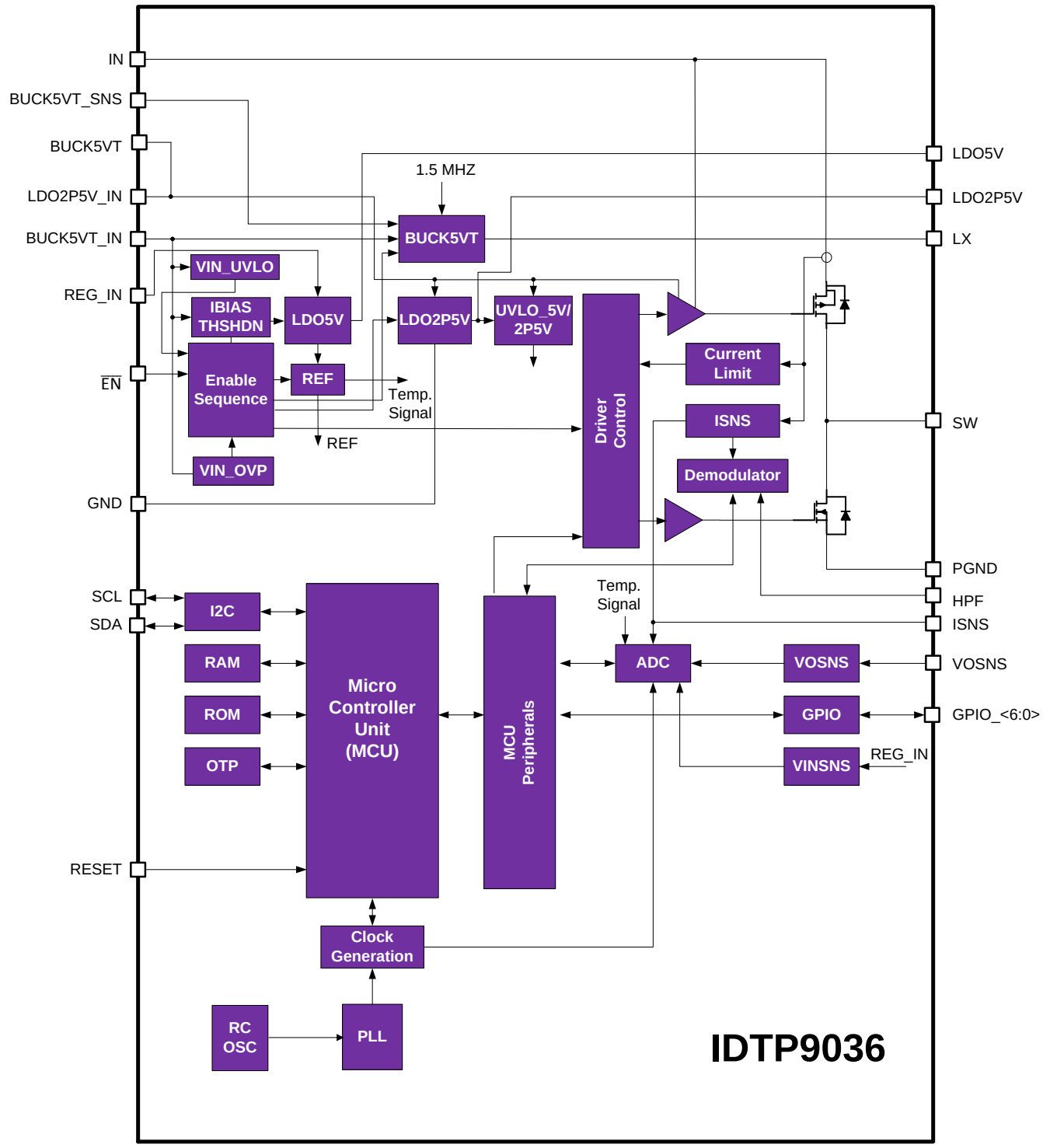


Figure 4. IDTP9036 Internal Functional Block Diagram

THEORY OF OPERATION

The IDTP9036 is a highly-integrated WPC[1] (Wireless Power Consortium)-compliant wireless power charging IC solution for the transmitter base station. It can deliver more than 5W of power to the receiver when used with the IDTP9020 or 5W in WPC "Qi" mode using near-field magnetic induction as a means to transfer energy. It is the industry's first 12V single-chip WPC-compliant solution designed to drive a WPC-compliant Type-A6 transmitter coil.

OVERVIEW

Figure 4 shows the block diagram of the IDTP9036. When the VIN_UVLO block detects that the voltage at IN, REG_IN, and BUCK5VT_IN (all connected together externally) is above the Vin_rising threshold and $\overline{EN}$ is at a logic LOW, the Enable Sequence circuitry activates the voltage reference, the 5V and 2.5V LDOs, the 5V buck switching regulator, and the Driver Control for the output inverter.

The voltages at the outputs of the LDOs and the buck regulator are monitored to ensure that they remain in regulation, and the adaptor voltage, coil current, and internal temperature are monitored.

The Driver Control block converts a PWM signal (generated by the digital block and the MCU) to the gate drive signals required by the output inverter to drive the external field-generating coil.

Communication packets from the receiver in the mobile device are recovered by the Demodulator and converted to digital signals that can be read by the MCU.

Several internal voltages and the external thermistor voltage (through GPIO2) are digitized by the ADC and supplied to the MCU.

Four GPIO ports are available to the system designer for measuring an external temperature (ambient or inductor, for example) and driving LEDs and a buzzer.

The clock for the MCU and other circuitry is generated by an internal RC oscillator.

I²C SDA and SCL pins permit communication with an external device or host.

Note 1 - Refer to the WPC specification at http://www.wirelesspowerconsortium.com/ for the most current information

UNDER VOLTAGE LOCKOUT (UVLO)

The IDTP9036 has a built-in UVLO circuit that monitors the input voltage and enables normal operation, as shown in Figure 5.

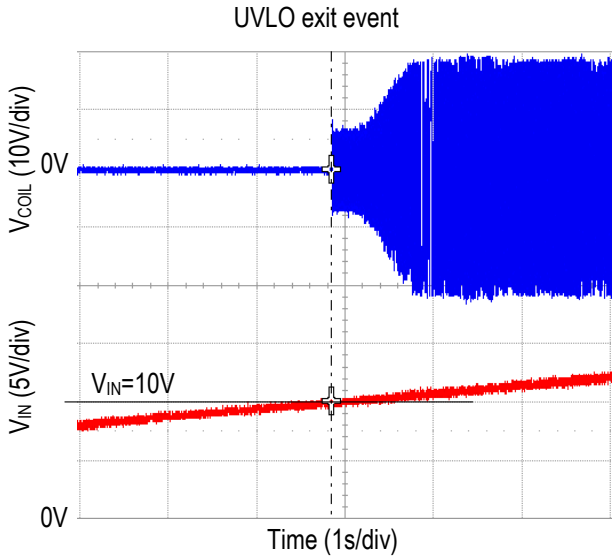


Figure 5. V_{IN} versus UVLO threshold with /EN low.

OVER-CURRENT/TEMPERATURE PROTECTION

The current in the inverter is monitored by an analog Current Limit block. If the instantaneous coil current exceeds the OCP level, the upper switch in the inverter will be turned off and the lower switch will be turned on for the remainder of the cycle. The internal temperature is also monitored, and the part is temporarily deactivated if the temperature exceeds 140°C and reactivated when the temperature falls below 110°C.

DRIVER CONTROL BLOCK and INVERTER

The Driver Control block contains the logic, shoot-through protection, and gate drivers for the on-chip power FETs. The FETs are configured as a very large inverter that switches the SW pin between the voltage at IN and ground at a rate set by the MCU.

DEMODULATOR

Power is transferred from the transmitter to the receiver through the coupling of their respective coils: a loosely-coupled transformer. The amount of power transferred is determined by the transmitter's switching frequency (115kHz-205kHz, by WPC[1]), and is controlled by the receiver through instructions the receiver sends back through the coils to the transmitter to change its frequency, end power transfer, or do something else. The instructions take the form of data packets, which are coupled through a series of filters connected to the IDTP9036's Demodulator through the HPF pin. Recovering the data packets is the function of the Demodulator. Decoding and executing the packets is one of the functions of the MCU.

MICRO-CONTROLLER UNIT (MCU)

The IDTP9036's MCU processes the algorithm, commands, and data that control the power transferred to the reciever. The MCU is provided with RAM and ROM, and parametric trim and operational modes are set at the factory through the One-Time Programming (OTP) block, read by the MCU at power-up. Communication with external memory is performed through I²C via the SCL and SDA pins.

APPLICATIONS INFORMATION

The recommended applications schematic diagram is shown in Figure 8. The IDTP9036 operates with a $12V_{DC}$ (±5%) input. The switching frequency varies from 115kHz to 205kHz. At the 205kHz limit the duty cycle is also variable. The power transfer is controlled via changes in switching frequency and duty cycle. The base or TX-side has three series resonance circuits made of a WPC Type-A6 triple coil. Two of the coils are 11.5µH each, and the other one is 12.5µH, each with a series resonant capacitor (~133nF or 147nF). The resonant circuits are driven by a half-bridge inverter, as shown in Figure 6. Only the resonant circuit that is aligned with a receiver coil gets a complete path from the inverter output to power ground. The selection is made by voltage levels from GPIO5 and GPIO6, each of which drives a selection FET directly and drives an input of a wired-NAND circuit that activates or de-activates the third resonant circuit.

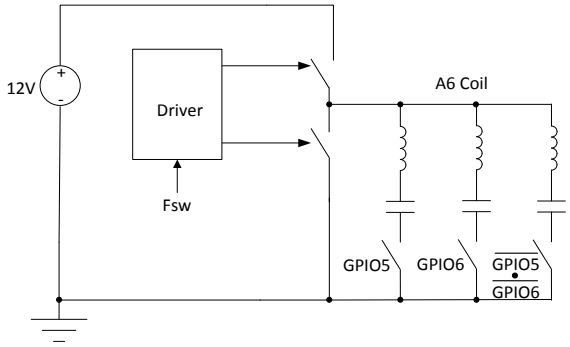


Figure 6. Half Bridge inverter TX Coil Driver.

EXTERNAL CHIP RESET and $\overline{EN}$

The IDTP9036 can be externally reset by pulling the RESET pin to a logic high above the V_{IH} level.

The RESET pin is a dedicated high-impedance active-high digital input, and its effect is similar to the power-up reset function. Because of the internal low-voltage monitoring scheme, the use of the external RESET pin is not mandatory. A manual external reset scheme can be added by connecting 5V to the RESET pin through a simple switch. When RESET is HIGH, the microcontroller's registers are set to the default configuration. When the RESET pin is released to a LOW, the microcontroller starts executing the code from the boot address.

If the particular application requires the IDTP9036 to be disabled, this can be accomplished with the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active.

The current into $\overline{EN}$ is approximately

$$I(\overline{EN}) = \frac{V(\overline{EN}-2V)}{300k},$$

or close to zero if V($\overline{EN}$) is less than 2V.

SYSTEM FEEDBACK CONTROL (WPC)

The IDTP9036 contains logic to demodulate and decode error packets sent by the mobile device (Rx-side), and adjusts power transfer accordingly. The IDTP9036 varies the switching frequency of the half bridge inverter between 115kHz to 205 kHz to adjust power transfer. The mobile device controls the amount of power transferred via a communication link that exists from the mobile device to the base station. The mobile device (IDTP9020 or another WPC-compliant receiver) communicates with the

IDTP9036 via Communication Packets. Each packet has the following format:

Table 6 – Data Packet Format.

Preamble	Header	Message	Checksum

The overall system behavior between the transmitter and receiver follows the state machine diagram below:

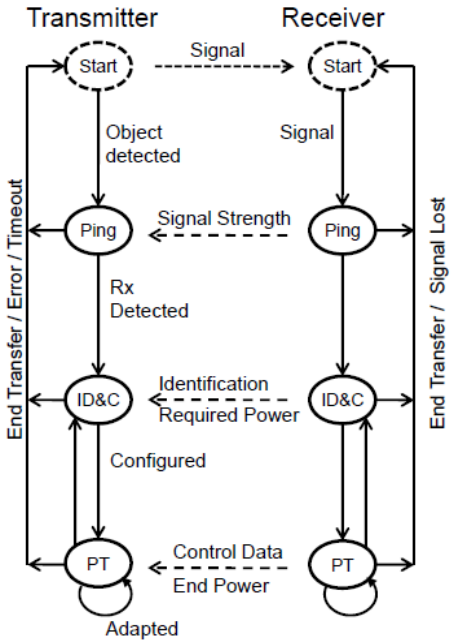


Figure 7. System state machine diagram

The IDTP9036 performs four phases: Selection, Ping, Identification & Configuration, and Power Transfer.

START (SELECTION) PHASE

In this phase, the IDTP9036 operates in a low power mode to determine if a potential receiver has been placed on the coil surface prior to the PING state. Twice a second, the IDTP9036 applies a brief AC signal to its coil and listens for a response.

PING PHASE

In this phase, the IDTP9036 applies a power signal at 175 kHz with a fixed 50% duty cycle and attempts to establish a communication link with a mobile device.

Required packet(s) in PING:

1. Signal Strength Packet (0x01)

The mobile device must send a Signal Strength Packet within a time period specified by the WPC, otherwise the power signal is terminated and the process repeats.

The mobile device calculates the Signal Strength Packet value, which is an unsigned integer value between 0-255, based on this formula:

$$Signal\ Strength\ Value = \left(\frac{U}{U_{max}}\right).256$$

where U is a monitored variable (i.e. rectified voltage/current/power) and U_{max} is a maximum value of that monitored variable expected during the digital ping phase at 175 kHz.

If the IDTP9036 does not detect the start bit of the header byte of the Signal Strength Packet during the Ping Phase, it removes the Power Signal after a delay. If a Signal Strength Packet is received, the IDTP9036 goes to the Identification and Configuration Phase. If the IDTP9036 does not move to the Identification and Configuration Phase after receiving the Signal Strength Packet, or if a packet other than a Signal Strength Packet is received, then power is terminated.

IDENTIFICATION AND CONFIGURATION (ID & Config)

In this phase, the IDTP9036 tries to identify the mobile device and collects configuration information.

Required packet(s) in ID & Config:

1. Identification Packet (0x71)
2. Extended Identification Packet (0x81)*
3. Configuration Packet (0x51)

* *If Ext bit of 0x71 packet is set to 1.*

Also, the IDTP9036 must correctly receive the following sequence of packets without changing the operating point (175 kHz @ 50% duty cycle):

1. Identification Packet (0x71)
2. Extented Identification (0x81)
3. Up to 7 optional configuration packets from the following set:
    a. Power Control Hold-Off Packet (0x06)
    b. Proprietary Packet (0x18 – 0xF2)
    c. Reserved Packet

4. Configuration Packet (0x51)

If the IDTP9036 does not detect the start bit of the header byte of the next packet in the sequence within a WPC-specified time after receiving the stop bit of the checksum byte of the preceding Signal Strength Packet, then the Power Signal is removed within after a delay. If a correct Control Packet in the above sequence is received late, or if Control Packets that are not in the sequence are received, the IDTP9036 removes the Power Signal after a delay.

POWER TRANSFER PHASE

In this phase, the IDTP9036 adapts the power transfer to the receiver based on control data it receives in Control Error Packets.

Required packet(s) in Power Transfer:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)

For this purpose, the IDTP9036 may receive zero or more of the following packets:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)
3. Charge Status Packet (0x05)
4. End Power Transfer Packet (0x02)
5. Any Proprietary Packet
6. Any reserved Packets

If the IDTP9036 does not correctly receive the first Control Error Packet in time, it removes the Power Signal after a delay. Because Control Error Packets come at a regular interval, the IDTP9036 expects a new Control Error Packet after receiving the stop bit of the checksum byte of the preceding Control Error Packet. If that does not happen, then the IDTP9036 removes the Power Signal. Similary, the IDTP9036 must receive a Rectified Power Packet within a WPC-specified time after receiving the stop bit of the checksum byte of the Configuration Packet (which was received earlier in the *identification and configuration* phase). Otherwise, it removes the Power Signal.

Upon receiving a Control Error value, the IDTP9036 makes adjustments to its operating point after a delay to enable the Primary Coil current to stabilize again after communication.

If the IDTP9036 correctly receives a packet that does not comply with the sequence, then it removes the Power Signal.

FOREIGN OBJECT DETECTION (FOD)

In addition to over-temperature protection, the IDTP9036 employs a proprietary FOD technique which detects foreign objects placed on the base station. The FOD algorithm is multi-layered and may issue warnings and/or change device operation depending on the severity of the warning.

FOD is an optional feature that is not included in the standard firmware. Please contact IDT to incorporate this feature into a specific product, indicating volume and business case.

APPLICATIONS INFORMATION

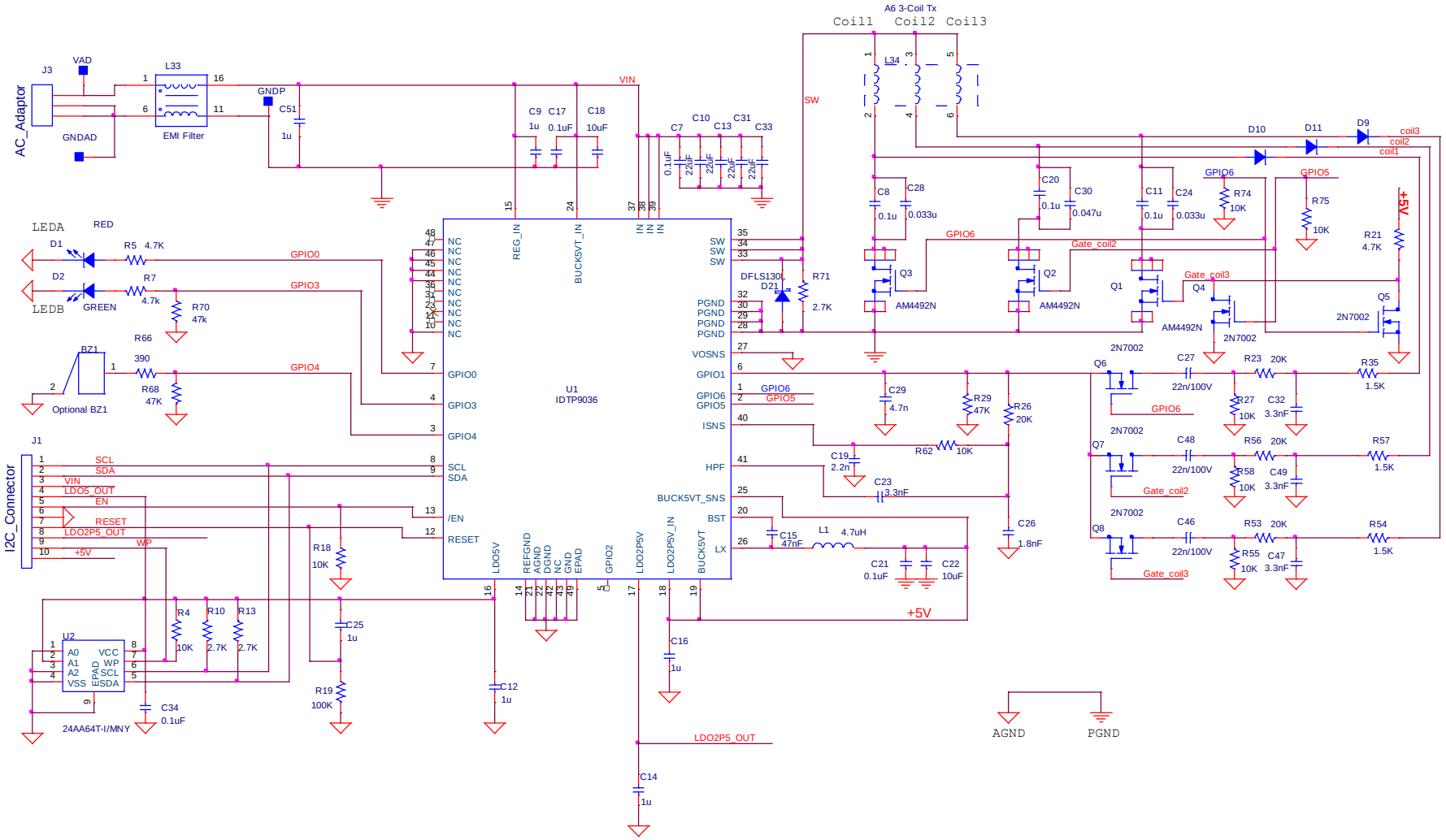


Figure 8. IDTP9036 WPC "Qi" Compliance Schematic (See IDTP9036 Evaluation Kit User Manual for complete details)

Table 7. IDTP9036 WPC "Qi" Compliance Bill of Materials

Item	Quantity	Reference	Part	Manufacturer	Part_Number	PCB Footprint
1	1	BZ1	BUZZER PIEZO 4KHZ	TDK	PS1240P02CT3	12.2MM PC MNT
2	1	C6	POSCON 100uF 16V 5%	Panasonic/Sanyo	16TQC100MYF	POSCON_D3
3	4	C7,C17,C21,C34	CAP CER 0.1UF 50V 10% X7R	Murata	GRM188R71H104KA93D	603
4	3	C8,C11,C20	CAP CER 0.1UF 100V 5% NP0	TDK	C4532C0G2A104J	1812
5	6	C9,C12,C14,C16,C25,C51	CAP CER 1UF 35V 10% X5R	Taiyo Yuden	GMK107BJ105KA-T	603
6	4	C10,C13,C31,C33	CAP CER 22UF 25V 10% X7R	Murata	GRM32ER71E226KE15L	1210
7	1	C15	CAP CER 0.047UF 16V 10% X7R	Murata	GRM188R71C473KA01D	603
8	1	C18	CAP CER 10UF 25V 20% X5R	TDK	C2012X5R1E106M	805
9	1	C19	CAP CER 2200PF 50V 10% X7R	Taiyo Yuden	UMK105B7222KV-F	402
10	1	C22	CAP CER 10UF 10V 10% X7R	Murata	GRM21BR71A106KE51L	805
11	1	C23	CAP CER 3300PF 50V 10% X7R	Murata	GRM155R71H332KA01D	402
12	1	C24	CAP CER 0.047UF 100V 5% NP0	TDK	C3225C0G2A473J	1210
13	1	C26	CAP CER 1800PF 50V 10% X7R	Murata	GRM155R71H182KA01D	402
14	3	C27,C46,C48	CAP CER 0.022UF 100V X7R	TDK	C1608X7R2A223K	603
15	2	C28,C30	CAP CER 0.033UF 100V 5% NP0	TDK	C3225C0G2A333J	1210
16	1	C29	CAP CER 4700PF 100V 10% X7S	TDK	C1005X7S2A472K	402
17	3	C32,C47,C49	CAP CER 1200PF 100V 5% NP0	TDK	C1608C0G2A122J	603
18	1	D1	LED SMARTLED 630NM RED	Osram	L29K-G1J2-1-0-2-R18-Z	0603_DIODE
19	1	D2	LED SMARTLED GREEN 570NM	Osram	LG L29K-G2J1-24-Z	0603_DIODE
20	1	D21	1.0A SCHOTTKY BARRIER RECTIFIER	Diodes Inc.	DFLS130L	PowerDI123
21	3	D9,D10,D11	DIODE SWITCH 200V 250MW	Diodes Inc.	BAV21W-7-F	SOD123
22	7	GND1,VIN,VAD,PGND,GNDP, GNDAD,GND	VC6	Keystone	5015	TEST_PT_SM_135X70
23	1	J1	CONN HEADER LOPRO STR 10POS GOLD	TE Connectivity	5103308-1	CON10
24	1	J3	CONN POWER JACK 2.1X5.5MM HI CUR	CUI Inc.	PJ-002AH	JACK_5MM
25	1	L1	4.7uH 10% 580mA	Coilcraft	XPL2010-472ME_	IND_2SQ_TO_3P3REC
26	1	L33	EMI Filter	Coilcraft	NA6054-CE	clcft_na6054
27	1	L34	WPC A6 3-Coil Tx	TDK	WT-1005660-12K2-A6-G	3coil_A6_WPC standard
				E&E	Y31-60054F	
28	3	Q1,Q2,Q3	N-Channel 100-V (D-S) MOSFET	Analog Power	AM4492N	SOIC8
29	5	Q4,Q5,Q6,Q7,Q8	MOSFET N-CHAN DUAL 60V SOT363	Fairchild	2N7002	SOT363
30	5	R4,R18,R62,R74,R75	RES 10.0K OHM 1/16W 1%	Yageo	RC0402FR-0710KL	402
31	3	R5,R7,R21	RES 4.99K OHM 1/10W 1%	Panasonic	ERJ-2RKF4991X	402
32	2	R10,R13	RES 2.7K OHM 1/10W 5%	Panasonic	ERJ-2GEJ272X	402
33	1	R19	RES 100K OHM 1/16W 1%	Yageo	RC0402FR-07100KL	402
34	1	R20	RES 100 OHM 1/16W 1%	Yageo	RC0402FR-07100RL	402
35	3	R23,R53,R56	RES 20.0K OHM 1/10W 1%	Panasonic	ERJ-3EKF2002V	603
36	1	R26	RES 20.0K OHM 1/10W 1%	Panasonic	ERJ-2RKF2002X	402
37	3	R27,R55,R58	RES 10.0K OHM 1/10W 1%	Panasonic	ERJ-3EKF1002V	603
38	3	R29,R68,R70	RES 47K OHM 1/10W 5%	Panasonic	ERJ-2GEJ473X	402
39	3	R35,R54,R57	RES 1.00K OHM 1/10W 1%	Panasonic	ERJ-3EKF1001V	603
40	1	R66	RES 390 OHM 1/10W 5%	Panasonic	ERJ-3GEYJ391V	603
41	1	R71	RES 2.7K OHM 1/10W 5%	Panasonic	ERJ-3GEYJ272V	603
42	2	R72,R73	RES 0.0 OHM 1/8W	Panasonic	ERJ-6GEY0R00V	805
43	1	S1	MOM SPST	Wurth	434 121 043 816	we_mom_spst_4341
44	1	U2	IC EEPROM 64KBIT 400KHZ	Microchip	24AA64T-I/MNY	TDFN8
45	1	U1	12V Wireless Transmitter IC for TX-A6	IDT	IDTP9036	48LD_6X6MM_0P4

Note 1: Recommended capacitor temperature/dielectric and voltage ratings: 100V capacitors are recommended because 100Vp-p voltage transients may appear on the resonance capacitors as stated in the WPC specification. C0G/NPO-type capacitor values stay relatively constant with voltage while X7R and X5R ceramic capacitor values de-rate from 40% to over 80%. The decision to use lower voltage 50V capacitors or other type temperature/dielectric capacitors is left to the end user.

External Components

The IDTP9036 requires a minimum number of external components for proper operation (see the BOM in Table 7). A complete design schematic compliant to the WPC "Qi" standard is given in Figure 8. It includes WPC "Qi" LED signaling, buzzer, thermistor circuit, and EEPROM for loading IDTP9036 firmware.

I²C Communication

The IDTP9036 includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the IDTP9036 will initially become I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the IDTP9036 does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the IDTP9036 has finished

any firmware uploading and has released control of the bus as I²C Master. After any firmware uploading from external memory is complete, and when the IDTP9036 begins normal operation, the IDTP9036 is normally configured by the firmware to be exclusively in I²C Slave mode.

For maximum flexibility, the IDTP9036 tries to communicate with the first address on the EEPROM at 100kHz. If no ACK is received, communication is attempted at the other addresses at 300kHz.

EEPROM

The IDTP9036 could use an external EEPROM which contains either standard or custom TX firmware. The external EEPROM memory chip is pre-programmed with a standard start-up program that is automatically loaded when 12V power is applied. The IDTP9036 uses I²C slave address 0x52 to access the EEPROM. The IDTP9036 slave address is 0x39. The EEPROM can be reprogrammed to suit the needs of a specific application using the IDTP9036 software tool (see the IDTP9036-Qi Demo Board User Manual for complete details). The IC will look initially for an external EEPROM and use the firmware built into the IC ROM only if no external memory device is found. A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard default/built-in firmware is not suitable for the application, custom ROM options are possible. Please contact IDT sales for more information. IDT will provide the appropriate image in the format best suited to the application.

Overview of Standard GPIO Usage

There are 7 GPIO's on the IDTP9036 transmitter IC, of which four are available for use as follows:

- GPIO0: Red LED_A to indicate standby, fault conditions, and FOD warnings; see table 7.
- GPIO2: Temperature sensor input. Contact IDT for a spreadsheet facilitating selection and use of thermistors.
- GPIO3: Green LED_B to indicate standby, power transfer, and power complete. Table 8 lists how the red and green LEDs can be used to display information about the IDTP9036's operating modes. The table also includes information about external resistors or internal pull up/down options to select LED modes. Eight of the ten LED modes (those associated with advanced charging modes) are currently designated as "Future" modes.
- GPIO4: AC or DC buzzer (optional) with resistor options for different buzzer .

LED FUNCTIONS

Two GPIOs are used to drive LEDs which indicate, through various on/off and illumination options, the state of charging and some possible fault conditions.

A red LED indicates various Fault and FOD ("Foreign Object Detection") states. The green LED indicates Power Transfer and Charge Complete state information. Upon power up, the two LEDs together may optionally indicate the Standby State and remain in this state until another of the defined Operational States occurs

As shown in Figure 9, one or two resistors configure the defined LED option combinations. The DC voltage set in this way is read one time during power-on to determine the LED configuration. To avoid interfering with the LED operation, the useful DC voltage range must be limited to not greater than 1Vdc.

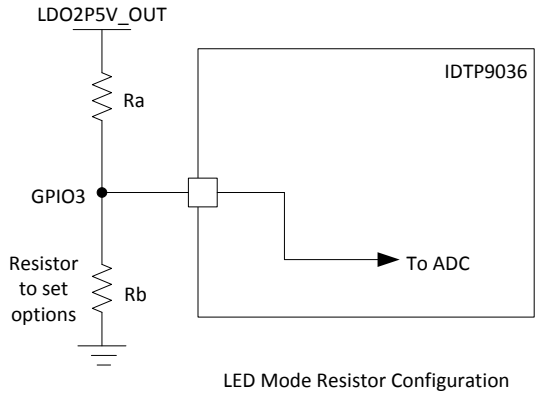


Figure 9. IDTP9036 LED Resistor Options.

LED Pattern Operational Status Definitions:

Blink Slow, Fast, repeat.

Table 8 – IDTP9036 LED Resistor Optioning (Not all options supported, shaded rows are for future development).

LED Control Option	LED Select Resistor Value	Description	LED #/ Color	Operational Status				FOD Warning
				Standby	Transfer	Complete	Condition	
1	Pull Down	Standby LEDs ON	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
2	R1	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
3	R2	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
4	R3	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
5	R4	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
6	Pull Up	Standby LEDs OFF	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
7	R5	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
8	R6	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
9	R7	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
10	R8	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST

R1-R8 are created using combination of two 1% resistors.

Designates Future Option

Buzzer Function

An optional buzzer feature is supported on GPIO4. The default configuration is an "AC" buzzer. The signal is created by toggling GPIO4 active-high/active-low at a 2kHz frequency.

Buzzer Action: Power Transfer Indication

The IDTP9036 supports audible notification when the device operation successfully reaches the Power Transfer state. The duration of the power transfer indication sound is 400ms.

The latency between reaching the Power Transfer state and sounding the buzzer does not exceed 500ms. Additionally, the buzzer sound is concurrent within ±250ms of any change to the LED configuration indicating the start of power transfer.

Buzzer Action: No Power Transfer due to Foreign Object Detected (FOD)

When a major FOD situation is detected such that, for safety reasons, power transfer is not initiated, or that power transfer is terminated, the buzzer is sounded in a repeating sequence:

For 30 seconds: 400ms ON, 800ms OFF, repeat
Next 30 seconds: Off/silence (but no change to LED on/off patterns)
The pattern is repeated while the error condition exists

The buzzer is synchronized with the FOD LED such that the 400ms on tone corresponds with the red LED illumination and 800ms off (no sound) corresponds with the red LED being off.

Decoupling/Bulk Capacitors

As with any high-performance mixed-signal IC, the IDTP9036 must be isolated from the system power supply noise to perform optimally. A decoupling capacitor of 0.1µF must be connected between each power supply and the PCB ground plane as close to these pins as possible. For optimum device performance, the decoupling capacitor must be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit. Additionally, medium value capacitors in the 22µF range must be used at the VIN input to minimize ripple current and voltage droop due to the large current requirements of the resonant half Half-Bridge driver. At least four 22µF

capacitors must be used close to the IN pins of the device. Since the operating voltage is 11.4V to 12.6V, the value of the capacitors will decrease due to voltage derating characteristics. For example, a 22µF X7R 25V capacitor's value is actually 6µF when operating at 13V.

There must also be an 82µF to 100µF bulk capacitor connected at the node where the input voltage to the board is applied. A 100µF 16V POSCON or aluminum electrolytic must be connected between the input supply and ground as shown in Figure 20. POSCON capacitors have much lower ESR than aluminum electrolytic capacitors and will reduce voltage ripple.

ADC Considerations

The GPIO pins are connected internally to a successive approximation ADC with a multiplexed input. The GPIO pins that are connected to the ADC have limited input range, so attention must be paid to the maximum VIN (2.4V). 0.01µF decoupling capacitors can be added to the GPIO inputs to minimize noise.

WPC TX-A6 Coil

The SW pin connects to a series-resonance circuit comprising a WPC triple Type-A6 coil (two 11.5µH side coils and one 12.5µH center coil) and series resonant capacitors (total value 133nF for the two side coils and total value 147nF for the center coil). The inductor serves as the primary coil in a loosely-coupled transformer, the secondary of which is the inductor connected to the power receiver (IDTP9020 or another).

The TX-A6 power transmitter coils are mounted on a ferrite shield to reduce EMI. The coil assembly can be mounted next to the IDTP9036. Either ground plane or grounded copper shielding can be added beneath the ferrite shield for added reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the IDTP9036 ground plane by a single trace.

Resonance Capacitors

The resonance capacitors must be C0G type dielectric and have a DC rating to 100V. Use one 33nF and one 100nF capacitor for each side coil, and one 47nF and one 100nF capacitor for the center coil. The part numbers are shown in Table 7.

Buck Converter

The input capacitors (C_{IN}) must be connected directly between the power V_{IN} and power PGND pins. The output capacitor (C_{OUT}) and power ground must be connected together to minimize any DC regulation errors caused by ground potential differences.

The bootstrap pin requires a small capacitor; connect a 47nF bootstrap capacitor rated above 25V between the BST pin and the LX pin.

The output-sense connection to the feedback pins must be separated from any power trace. Connect the output-sense trace as close as possible to the load point to avoid additional load regulation errors. Sensing through a high-current load trace will degrade DC load regulation.

The power traces, including PGND traces, the SW or OUT traces and the VIN trace must be kept short, direct and wide to allow large current flow. The inductor connection to the SW or OUT pins must be as short as possible. Use several via pads when routing between layers.

LDOs

Input Capacitor

The input capacitors must be located as physically close as possible to the power pin (LDO2P5V_IN) and power ground (GND). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently more capable than are tantalum capacitors to withstand input current surges from low impedance sources such as batteries used in portable devices. Typically, 10V- or 16V-rated capacitors are required. The recommended external components are shown in Table 10.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO (LDO2P5V and LDO5V). The output capacitor must be placed as close to the device and power (PGND) pins as possible. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines must be observed. Please contact IDT for Gerber files that contain the recommended board layout.
- As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths.
- The 0.1µF decoupling capacitors must be mounted on the component side of the board as close to the VDD pin as possible. Do not use vias between decoupling capacitors and VDD pins. Keep PCB traces to each VDD pin and to ground vias as short as possible.
- To optimize board layout, place all components on the same side of the board and limit the use of vias. Route other signal traces away from the IDTP9036. For example, use keepouts for signal traces routing on inner and bottom layers underneath the device.
- The NQG48 6.0 mm x 6x0 mm x 75mm 48L package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.
- The package center exposed pad (EP) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EP) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of PTH vias embedded in the PCB center land pad for the NTG48. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board. There, these thermal vias embed in a copper fill having the same dimensions as the center land pad on the component side. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques must then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
    1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the top layer of the PCB.
    2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
    3. Thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.
    4. Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).
    5. Do not use solder mask or place silkscreen on the heat-dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

Power Dissipation/Thermal Requirements

The IDTP9036 is offered in a TQFN-48L package. The maximum power dissipation capability is 2W, limited by the die's specified maximum operating junction temperature, T_J, of 125°C. The junction temperature rises with the device power dissipation based on the package thermal resistance. The package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 31°C/W when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout, as well as the placement of the IDTP9036 IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics,

die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB itself upon which the TQFN is mounted. For example, in a still air environment, as is often the case, a significant amount of the heat that is generated (60 - 85%) sinks into the PCB. Changing the design or configuration of the PCB impacts the overall thermal resistivity and, thus, the board's heat sinking efficiency.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation must be calculated:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP9036 device is 150°C. The thermal resistance of the 48-pin NQG package (NGQ48) is optimally θ_{JA}=30°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is:

$$P_{D(Max)} = (150°C - 85°C) / 30°C/W \cong 2 \text{ Watt}$$

Thermal Overload Protection

The IDTP9036 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 140°C. To allow the maximum load current on each regulator and resonant transmitter, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP9036 is dissipated into the PCB. The package exposed paddle must be soldered to the PCB, with multiple vias evenly distributed under the exposed paddle and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes

NQG TQFN-48 Package Assembly

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

PACKAGE OUTLINE DRAWING

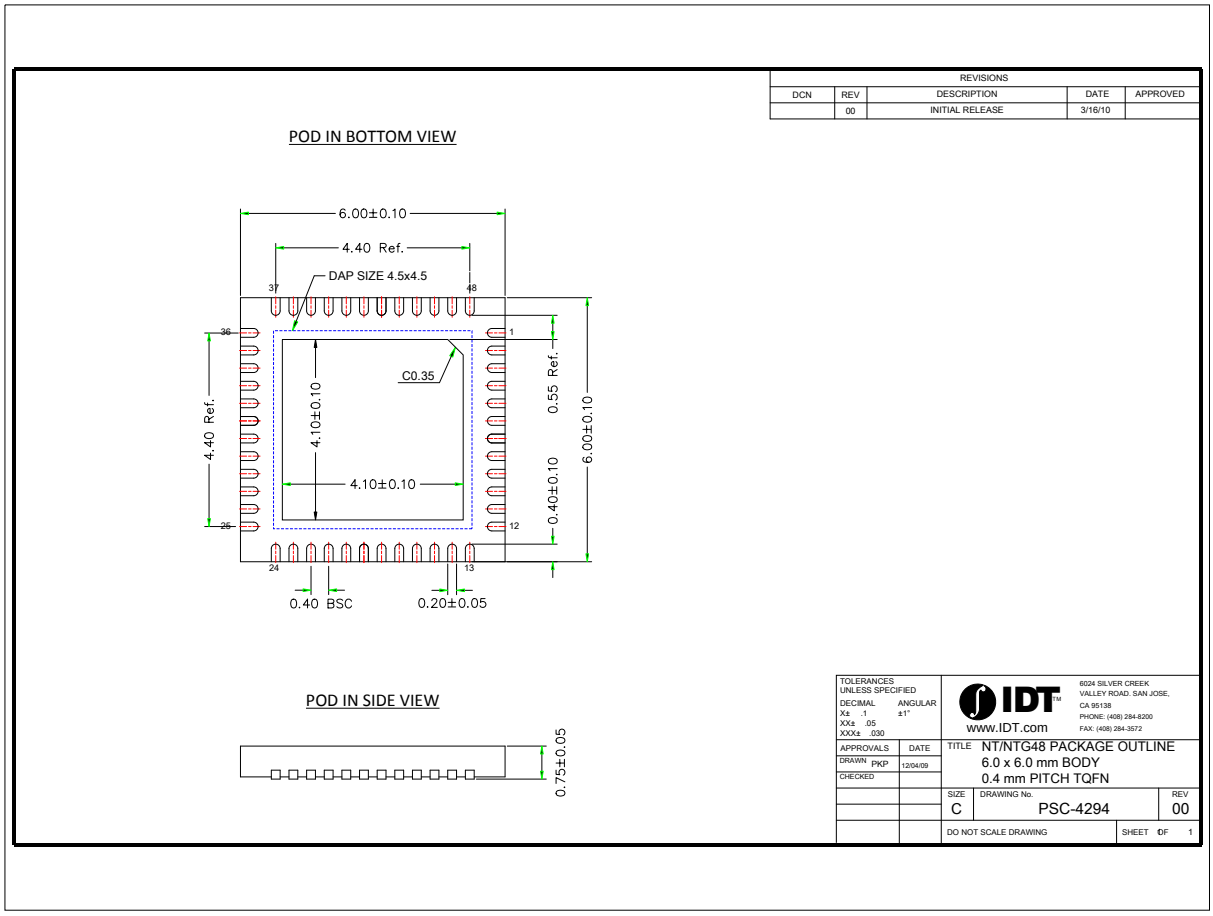


Figure 10. IDTP9036 Package Outline Drawing (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm48L, 0.4mm pitch)

ORDERING GUIDE

Table 8. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9036-0NTGI	P9036NTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tape or Canister	25
P9036-0NTGI8	P9036NTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tape and Reel	2,500

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