

## 2.5V, 3.3V ECL/LVPECL/LVDS DUAL DIFFERENTIAL 2:1 MULTIPLEXER

# MC100ES6056

The MC100ES6056 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple  $V_{BB}$  pins are provided.

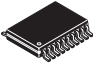
The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The device features both individual and common select inputs to address both data path and random logic applications.


The 100ES Series contains temperature compensation.

### Features


- 360 ps Typical Propagation Delays
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- ECL Mode Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -2.375 \text{ V to } -3.8 \text{ V}$
- Open Input Default State
- Separate and Common Select
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- $V_{BB}$  Outputs
- LVDS Input Compatible
- 20-Lead Pb-Free Package Available



**DT SUFFIX**  
20-LEAD TSSOP PACKAGE  
CASE 948E-03

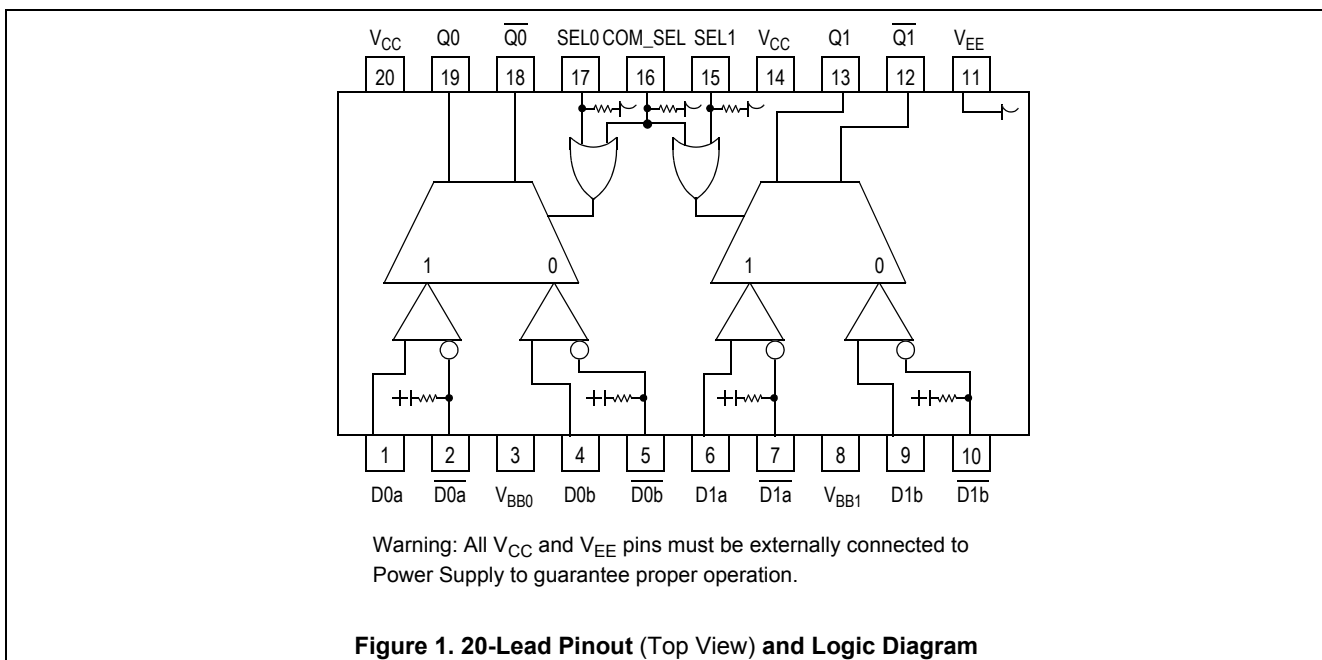


**EJ SUFFIX**  
20-LEAD TSSOP PACKAGE  
Pb-FREE PACKAGE  
CASE 948E-03



**EG SUFFIX**  
20-LEAD SOIC PACKAGE  
Pb-FREE PACKAGE  
CASE 751D-07

| ORDERING INFORMATION |                    |
|----------------------|--------------------|
| Device               | Package            |
| MC100ES6056DT        | TSSOP-20           |
| MC100ES6056DTR2      | TSSOP-20           |
| MC100ES6056EJ        | TSSOP-20 (Pb-Free) |
| MC100ES6056EJR2      | TSSOP-20 (Pb-Free) |
| MC100ES6056EG        | SOIC-20 (Pb-Free)  |
| MC100ES6056EGR2      | SOIC-20 (Pb-Free)  |



**Figure 1. 20-Lead Pinout (Top View) and Logic Diagram**

Table 1. Pin Description

| Pin                                   | Function                 |
|---------------------------------------|--------------------------|
| D0a* – D1a*                           | ECL Input Data a         |
| $\overline{D0a^*} - \overline{D1a^*}$ | ECL Input Data a Invert  |
| D0b* – D1b*                           | ECL Input Data b         |
| $\overline{D0b^*} - \overline{D1b^*}$ | ECL Input Data b Invert  |
| SEL0* – SEL1*                         | ECL Indiv. Select Input  |
| COM_SEL*                              | ECL Common Select Input  |
| V <sub>BB0</sub> , V <sub>BB1</sub>   | Output Reference Voltage |
| Q0 – Q1                               | ECL True Outputs         |
| $\overline{Q0} - \overline{Q1}$       | ECL Inverted Outputs     |
| V <sub>CC</sub>                       | Positive Supply          |
| V <sub>EE</sub>                       | Negative Supply          |

Table 2. Function Table

| SEL0 | SEL1 | COM_SEL | Q0, $\overline{Q0}$ | Q1, $\overline{Q1}$ |
|------|------|---------|---------------------|---------------------|
| X    | X    | H       | a                   | a                   |
| L    | L    | L       | b                   | b                   |
| L    | H    | L       | b                   | a                   |
| H    | H    | L       | a                   | a                   |
| H    | L    | L       | a                   | b                   |

\* Input function will default LOW when left open.

Table 3. General Specifications

| Characteristics                             |                      | Value         |
|---|----------------------|---------------|
| Internal Input Pulldown Resistor            |                      | 75 k $\Omega$ |
| Internal Input Pullup Resistor              |                      | 75 k $\Omega$ |
| ESD Protection                              | Human Body Model     | > 4 kV        |
|   | Machine Model        | > 400 V       |
|   | Charged Device Model | > 2 kV        |
| Thermal Resistance<br>(Junction-to-Ambient) | 0 LFPM, 20 TSSOP     | 140°C/W       |
|   | 500 LFPM, 20 TSSOP   | 100°C/W       |

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

**Table 4. DC Characteristics** ( $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.5\text{ V} \pm 5\%$  or  $3.8\text{ V}$  to  $-3.135\text{ V}$ ;  $V_{CC} = 2.5\text{ V} \pm 5\%$  or  $3.135\text{ V}$  to  $3.8\text{ V}$ ,  $V_{EE} = 0\text{ V}$ )

| Symbol    | Characteristics                                 | -40°C           |                 |                 | 0°C to 85°C     |                 |                 | Unit |
|-----------|---|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|
|           |   | Min             | Typ             | Max             | Min             | Typ             | Max             |      |
| $I_{EE}$  | Power Supply Current                            |                 | 30              | 60              |                 | 30              | 60              | mA   |
| $V_{OH}$  | Output HIGH Voltage <sup>(1)</sup>              | $V_{CC} - 1150$ | $V_{CC} - 1020$ | $V_{CC} - 800$  | $V_{CC} - 1200$ | $V_{CC} - 970$  | $V_{CC} - 750$  | mV   |
| $V_{OL}$  | Output LOW Voltage <sup>(1)</sup>               | $V_{CC} - 1950$ | $V_{CC} - 1620$ | $V_{CC} - 1250$ | $V_{CC} - 2000$ | $V_{CC} - 1680$ | $V_{CC} - 1300$ | mV   |
| $V_{IH}$  | Input HIGH Voltage                              | $V_{CC} - 1165$ |                 | $V_{CC} - 880$  | $V_{CC} - 1165$ |                 | $V_{CC} - 880$  | mV   |
| $V_{IL}$  | Input LOW Voltage                               | $V_{CC} - 1810$ |                 | $V_{CC} - 1475$ | $V_{CC} - 1810$ |                 | $V_{CC} - 1475$ | mV   |
| $V_{BB}$  | Output Reference Voltage                        | $V_{CC} - 1380$ | $V_{CC} - 1290$ | $V_{CC} - 1220$ | $V_{CC} - 1380$ | $V_{CC} - 1290$ | $V_{CC} - 1200$ | mV   |
| $V_{PP}$  | Differential Input Voltage <sup>(2)</sup>       | 0.15            |                 | 1.3             | 0.15            |                 | 1.3             | V    |
| $V_{CMR}$ | Differential Cross Point Voltage <sup>(3)</sup> | $V_{CC} - 2.3$  |                 | $V_{CC} - 0.8$  | $V_{CC} - 2.3$  |                 | $V_{CC} - 0.8$  | V    |
| $I_{IH}$  | Input HIGH Current                              |                 |                 | 150             |                 |                 | 150             | μA   |
| $I_{IL}$  | Input LOW Current                               | -200            |                 |                 | -200            |                 |                 | μA   |

1. Output termination voltage  $V_{TT} = 0\text{ V}$  for  $V_{CC} = 2.5\text{ V}$  operation is supported but the power consumption of the device will increase.
2.  $V_{PP}$  (DC) is the minimum differential input voltage swing required to maintain device functionality.
3.  $V_{CMR}$  (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the  $V_{CMR}$  (DC) range and the input swing lies within the  $V_{PP}$  (DC) specification.

**Table 5. Absolute Maximum Ratings<sup>(1)</sup>**

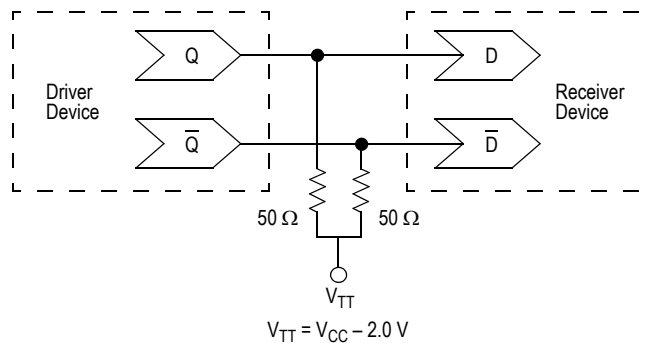
| Symbol       | Characteristic               | Conditions                             | Rating                           | Units    |
|--------------|------------------------------|--|----------------------------------|----------|
| $V_{SUPPLY}$ | Power Supply Voltage         | Difference between $V_{CC}$ & $V_{EE}$ | 3.9                              | V        |
| $V_{IN}$     | Input Voltage                | $V_{CC} - V_{EE} \leq 3.6\text{ V}$    | $V_{CC} + 0.3$<br>$V_{EE} - 0.3$ | V        |
| $I_{OUT}$    | Output Current               | Continuous<br>Surge                    | 50<br>100                        | mA<br>mA |
| $I_{BB}$     | $V_{BB}$ Sink/Source Current |  | ±0.5                             | °C       |
| $T_A$        | Operating Temperature Range  |  | -40 to +85                       | °C       |
| $T_{STG}$    | Storage Temperature Range    |  | -65 to +150                      | °C       |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

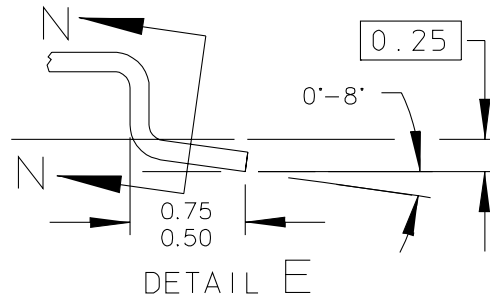
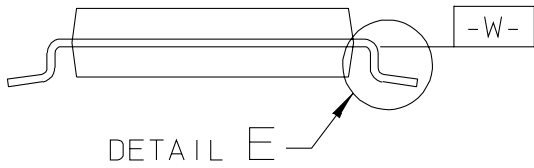
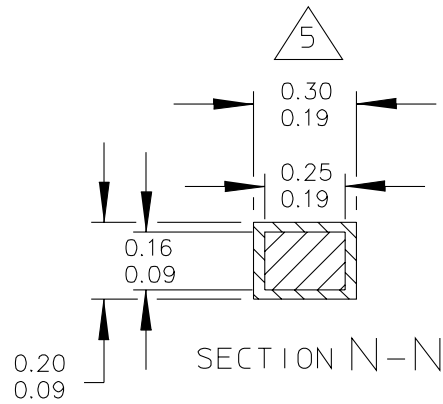
**Table 6. AC Characteristics** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -2.5\text{ V} \pm 5\%$  or  $-3.8\text{ V}$  to  $-3.135\text{ V}$ ;  $V_{CC} = 2.5\text{ V} \pm 5\%$  or  $3.135\text{ V}$  to  $3.8\text{ V}$ ;  $V_{EE} = 0\text{ V}$ )<sup>(1)</sup>

| Symbol                | Characteristics                          | -40°C to 85°C                   |     |              | Unit |    |
|-----------------------|--|---------------------------------|-----|--------------|------|----|
|                       |  | Min                             | Typ | Max          |      |    |
| $f_{\max}$            | Maximum Frequency                        |                                 | > 3 |              | GHz  |    |
| $t_{PLH}$ , $t_{PHL}$ | Propagation Delay to Output Differential | D to Q, $\bar{Q}$               | 300 | 400          | 500  | ps |
|                       |  | SEL to Q, $\bar{Q}$             | 300 | 430          | 600  | ps |
|                       |  | COM_SEL to Q, $\bar{Q}$         | 300 | 490          | 650  | ps |
| $t_{SKEW}$            | Skew                                     | Output-to-Output <sup>(2)</sup> |     | 10           | 50   | ps |
|                       |  | Part-to-Part                    |     |              | 200  | ps |
| $t_{JITTER}$          | Cycle-to-Cycle Jitter                    |                                 |     |              | 1    | ps |
| $V_{PP}$              | Minimum Input Swing                      | 200                             | 800 | 1200         |      | mV |
| $V_{CMR}$             | Differential Cross Point Voltage         | $V_{CC}-2.1$                    |     | $V_{CC}-1.1$ |      | V  |
| $t_r / t_f$           | Output Rise/Fall Time (20%–80%)          | 70                              | 120 | 230          |      | ps |

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\Omega$  to  $V_{CC}-2.0\text{ V}$ .
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

**Figure 2. Typical Termination for Output Driver and Device Evaluation**

PACKAGE DIMENSIONS



|   |                          |                            |             |
|---|--------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |             |
| TITLE:<br>20 LD TSSOP, PITCH 0.65MM                     | DOCUMENT NO: 98ASH70169A |                            | REV: B      |
|   | CASE NUMBER: 948E-03     |                            | 09 MAR 2005 |
|   | STANDARD: JEDEC          |                            |             |

**CASE 948E-03  
ISSUE B  
20-LEAD TSSOP PACKAGE**

## PACKAGE DIMENSIONS

## NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

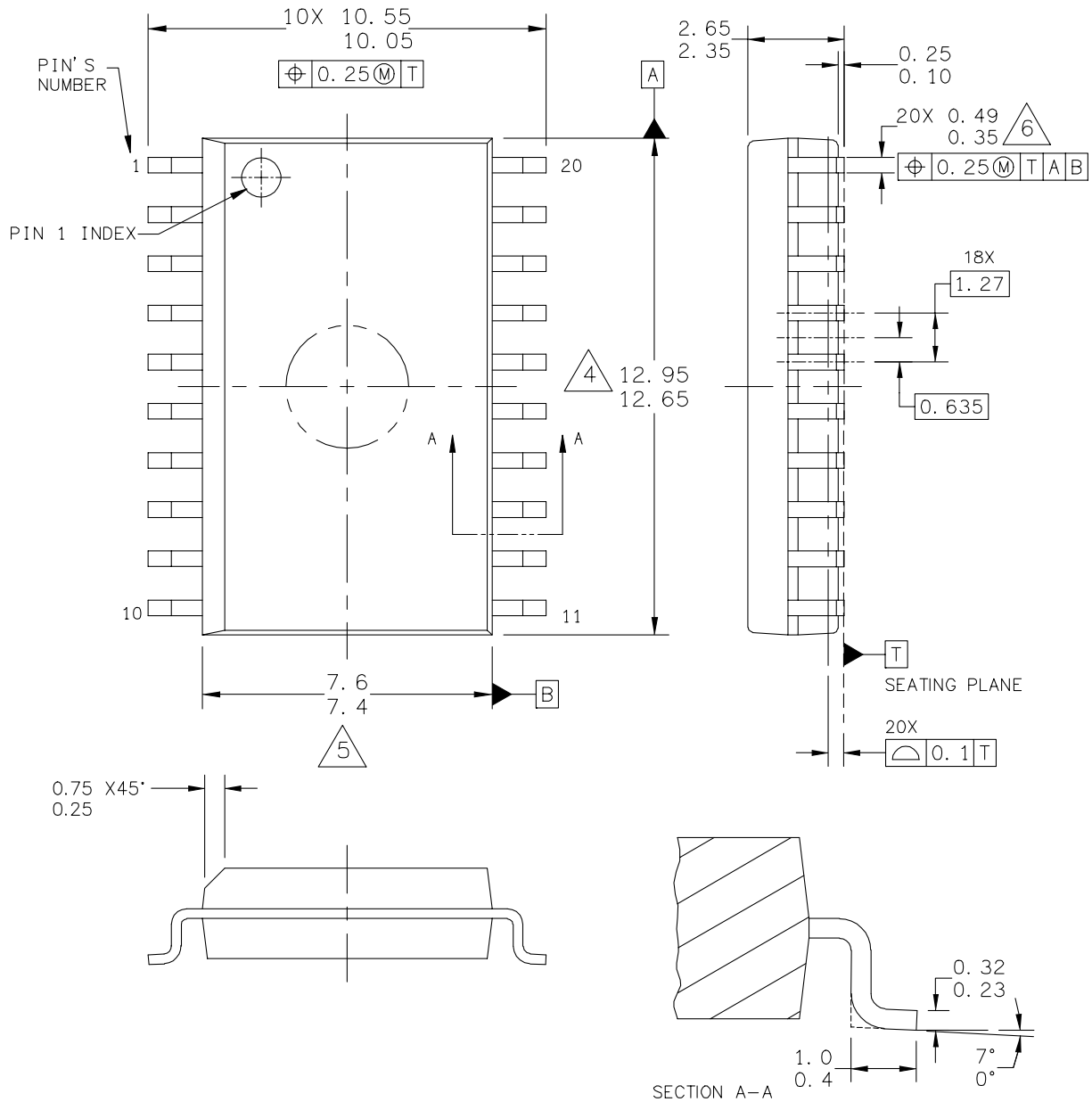
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

|   |                          |                            |  |
|---|--------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>20 LD TSSOP, PITCH 0.65MM                     | DOCUMENT NO: 98ASH70169A | REV: B                     |  |
|   | CASE NUMBER: 948E-03     | 09 MAR 2005                |  |
|   | STANDARD: JEDEC          |                            |  |

**CASE 948E-03  
ISSUE B  
20-LEAD TSSOP PACKAGE**

PACKAGE DIMENSIONS



|   |                          |                            |
|---|--------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |
| TITLE:<br>20LD SOIC W/B, 1.27 PITCH<br>CASE-OUTLINE     | DOCUMENT NO: 98ASB42343B | REV: J                     |
|   | CASE NUMBER: 751D-07     | 23 MAR 2005                |
|   | STANDARD: JEDEC MS-013AC |                            |

**CASE 751D-07  
ISSUE J  
20-LEAD SOIC PACKAGE**

## PACKAGE DIMENSIONS

## NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

|   |                          |                            |  |
|---|--------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>20LD SOIC W/B, 1.27 PITCH,<br>CASE OUTLINE    | DOCUMENT NO: 98ASB42343B | REV: J                     |  |
|   | CASE NUMBER: 751D-07     | 23 MAR 2005                |  |
|   | STANDARD: JEDEC MS-013AC |                            |  |

**CASE 751D-07  
ISSUE J  
20-LEAD SOIC PACKAGE**



MC100ES6056

3.3V, 2.5VECL/LVPECL/LVDS DUAL DIFFERENTIAL 2:1 MULTIPLEXER

Innovate with IDT and accelerate your future networks. Contact:

**www.IDT.com**

**For Sales**

800-345-7015  
408-284-8200  
Fax: 408-284-2775

**For Tech Support**

netcom@idt.com  
480-763-2056

**Corporate Headquarters**

Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road  
San Jose, CA 95138  
United States  
800 345 7015  
+408 284 8200 (outside U.S.)

**Asia**

Integrated Device Technology  
IDT (S) Pte. Ltd.  
1 Kallang Sector, #07-01/06  
Kolam Ayer Industrial Park  
Singapore 349276  
+65 67443356  
Fax: +65 67441764

**Japan**

NIPPON IDT KK  
Sanbancho Tokyu, Bld. 7F,  
8-1 Sanbancho  
Chiyoda-ku, Tokyo 102-0075  
+81 3 3221 9822  
Fax: +81 3 3221 9824

**Europe**

IDT Europe, Limited  
321 Kingston Road  
Leatherhead, Surrey  
KT22 7TU  
England  
+44 (0) 1372 363 339  
Fax: +44 (0) 1372 37885  
idteurope@idt.com



© 2008 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice. IDT and the IDT logo are trademarks of Integrated Device Technology, Inc. Accelerated Thinking is a service mark of Integrated Device Technology, Inc. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners.  
Printed in USA