Integrated Circuit Systems, Inc.

# ICS950410

**Preliminary Product Preview**

# AMD - K8™ System Clock Chip

**Recommended Application:**
AMD K8 System Clock with AMD, VIA or ALI Chipset

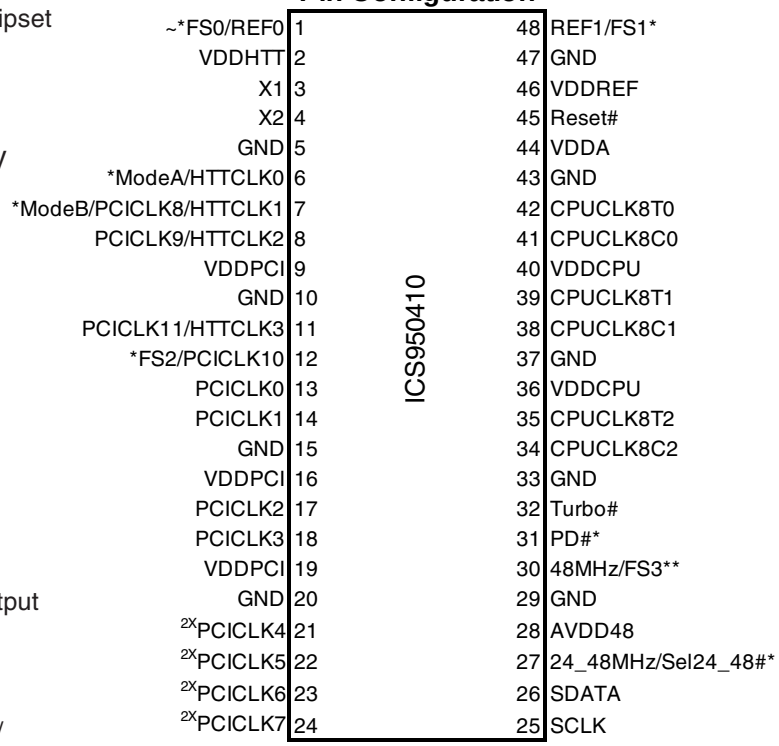
**Output Features:**

- 3 - Differential pair push-pull CPU clocks @ 3.3V
- 9 - PCICLK (Including 1 free running) @ 3.3V
- 3 - Selectable PCICLK/HTTCLK @ 3.3V
- 1 - HTTCLK @ 3.3V
- 1 - 48MHz @ 3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz.

**Features:**

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology and RESET# output to reset system
  if system malfunctions.
- Programmable watch dog safe frequency.
- Support $I^2C$ Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.
- Supports Hyper Transport Technology (HTTCLK).

## Pin Configuration




**48-SSOP**

* Internal Pull-Up Resistor

2X This Output has 2X Default Drive and can be programmaed lower via IIC

~ This Output has 1.5x drive

## Functionality

| FS3 | FS2 | FS1 | FS0 | CPU | HTT | PCI |
|---|---|---|---|---|---|---|
| | | | | MHz | MHz | MHz |
| 0 | 0 | 0 | 0 | 100.90 | 67.27 | 33.63 |
| 0 | 0 | 0 | 1 | 133.90 | 66.95 | 33.48 |
| 0 | 0 | 1 | 0 | 168.00 | 67.20 | 33.60 |
| 0 | 0 | 1 | 1 | 202.00 | 67.33 | 33.67 |
| 0 | 1 | 0 | 0 | 100.20 | 66.80 | 33.40 |
| 0 | 1 | 0 | 1 | 133.50 | 66.75 | 33.38 |
| 0 | 1 | 1 | 0 | 166.70 | 66.68 | 33.34 |
| 0 | 1 | 1 | 1 | 200.40 | 66.80 | 33.40 |
| 1 | 0 | 0 | 0 | 150.00 | 60.00 | 30.00 |
| 1 | 0 | 0 | 1 | 180.00 | 60.00 | 30.00 |
| 1 | 0 | 1 | 0 | 210.00 | 70.00 | 35.00 |
| 1 | 0 | 1 | 1 | 240.00 | 60.00 | 30.00 |
| 1 | 1 | 0 | 0 | 270.00 | 67.50 | 33.75 |
| 1 | 1 | 0 | 1 | 233.33 | 66.67 | 33.33 |
| 1 | 1 | 1 | 0 | 266.67 | 66.67 | 33.33 |
| 1 | 1 | 1 | 1 | 300.00 | 75.00 | 37.50 |

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## Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | ~*FS0/REF0 | I/O | Frequency select latch input pin / 14.318 MHz reference clock. |
| 2 | VDDHTT | PWR | Supply for HTT clocks, nominal 3.3V. |
| 3 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 4 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 5 | GND | PWR | Ground pin. |
| 6 | *ModeA/HTTCLK0 | I/O | Mode selection latch input pin / Hyper Transport output. |
| 7 | *ModeB/PCICLK8/HTTCLK1 | I/O | Mode selection latch input pin / PCI clock output / Hyper Transport output. |
| 8 | PCICLK9/HTTCLK2 | OUT | PCI clock output / Hyper Transport output. |
| 9 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 10 | GND | PWR | Ground pin. |
| 11 | PCICLK11/HTTCLK3 | OUT | PCI clock output / Hyper Transport output. |
| 12 | *FS2/PCICLK10 | I/O | Frequency select latch input pin / 3.3V PCI clock output. |
| 13 | PCICLK0 | OUT | PCI clock output. |
| 14 | PCICLK1 | OUT | PCI clock output. |
| 15 | GND | PWR | Ground pin. |
| 16 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 17 | PCICLK2 | OUT | PCI clock output. |
| 18 | PCICLK3 | OUT | PCI clock output. |
| 19 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 20 | GND | PWR | Ground pin. |
| 21 | 2XPCICLK4 | OUT | PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC. |
| 22 | 2XPCICLK5 | OUT | PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC. |
| 23 | 2XPCICLK6 | OUT | PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC. |
| 24 | 2XPCICLK7 | OUT | PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC. |
| 25 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 26 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 27 | 24_48MHz/Sel24_48#* | I/O | 24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz. |
| 28 | AVDD48 | PWR | Analog power for 48MHz outputs and fixed PLL core, nominal 3.3V |
| 29 | GND | PWR | Ground pin. |
| 30 | 48MHz/FS3** | I/O | Fixed 48MHz clock output. 3.3V / 'Frequency select latch input pin |
| 31 | PD#* | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped. |
| 32 | Turbo# | IN | Real time input pin to change frequency to a pre-programmed under or over clock entries located in IIC Rom table. |
| 33 | GND | PWR | Ground pin. |
| 34 | CPUCLK8C2 | OUT | Complimentary clock of differential 3.3V push-pull K8 pair. |
| 35 | CPUCLK8T2 | OUT | True clock of differential 3.3V push-pull K8 pair. |
| 36 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 37 | GND | PWR | Ground pin. |
| 38 | CPUCLK8C1 | OUT | Complimentary clock of differential 3.3V push-pull K8 pair. |
| 39 | CPUCLK8T1 | OUT | True clock of differential 3.3V push-pull K8 pair. |
| 40 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 41 | CPUCLK8C0 | OUT | Complimentary clock of differential 3.3V push-pull K8 pair. |
| 42 | CPUCLK8T0 | OUT | True clock of differential 3.3V push-pull K8 pair. |
| 43 | GND | PWR | Ground pin. |
| 44 | VDDA | PWR | 3.3V power for the PLL core. |
| 45 | Reset# | OUT | Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low. |
| 46 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 47 | GND | PWR | Ground pin. |
| 48 | REF1/FS1* | I/O | 14.318 MHz reference clock / Frequency select latch input pin. |

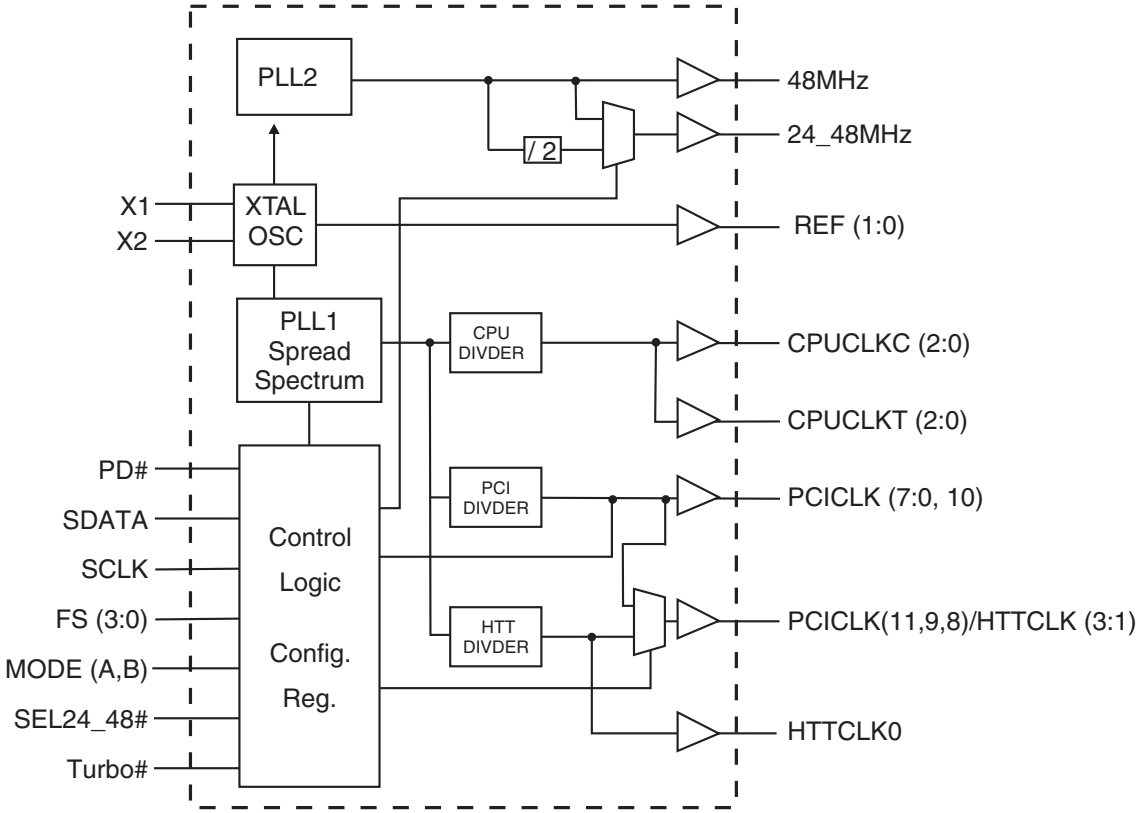
* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ 1.5X Drive Strength

## General Description

The **ICS950410** is a main system clock solution for desktop designs using the AMD K8 CPU. It provides all necessary clock signals for Clawhammer and Sledgehammer with AMD, VIA or ALI systems.

The **ICS950410** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable $I^2C$ interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

## Block Diagram




## Power Groups

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 2 | 5 | Xtal, POR |
| 9 | 10 | PCICLK, HTTCLK O/p |
| 16,19 | 15,20 | PCICLK Outputs |
| 29 | 27,30,33 | 48 MHz, Fix Analog |
| 35,38 | 34,39 | CPU Outputs |
| 43 | 42 | Analog, CPU PLL, MCLK |
| 46 | 47 | REF, Digital Core |

**Table1: Frequency Selection Table**

| Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | CPU | HTT | PCI |
|---|---|---|---|---|---|---|---|
| FS4 | FS3 | FS2 | FS1 | FS0 | MHz | MHz | MHz |
| 0 | 0 | 0 | 0 | 0 | 100.90 | 67.27 | 33.63 |
| 0 | 0 | 0 | 0 | 1 | 133.90 | 66.95 | 33.48 |
| 0 | 0 | 0 | 1 | 0 | 168.00 | 67.20 | 33.60 |
| 0 | 0 | 0 | 1 | 1 | 202.00 | 67.33 | 33.67 |
| 0 | 0 | 1 | 0 | 0 | 100.20 | 66.80 | 33.40 |
| 0 | 0 | 1 | 0 | 1 | 133.50 | 66.75 | 33.38 |
| 0 | 0 | 1 | 1 | 0 | 166.70 | 66.68 | 33.34 |
| 0 | 0 | 1 | 1 | 1 | 200.40 | 66.80 | 33.40 |
| 0 | 1 | 0 | 0 | 0 | 150.00 | 60.00 | 30.00 |
| 0 | 1 | 0 | 0 | 1 | 180.00 | 60.00 | 30.00 |
| 0 | 1 | 0 | 1 | 0 | 210.00 | 70.00 | 35.00 |
| 0 | 1 | 0 | 1 | 1 | 240.00 | 60.00 | 30.00 |
| 0 | 1 | 1 | 0 | 0 | 270.00 | 67.50 | 33.75 |
| 0 | 1 | 1 | 0 | 1 | 233.33 | 66.67 | 33.33 |
| 0 | 1 | 1 | 1 | 0 | 266.67 | 66.67 | 33.33 |
| 0 | 1 | 1 | 1 | 1 | 300.00 | 75.00 | 37.50 |
| 1 | 0 | 0 | 0 | 0 | 100.00 | 66.67 | 33.33 |
| 1 | 0 | 0 | 0 | 1 | 133.33 | 66.67 | 33.33 |
| 1 | 0 | 0 | 1 | 0 | 166.66 | 66.66 | 33.33 |
| 1 | 0 | 0 | 1 | 1 | 200.00 | 66.67 | 33.33 |
| 1 | 0 | 1 | 0 | 0 | 103.00 | 68.67 | 34.33 |
| 1 | 0 | 1 | 0 | 1 | 137.33 | 68.66 | 34.33 |
| 1 | 0 | 1 | 1 | 0 | 171.66 | 68.66 | 34.33 |
| 1 | 0 | 1 | 1 | 1 | 206.00 | 68.67 | 34.33 |
| 1 | 1 | 0 | 0 | 0 | 154.49 | 61.79 | 30.90 |
| 1 | 1 | 0 | 0 | 1 | 185.38 | 61.79 | 30.90 |
| 1 | 1 | 0 | 1 | 0 | 216.31 | 72.10 | 36.05 |
| 1 | 1 | 0 | 1 | 1 | 247.20 | 61.80 | 30.90 |
| 1 | 1 | 1 | 0 | 0 | 278.10 | 69.53 | 34.76 |
| 1 | 1 | 1 | 0 | 1 | 240.34 | 68.67 | 34.33 |
| 1 | 1 | 1 | 1 | 0 | 274.68 | 68.67 | 34.34 |
| 1 | 1 | 1 | 1 | 1 | 308.97 | 77.24 | 38.62 |

## Mode Functionality Tables

| ModeA | ModeB | Pin7 | Pin8 | Pin11 |
|---|---|---|---|---|
| 0 | 0 | HTTCLK1 | HTTCLK2 | PCICLK11 |
| 0 | 1 | HTTCLK1 | HTTCLK2 | HTTCLK3 |
| 1 | 0 | PCICLK8 | PCICLK9 | PCICLK11 |
| 1 | 1 | HTTCLK1 | PCICLK9 | PCICLK11 |

# General $I^2C$ serial interface information

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | | ICS (Slave/Receiver) |
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| | O | | |
| | O | | O |
| | O | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | | ICS (Slave/Receiver) |
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address D3(H) | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count = X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| | O | | O |
| | O | | O |
| | O | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

### I²C Table: Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SS_EN | Spread Enable | RW | OFF | ON | 1 |
| Bit 6 | - | SEL24_48MHz | Output Select | RW | 48MHz | 24MHz | Latch |
| Bit 5 | - | FS Source Select | FS Source Select | RW | latch | I2C | 0 |
| Bit 4 | - | FS4 | Freq Select Bit 4 | RW | See Table1: Frequency Selection Table | | 0 |
| Bit 3 | - | FS3 | Freq Select Bit 3 | RW | | | Latch |
| Bit 2 | - | FS2 | Freq Select Bit 2 | RW | | | Latch |
| Bit 1 | - | FS1 | Freq Select Bit 1 | RW | | | Latch |
| Bit 0 | - | FS0 | Freq Select Bit 0 | RW | | | Latch |

### I²C Table: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 1 | CPUCLK8T/C2 | Output Control | RW | Disable | Enable | 1 |
| Bit 6 | 6 | HTTCLK0 | Output Control | RW | Disable | Enable | 1 |
| Bit 5 | 7 | PCICLK8/HTTCLK1 | Output Control | RW | Disable | Enable | 1 |
| Bit 4 | 8 | PCICLK9/HTTCLK2 | Output Control | RW | Disable | Enable | 1 |
| Bit 3 | 11 | PCICLK11/HTTCLK3 | Output Control | RW | Disable | Enable | 1 |
| Bit 2 | 12 | PCICLK10 | Output Control | RW | Disable | Enable | 1 |
| Bit 1 | 13 | PCICLK0 | Output Control | RW | Disable | Enable | 1 |
| Bit 0 | 14 | PCICLK1 | Output Control | RW | Disable | Enable | 1 |

### I²C Table: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 17 | PCICLK2 | Output Control | RW | Disable | Enable | 1 |
| Bit 6 | 18 | PCICLK3 | Output Control | RW | Disable | Enable | 1 |
| Bit 5 | 21 | PCICLK4 | Output Control | RW | Disable | Enable | 1 |
| Bit 4 | 22 | PCICLK5 | Output Control | RW | Disable | Enable | 1 |
| Bit 3 | 23 | PCICLK6 | Output Control | RW | Disable | Enable | 1 |
| Bit 2 | 24 | PCICLK7 | Output Control | RW | Disable | Enable | 1 |
| Bit 1 | 28 | 24_48MHz | Output Control | RW | Disable | Enable | 1 |
| Bit 0 | 31 | 48MHz | Output Control | RW | Disable | Enable | 1 |

### I²C Table: Output Control Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 37,36 | CPUCLK8T/C_1 | Output Control | RW | Disable | Enable | 1 |
| Bit 6 | 41,40 | CPUCLK8T/C_0 | Output Control | RW | Disable | Enable | 1 |
| Bit 5 | | Reserved | Reserved | RW | - | - | 1 |
| Bit 4 | 45,48 | REF0/REF1 | Output Control | RW | Disable | Enable | 1 |
| Bit 3 | - | PCI_Str1 | PCI9,8 Strength Control only | RW | 00: 0.5X Drive | 10: 1.5X Drive | 0 |
| Bit 2 | - | PCI_Str0 | | RW | 01: 1.0X Drive | 11: 2.0X Drive | 1 |
| Bit 1 | - | PCI_Str1 | PCI11 Strength Control only | RW | 00: 0.5X Drive | 10: 1.5X Drive | 0 |
| Bit 0 | - | PCI_Str0 | | RW | 01: 1.0X Drive | 11: 2.0X Drive | 1 |

### I²C Table: Output Control Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | PCIStr1 | All other PCICLK Strength Control | RW | 00: 0.5X Drive | 10: 1.5X Drive | 0 |
| Bit 6 | - | PCIStr0 | | RW | 01: 1.0X Drive | 11: 2.0X Drive | 1 |
| Bit 5 | - | PCIStr1 | PCICLK (7:6) Strength Control | RW | 00: 0.5X Drive | 10: 1.5X Drive | 1 |
| Bit 4 | - | PCIStr0 | | RW | 01: 1.0X Drive | 11: 2.0X Drive | 1 |
| Bit 3 | - | PCIStr1 | PCICLK (5) Strength Control | RW | 00: 0.5X Drive | 10: 1.5X Drive | 1 |
| Bit 2 | - | PCIStr0 | | RW | 01: 1.0X Drive | 11: 2.0X Drive | 1 |
| Bit 1 | - | PCIStr1 | PCICLK (4) Strength Control | RW | 00: 0.5X Drive | 10: 1.5X Drive | 1 |
| Bit 0 | - | PCIStr0 | | RW | 01: 1.0X Drive | 11: 2.0X Drive | 1 |

### I²C Table: Reserved Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 6 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 5 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 2 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 1 | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | Reserved | X |

### I²C Table: Byte Count Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes. | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 0 |
| Bit 2 | - | BC2 | | RW | | | 1 |
| Bit 1 | - | BC1 | | RW | | | 1 |
| Bit 0 | - | BC0 | | RW | | | 0 |

### I²C Table: Byte Count and Vendor ID Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | REV_ID3 | Revision ID | RW | - | - | 0 |
| Bit 6 | - | REV_ID2 | | RW | - | - | 0 |
| Bit 5 | - | REV_ID1 | | RW | - | - | 0 |
| Bit 4 | - | REV_ID0 | | RW | - | - | 0 |
| Bit 3 | - | Vendor_ID3 | Vendor ID | RW | - | - | 0 |
| Bit 2 | - | Vendor_ID2 | | RW | - | - | 0 |
| Bit 1 | - | Vendor_ID1 | | RW | - | - | 0 |
| Bit 0 | - | Vendor_ID0 | | RW | - | - | 1 |

### I²C Table: Skew Control Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | | 1 | | PWD |
|---|---|---|---|---|---|---|---|---|---|
| Bit 7 | - | PCI/HTTSkw3 | CPU-PCI/HTT 7 Step Skew Control (ps) | RW | 0000:0 | 0100:150 | 1000:300 | 1100:450 | 1 |
| Bit 6 | - | PCI/HTTSkw2 | | RW | 0001:N/A | 0101:N/A | 1001:N/A | 1101:600 | 1 |
| Bit 5 | - | PCI/HTTSkw1 | | RW | 0010:N/A | 0110:N/A | 1010:N/A | 1110:750 | 0 |
| Bit 4 | - | PCI/HTTSkw0 | | RW | 0011:N/A | 0111:N/A | 1011:N/A | 1111:900 | 0 |
| Bit 3 | - | PCISkw3 | CPU-PCI 7 Step Skew Control (ps) | RW | 0000:0 | 0100:150 | 1000:300 | 1100:450 | 1 |
| Bit 2 | - | PCISkw2 | | RW | 0001:N/A | 0101:N/A | 1001:N/A | 1101:600 | 1 |
| Bit 1 | - | PCISkw1 | | RW | 0010:N/A | 0110:N/A | 1010:N/A | 1110:750 | 0 |
| Bit 0 | - | PCISkw0 | | RW | 0011:N/A | 0111:N/A | 1011:N/A | 1111:900 | 0 |

### I²C Table: WD Time Control & Async Frequency Selection Register

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | ASEL | Async Frequency Select | RW | 66MHz | 75.4MHz | 0 |
| Bit 6 | - | AEN | AGP/PCI/ Freq Source Select | RW | FIX PLL | CPU PLL | 1 |
| Bit 5 | - | REF1 Strength | REF1 strength control | RW | 1x | 2x | 1 |
| Bit 4 | - | Reserved | Reserved | RW | - | - | 1 |
| Bit 3 | - | WDTCtrl | Watch Dog Time base Control | RW | 290ms Base | 1160ms Base | 0 |
| Bit 2 | - | WD2 | WD Timer Bit 2 | RW | These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s. | | 1 |
| Bit 1 | - | WD1 | WD Timer Bit 1 | RW | | | 1 |
| Bit 0 | - | WD0 | WD Timer Bit 0 | RW | | | 1 |

### I²C Table: VCO Control Select Bit & WD Timer Control Register

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | M/NEN | M/N Programming Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | WDEN | Watchdog Enable | RW | Disable | Enable | 0 |
| Bit 5 | - | WDStatus | WD Alarm Status | R | Normal | Alarm | 0 |
| Bit 4 | - | WD SF4 | Watch Dog Safe Freq Programming bits | RW | Writing to these bit will configure the safe frequency as Byte0 bit (4:0). | | 0 |
| Bit 3 | - | WD SF3 | | RW | | | 0 |
| Bit 2 | - | WD SF2 | | RW | | | 0 |
| Bit 1 | - | WD SF1 | | RW | | | 0 |
| Bit 0 | - | WD SF0 | | RW | | | 0 |

### I²C Table: VCO Frequency Control Register

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of N Divider in Byte 11 and 12 | | X |
| Bit 6 | - | N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | M Div5 | M Divider Programming bits (5:0) | RW | The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 4 | - | M Div4 | | RW | | | X |
| Bit 3 | - | M Div3 | | RW | | | X |
| Bit 2 | - | M Div2 | | RW | | | X |
| Bit 1 | - | M Div1 | | RW | | | X |
| Bit 0 | - | M Div0 | | RW | | | X |

### I²C Table: VCO Frequency Control Register

| Byte 12 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|---|
| Bit 7 | - | | N Div7 | N Divider Programming bit (7:0) | RW | The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | | N Div6 | | RW | | | X |
| Bit 5 | - | | N Div5 | | RW | | | X |
| Bit 4 | - | | N Div4 | | RW | | | X |
| Bit 3 | - | | N Div3 | | RW | | | X |
| Bit 2 | - | | N Div2 | | RW | | | X |
| Bit 1 | - | | N Div1 | | RW | | | X |
| Bit 0 | - | | N Div0 | | RW | | | X |

### I²C Table: Spread Spectrum Control Register

| Byte 13 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|---|
| Bit 7 | - | | SSP7 | Spread Spectrum Programming b(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming. | | X |
| Bit 6 | - | | SSP6 | | RW | | | X |
| Bit 5 | - | | SSP5 | | RW | | | X |
| Bit 4 | - | | SSP4 | | RW | | | X |
| Bit 3 | - | | SSP3 | | RW | | | X |
| Bit 2 | - | | SSP2 | | RW | | | X |
| Bit 1 | - | | SSP1 | | RW | | | X |
| Bit 0 | - | | SSP0 | | RW | | | X |

### I²C Table: Spread Spectrum Control Register

| Byte 14 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|---|
| Bit 7 | - | | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | | SSP14 | Spread Spectrum Programming b(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming. | | X |
| Bit 5 | - | | SSP13 | | RW | | | X |
| Bit 4 | - | | SSP12 | | RW | | | X |
| Bit 3 | - | | SSP11 | | RW | | | X |
| Bit 2 | - | | SSP10 | | RW | | | X |
| Bit 1 | - | | SSP9 | | RW | | | X |
| Bit 0 | - | | SSP8 | | RW | | | X |

## Absolute Maximum Rating

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| 3.3V Core Supply Voltage | VDD_A | - | | | $V_{DD}$ + 0.5V | V | 1 |
| 3.3V Logic Input Supply Voltage | VDD_In | - | GND - 0.5 | | $V_{DD}$ + 0.5V | V | 1 |
| Storage Temperature | Ts | - | -65 | | 150 | ˚C | 1 |
| Ambient Operating Temp | Tambient | - | 0 | | 70 | °C | 1 |
| Case Temperature | Tcase | - | | | 115 | °C | 1 |
| Input ESD protection HBM | ESD prot | - | 2000 | | | V | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{IL}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.8 | V | 1 |
| Input High Current | $I_{IH}$ | $V_{IN} = V_{DD}$ | -5 | | 5 | uA | 1 |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Low Threshold Input-High Voltage | $V_{IH\_FS}$ | 3.3 V +/-5% | 0.7 | | $V_{DD}$ + 0.3 | V | 1 |
| Low Threshold Input-Low Voltage | $V_{IL\_FS}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.35 | V | 1 |
| Operating Supply Current | $I_{DD3.3OP}$ | Full Active, $C_L$ = Full load; | | | 350 | mA | 1 |
| Operating Current | $I_{DD3.3OP}$ | all outputs driven | | | 400 | mA | 1 |
| Powerdown Current | $I_{DD3.3PD}$ | all diff pairs driven | | | 70 | mA | 1 |
| | | all differential pairs tri-stated | | | 12 | mA | 1 |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | | 14.31818 | | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance | $C_{IN}$ | Logic Inputs | | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| | $C_{INX}$ | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up or de-assertion of PD# to 1st clock | | | 1.8 | ms | 1 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_PD# | | CPU output enable after PD# de-assertion | | | 300 | us | 1 |
| Tfall_Pd# | | PD# fall time of | | | 5 | ns | 1 |
| Trise_Pd# | | PD# rise time of | | | 5 | ns | 1 |
| SMBus Voltage | $V_{DD}$ | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| Current sinking at $V_{OL}$ = 0.4 V | $I_{PULLUP}$ | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

## Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Output Impedance | $R_{DSP}$ | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -33 | | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | 1 |
| Edge Rate | $t_{slewr/f}$ | Rising/Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Group Skew | $t_{skew}$ | $V_T$ = 1.5 V | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[3] Spread Spectrum is off



## Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ppm | 1,2 |
| Clock period | $T_{period}$ | 48.00MHz output nominal | 20.8313 | | 20.8354 | ns | 2 |
| Output Impedance | $R_{DSP}$ | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -33 | | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | 1 |
| Edge Rate | $t_{slewr/f}$ | Rising/Falling edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | $t_{slewr/f\_USB}$ | USB48 Rising/Falling edge rate | 1 | | 2 | V/ns | 1 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns | 1 |
| Rise Time | $t_{r\_USB}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | | 2 | ns | 1 |
| Fall Time | $t_{f\_USB}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Group Skew | $t_{skew}$ | $V_T$ = 1.5 V | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - CPUCLKK8T/C K8 3.3V Push Pull Differential Pair

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Rising Edge Rate | $\delta V/\delta t$ | At CPU's test load. 0 V +/- 400 mV (diffential measurment) | 2 | | 10 | V/ns | 1 |
| Falling Edge Rate | $\delta V/\delta t$ | | 2 | | 10 | V/ns | 1 |
| Differential Voltage | $V_{DIFF}$ | At CPU's test load. (single-ended measurement) | 0.4 | | 2.3 | V | 1 |
| Change in $V_{DIFF\_DC}$ Magnitude | $\Delta V_{DIFF}$ | | -150 | | 150 | mV | 1 |
| Common Mode Voltage | $V_{CM}$ | | 1.05 | | 1.45 | V | 1 |
| Change in Common Mode Voltage | $\Delta V_{CM}$ | | -200 | | 200 | mV | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | Measurement from differential wavefrom | 0 | | 200 | ps | 1 |
| Jitter, Accumulated | $t_{ja}$ | | -1000 | | 1000 | | 1,2,3 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Output Impedance | $R_{ON}$ | Average value during switching transition. Used for determining series termination value. | 15 | | 55 | Ω | 1 |
| Group Skew | $t_{skew}$ | Measurement from differential wavefrom | | | 250 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All accumulated jitter specifications are guaranteed assuming that REF is at 14.31818MHz

[3] Spread Spectrum is off



## Electrical Characteristics - HTTCLK

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Output Impedance | $Z_O$ | $V_O = V_X$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | $V_{OH1}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL1}$ | $I_{OL}$ = 1 mA | | | 0.4 | V | 1 |
| Output High Current | $I_{OH1}$ | $V_{OH}$ = 2.0 V | | | -15 | mA | 1 |
| Output Low Current | $I_{OL1}$ | $V_{OL}$ = 0.8 V | 10 | | | mA | 1 |
| Edge Rate | $t_{slewr/f}$ | Rise/Fall edge rate between 20% 60% | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 50% | 45 | | 55 | % | 1 |
| Group Skew | $t_{skew}$ | $V_T$ = 1.5 V | | | 150 | ps | 1 |
| Jitter, Cycle-to-cycle | $t_{jcyc-cyc2B}$ | $V_T$ = 1.5 V | | | 250 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Clock period | $T_{period}$ | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V, $V_{OH}$@MAX = 3.135 V | -29 | | -23 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @MIN = 1.95 V, $V_{OL}$ @MAX = 0.4 V | 29 | | 27 | mA | 1 |
| Edge Rate | $t_{slewr/f}$ | Rising/Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | | 2 | ns | 1 |
| Skew | $t_{sk1}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Jitter | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 1000 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS950410 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

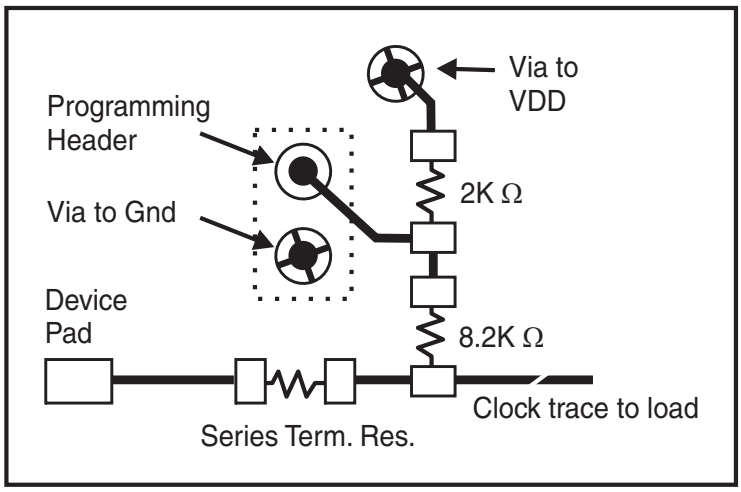
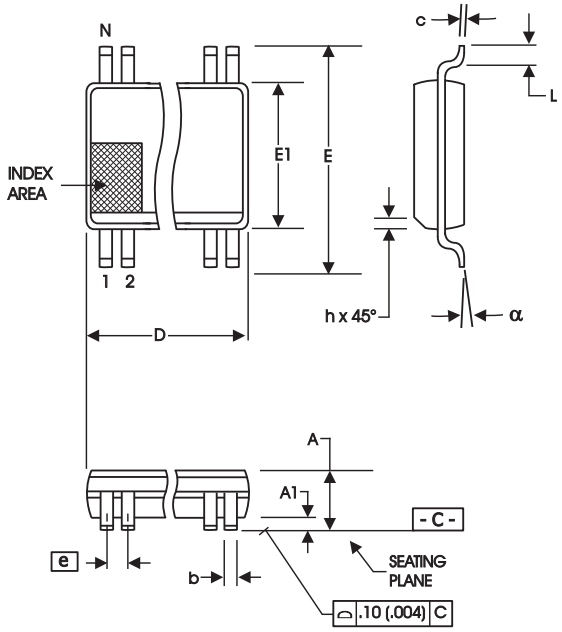



**Fig. 1**




**300 mil SSOP Package**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**ICS950410yFLF-T**

Example:

**ICS XXXX y F LF- T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0888A—04/22/05

## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| A | 4/22/2005 | 1. Updated Byte 11/12 M/N programming description<br>2. Updated Ordering Information from "Lead Free" to Annealed Lead Free".<br>3. Preliminary Release. | 8-9,15 |
| | | | |

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