

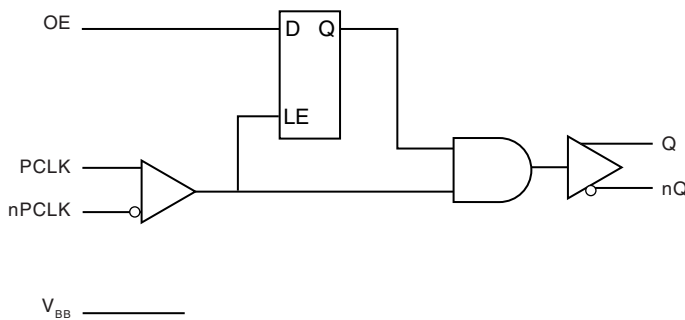
### GENERAL DESCRIPTION

The ICS853001 is a 1:1 Differential LVPECL-to-LVPECL Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS853001 may be used to regenerate LVPECL clocks which may have been attenuated, across a long trace, or may also be used as a differential-to-LVPECL translator. The differential input can accept the following differential input types: LVPECL, LVDS and CML. The device also has an output enable pin for debug/test purposes. When the output is disabled, it drives differential LOW (Q = LOW, nQ = HIGH). The ICS853001 is packaged in either a 3mm x 3mm 8-pin TSSOP or 3.9mm x 4.9mm 8-pin SOIC, making it ideal for use on space-constrained boards.

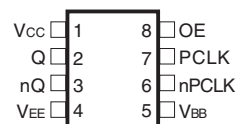
### FEATURES

- 1:1 Differential LVPECL-to-LVPECL / ECL buffer
- One LVPECL clock output pair
- One Differential LVPECL PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: >2.5GHz
- Part-to-part skew: 100ps (maximum)
- Propagation delay: 500ps (maximum)
- Additive phase jitter, RMS: 0.03ps (typical)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to  $5.25V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -5.25V$  to  $-2.375V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**ICS853001**  
**8-Lead TSSOP, 118 mil**  
 3mm x 3mm x 0.95mm package body  
**G Package**  
 Top View

**ICS853001**  
**8-Lead SOIC**  
 3.90mm x 4.90mm x 1.37mm package body  
**M Package**  
 Top View



# ICS853001

1:1, DIFFERENTIAL LVPECL-TO-  
2.5V, 3.3V, 5V LVPECL/ECL BUFFER

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	$V_{CC}$	Power		Positive supply pin.
2, 3	Q, nQ	Output		Differential output pair. LVPECL interface levels.
4	$V_{EE}$	Power		Negative supply pin.
5	$V_{BB}$	Output		Nominal bias voltage at $V_{CC} - 1.38V$ .
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating. Can accept LVPECL, LVDS, CML interface levels.
7	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input. Can accept LVPECL, LVDS, CML interface levels.
8	OE	Input	Pullup	Active HIGH output enable. When logic HIGH, the output is enabled and follows the input clock. When logic LOW, the output drives logic low (Q=LOW, nQ=HIGH). LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			37.5		$K\Omega$
$R_{PULLUP}$	Input Pullup Resistor			37.5		$K\Omega$

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	6V (LVPECL mode, $V_{EE} = 0$ )
Negative Supply Voltage, $V_{EE}$	-6V (ECL mode, $V_{CC} = 0$ )
Inputs, $V_I$ (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, $V_I$ (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
$V_{BB}$ Sink/Source, $I_{BB}$	$\pm 0.5mA$
Operating Temperature Range, $T_A$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$	
8 Lead TSSOP	101.7°C/W (0 m/s)
8 Lead SOIC	112.7°C/W (0 lfpm)
(Junction-to-Ambient)	

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $5.25V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	3.3	5.25	V
$I_{EE}$	Power Supply Current				27	mA

**TABLE 3B. LVCMOS DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $5.25V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	OE	$0.7V_{CC}$		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	OE	-0.3		$0.3V_{CC}$	V
$I_{IH}$	Input High Current	OE $V_{CC} = V_{IN}$			150	$\mu A$
$I_{IL}$	Input Low Current	OE $V_{CC} = V_{IN}$	-150			$\mu A$

**TABLE 3C. LVCMOS DC CHARACTERISTICS,  $V_{CC} = 0V$ ;  $V_{EE} = -5.25V$  TO  $-2.375V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	OE	$0.3V_{EE}$		0.3	V
$V_{IL}$	Input Low Voltage	OE	$V_{EE} - 0.3$		$0.7V_{EE}$	V
$I_{IH}$	Input High Current	OE $V_{CC} = V_{IN}$			150	$\mu A$
$I_{IL}$	Input Low Current	OE $V_{CC} = V_{IN}$	-150			$\mu A$



# ICS853001

## 1:1, DIFFERENTIAL LVPECL-TO-2.5V, 3.3V, 5V LVPECL/ECL BUFFER

**TABLE 3D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $5.25V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK	$V_{CC} = V_{IN}$		200	$\mu A$
		nPCLK	$V_{CC} = V_{IN}$		200	$\mu A$
$I_{IL}$	Input Low Current	PCLK	$V_{CC} = 5.25, V_{IN} = 0V$	-200		$\mu A$
		nPCLK	$V_{CC} = 5.25V, V_{IN} = 0V$	-200		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.2	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		1.2		$V_{CC}$	V
$V_{OH}$	Output High Voltage; NOTE 3			$V_{CC} - 1.005$		V
$V_{OL}$	Output Low Voltage; NOTE 3			$V_{CC} - 1.78$		V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V
$V_{BB}$	Bias Voltage		$V_{CC} - 1.44$	$V_{CC} - 1.38$	$V_{CC} - 1.32$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{CC} + 0.3V$ .

NOTE 3: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 4. AC CHARACTERISTICS,  $V_{CC} = 0V$ ;  $V_{EE} = -5.25V$  TO  $-2.375V$  OR  $V_{CC} = 2.375$  TO  $5.25V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				>2.5	GHz
$t_{PD}$	Propagation Delay; NOTE 1		250		500	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				100	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12KHz - 20MHz		0.03		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	$f \leq 1GHz$ $V_{CC} = 2.375V$ to $3.6V, V_{EE} = 0$	48		52	%
		$V_{CC} > 3.6V$ to $5.25V, V_{EE} = 0$ or $V_{EE} = -5.25V$ to $-3.6V, V_{CC} = 0$	46		54	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters are measured at  $f \leq 1.7GHz$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

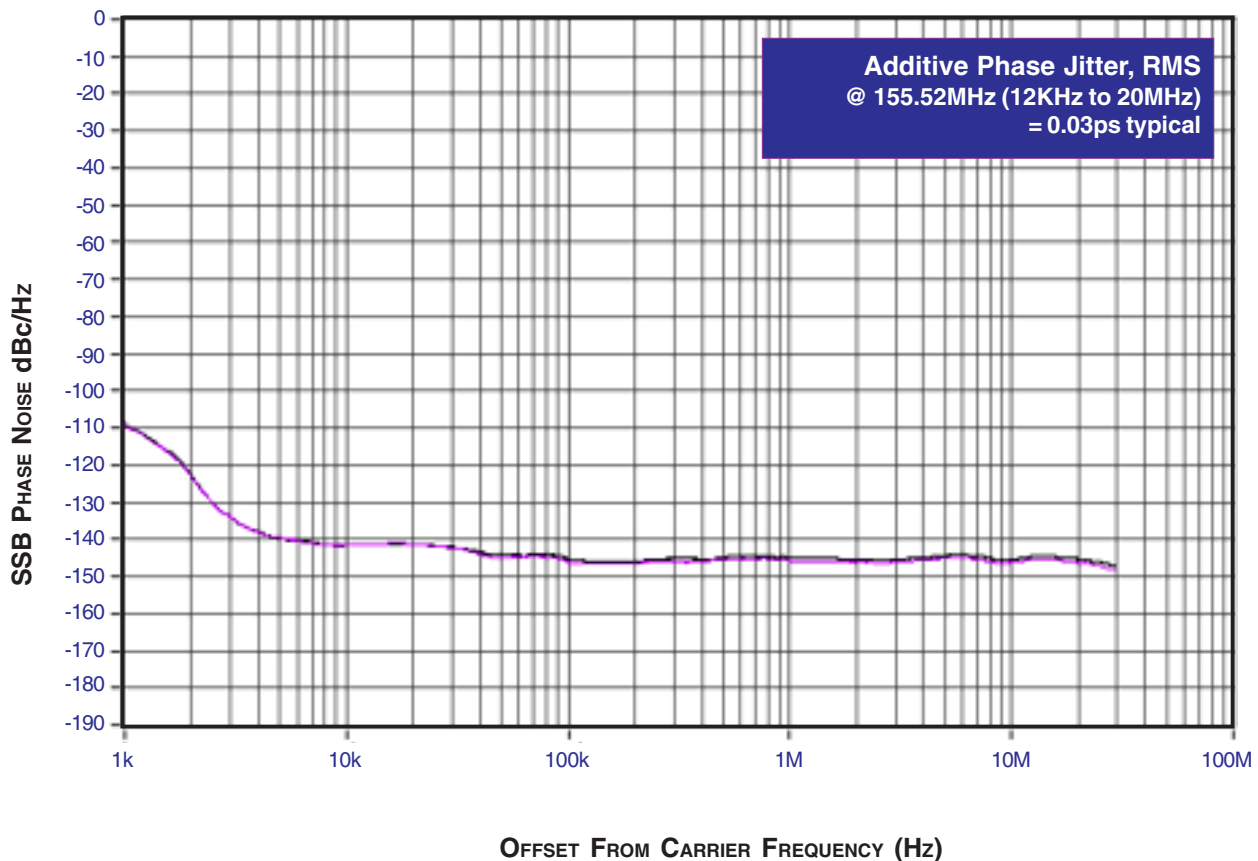
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in

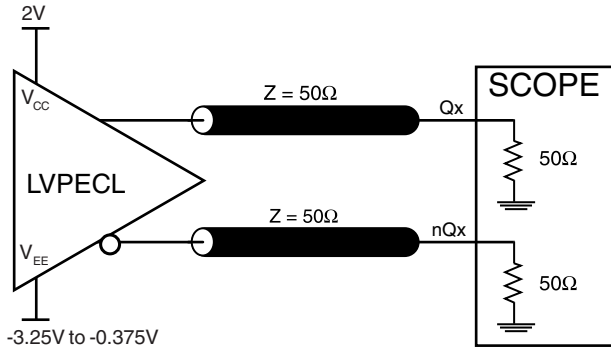
the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



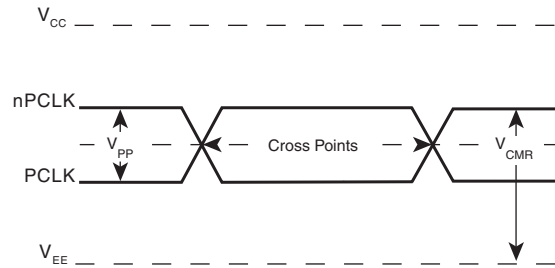
As with most timing specifications, phase noise measurements has issues. The primary issue relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated

above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

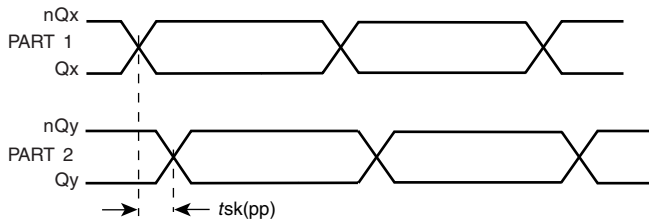
## PARAMETER MEASUREMENT INFORMATION



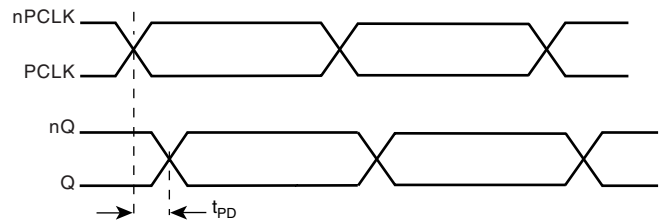
OUTPUT LOAD AC TEST CIRCUIT



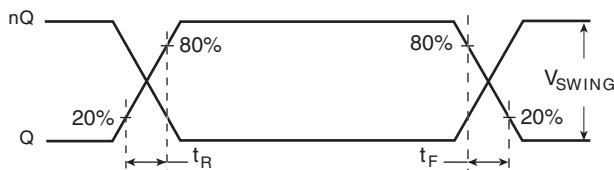
DIFFERENTIAL INPUT LEVEL



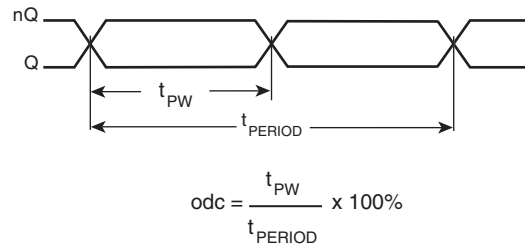
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



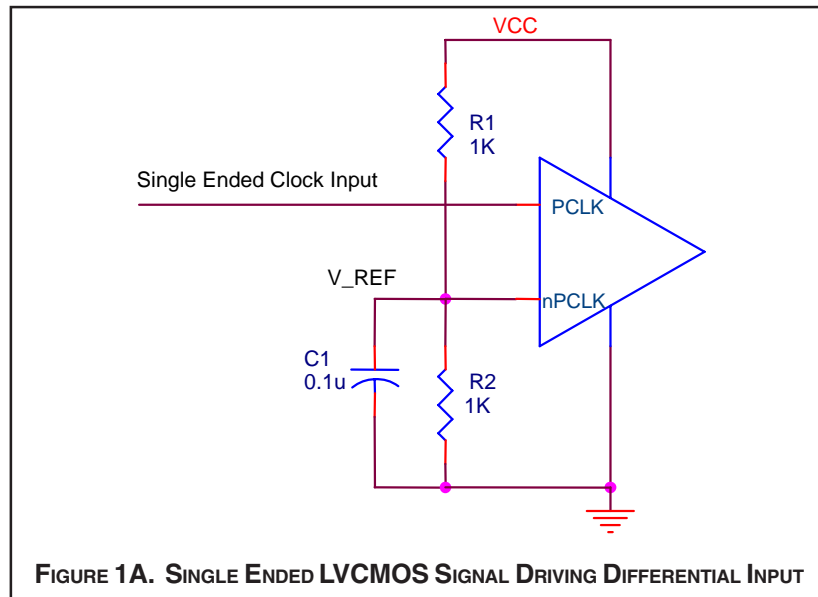
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS LEVELS

Figure 1A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level  $V_{BB}$  generated from the device is connected to

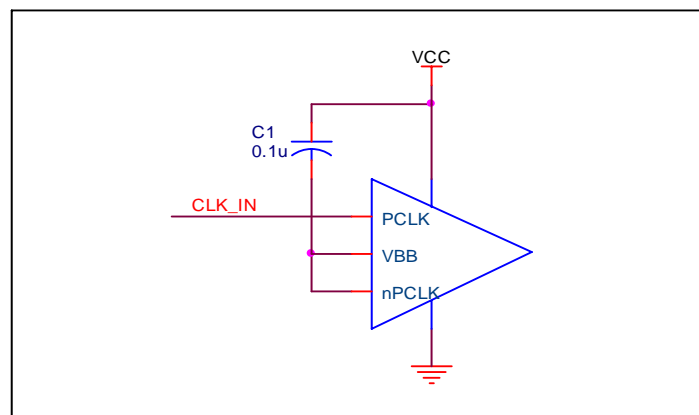
the negative input. The C1 capacitor should be located as close as possible to the input pin.



### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference

voltage level  $V_{BB}$  generated from the device is connected to the negative input.



### TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 2A and Figure 2B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to

ground level. The R3 in Figure 2B can be eliminated and the termination is shown in Figure 2C.

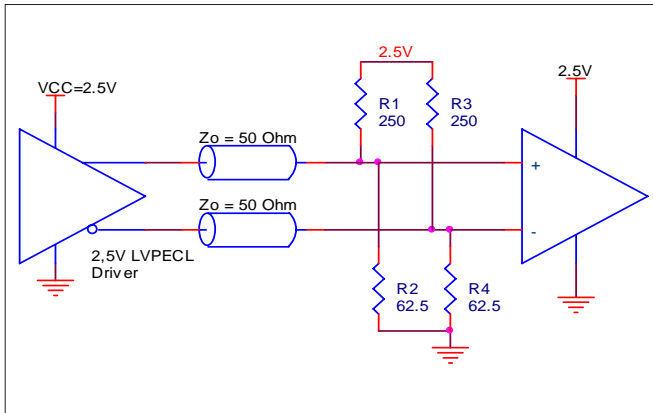


FIGURE 2A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

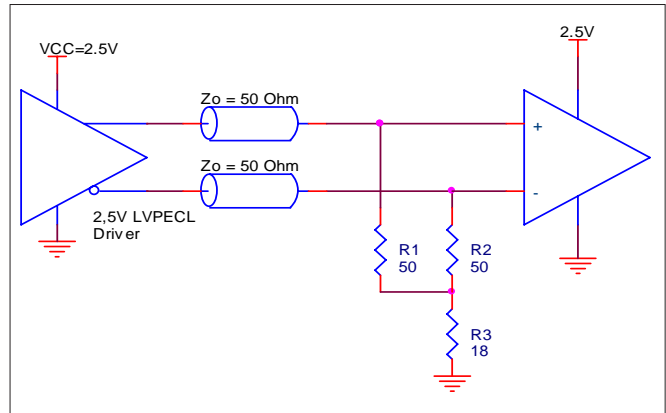


FIGURE 2B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

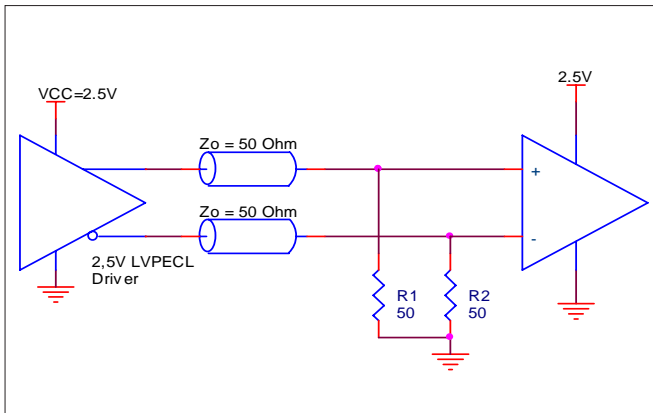


FIGURE 2C. 2.5V LVPECL TERMINATION EXAMPLE



### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

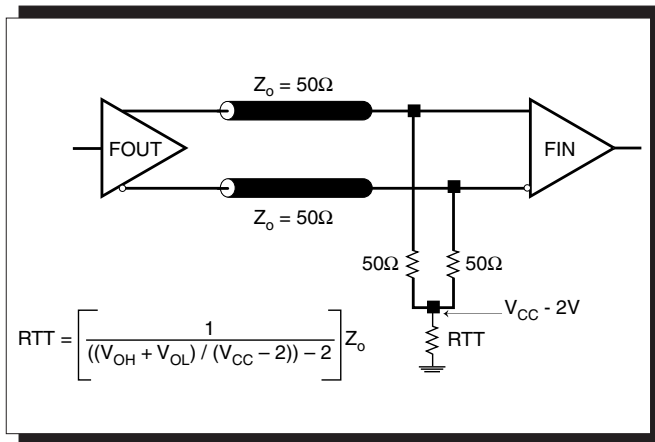


FIGURE 3A. LVPECL OUTPUT TERMINATION

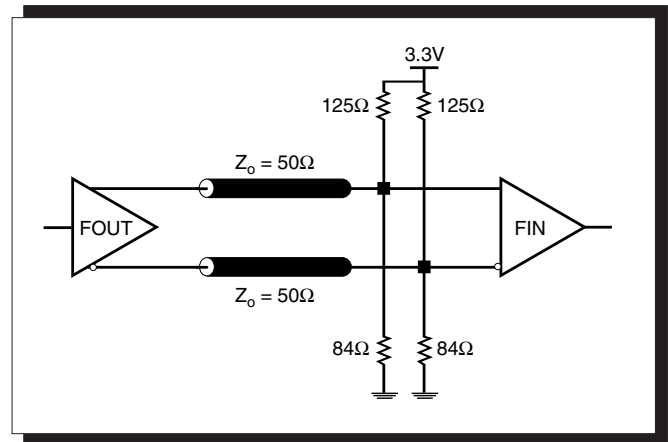


FIGURE 3B. LVPECL OUTPUT TERMINATION

### TERMINATION FOR 5V LVPECL OUTPUT

This section shows examples of 5V LVPECL output termination. *Figure 4A* shows standard termination for 5V LVPECL. The termination requires matched load of 50Ω resistors pull down to

$V_{CC} - 2V = 3V$  at the receiver. *Figure 4B* shows Thevenin equivalence of *Figure 4A*. In actual application where the 3V DC power supply is not available, this approach is normally used.

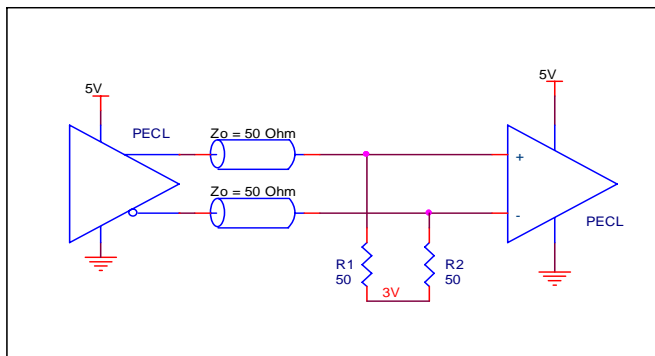


FIGURE 4A. STANDARD 5V PECL OUTPUT TERMINATION

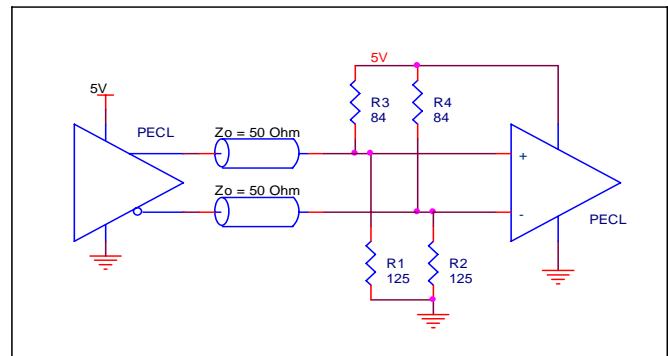
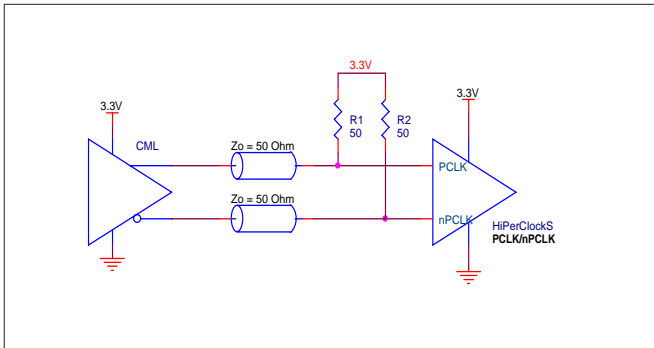


FIGURE 4B. 5V PECL OUTPUT TERMINATION EXAMPLE

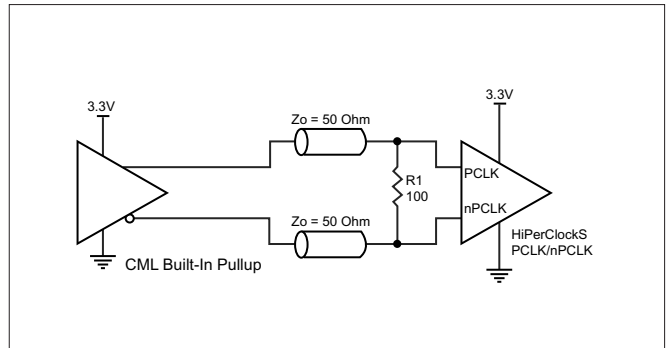
### LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 5A to 5F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested

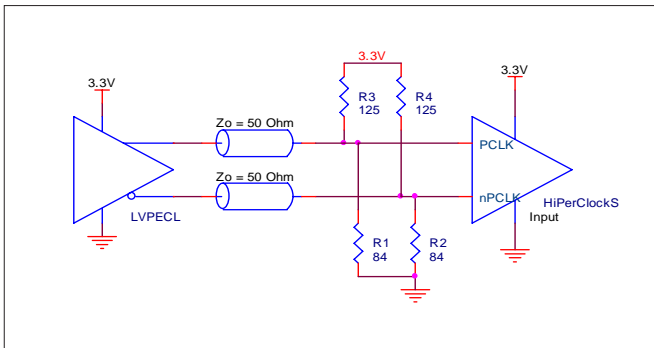
here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



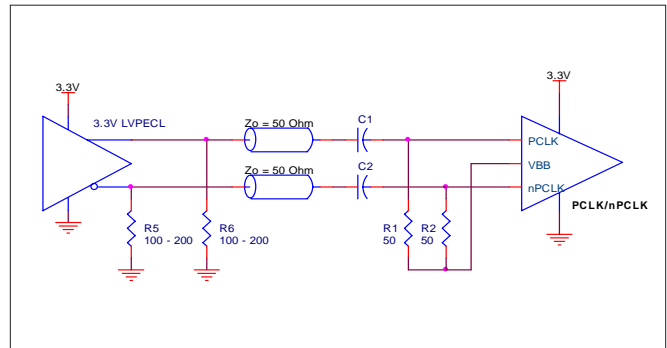
**FIGURE 5A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER**



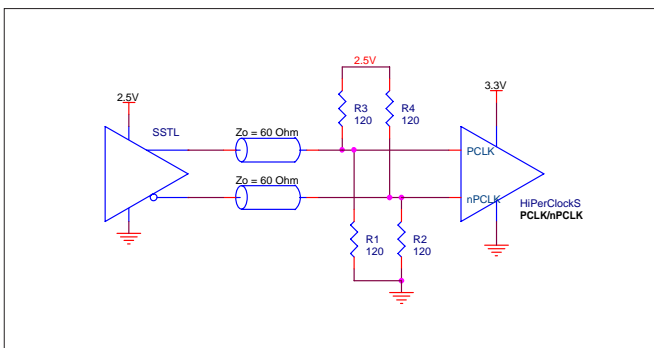
**FIGURE 5B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**



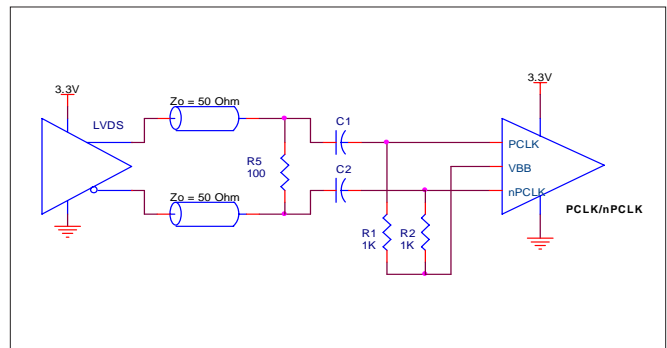
**FIGURE 5C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 5D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**



**FIGURE 5E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**



**FIGURE 5F. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**

### APPLICATION SCHEMATIC EXAMPLE

Figure 6 shows an example of ICS853001 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. Only

one termination example is shown in this schematic. For more termination approaches, please refer to the LVPECL Termination Application Note.

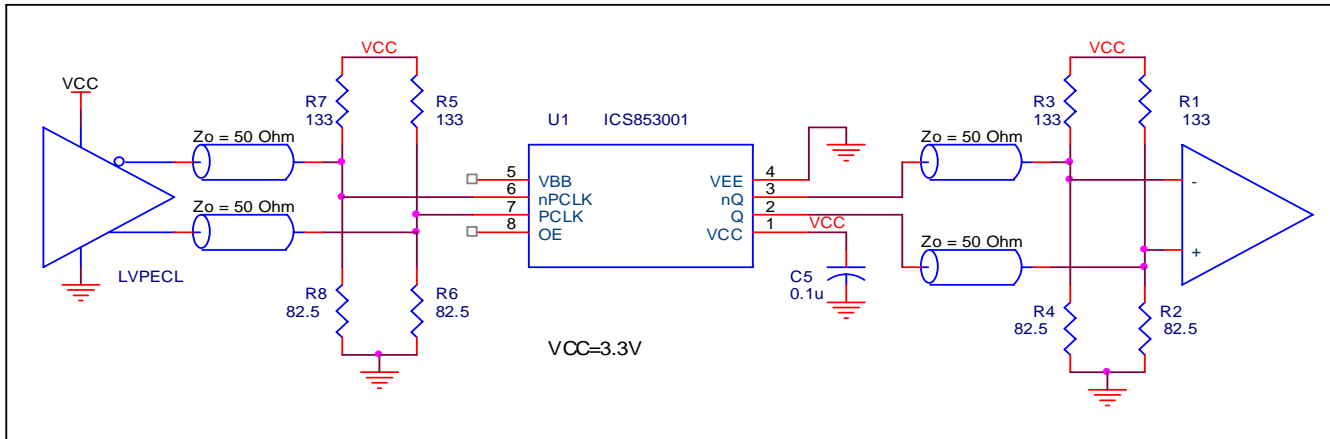


FIGURE 6. APPLICATION SCHEMATIC EXAMPLE

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853001. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS853001 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 5V + 5\% = 5.25V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{CC\_MAX} = 5.25V * 27mA = 141.75mW$
- Power (outputs)<sub>MAX</sub> = **27.83mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V) = 141.75mW + 27.83mW = 169.58mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 5A below. Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.170W * 90.5^\circ C/W = 100.4^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 5A. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN TSSOP, FORCED CONVECTION**

	$\theta_{JA}$ by Velocity (Meters per Second)		
	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

**TABLE 5B. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION**

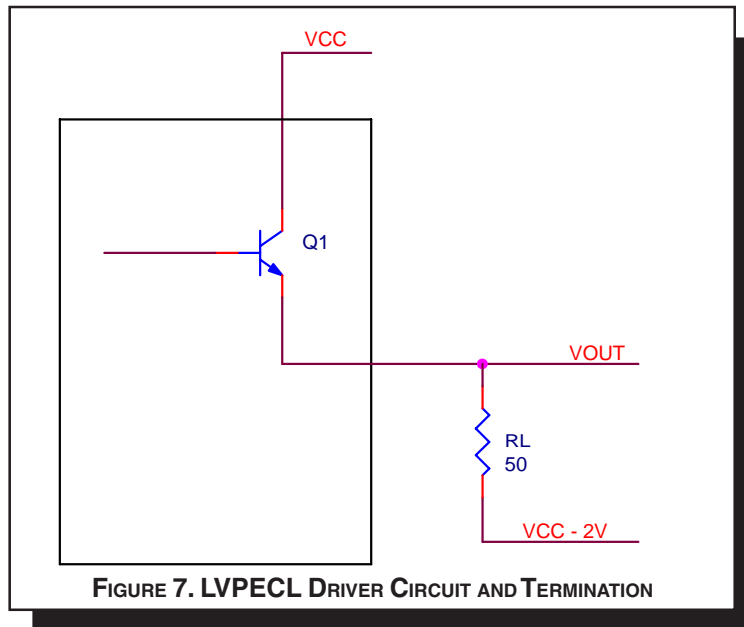
	$\theta_{JA}$ by Velocity (Linear Feet per Minute)		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 1.005V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 1.005$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.78V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.78V$$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 1.005V)/50\Omega] * 1.005V = 20mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.78V)/50\Omega] * 1.78V = 7.83mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 27.83mW$



## RELIABILITY INFORMATION

**TABLE 6A  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD TSSOP**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

**TABLE 6B.  $\theta_{JA}$  vs. AIR FLOW TABLE 8 LEAD SOIC**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS853001 is: 141

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

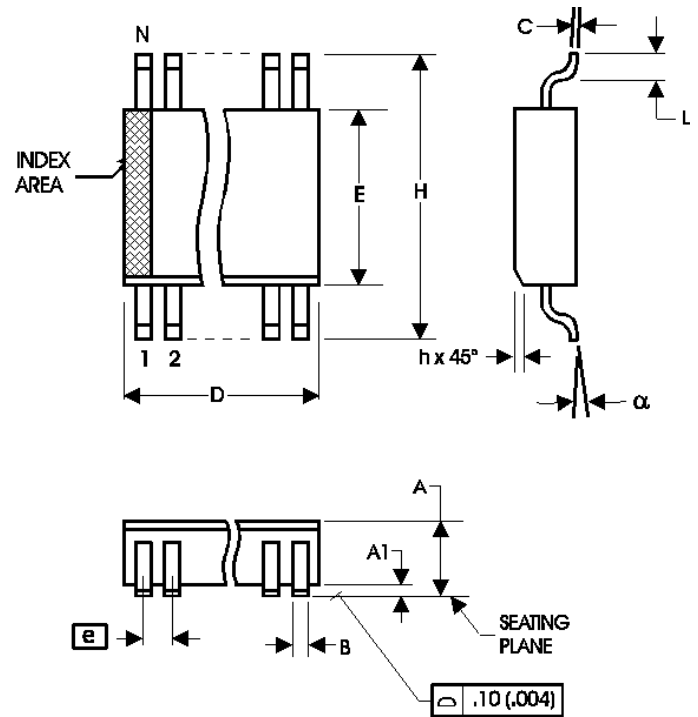
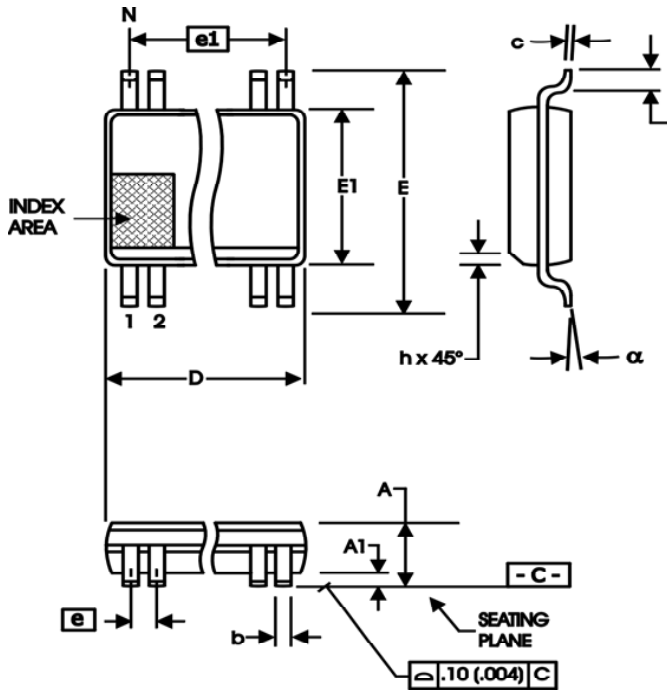


TABLE 7A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
e	0.65 BASIC	
e1	1.95 BASIC	
L	0.40	0.80
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-187

TABLE 7B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-012



# ICS853001

## 1:1, DIFFERENTIAL LVPECL-TO- 2.5V, 3.3V, 5V LVPECL/ECL BUFFER

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853001AG	001A	8 lead TSSOP	tube	-40°C to 85°C
853001AGT	001A	8 lead TSSOP	2500 tape & reel	-40°C to 85°C
853001AGLF	01AL	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
853001AGLFT	01AL	8 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C
853001AM	853001A	8 lead SOIC	tube	-40°C to 85°C
853001AMT	853001A	8 lead SOIC	2500 tape & reel	-40°C to 85°C
853001AMLF	853001AL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
853001AMLFT	853001AL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

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**ICS853001**  
1:1, DIFFERENTIAL LVPECL-TO-  
2.5V, 3.3V, 5V LVPECL/ECL BUFFER

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A		6	Output Rise/Fall Time Diagram - added Labels.	11/24/08