# 4-OUTPUT VERY LOW POWER PCIE GEN1-2-3 BUFFER

9DBV0431

## Description

The 9DBV0431 is a 4-output very low power buffer for 100MHz PCIe Gen1, Gen2 and Gen3 applications. It can also be used for 50M or 125M Ethernet Applications via software frequency selection. The device has 4 output enables for clock management, and 3 selectable SMBus addresses.

## Recommended Application

PCIe Gen1-2-3 Buffer

## Output Features

- 4 - 0.7V low-power HCSL-compatible (LP-HCSL) DIF pairs

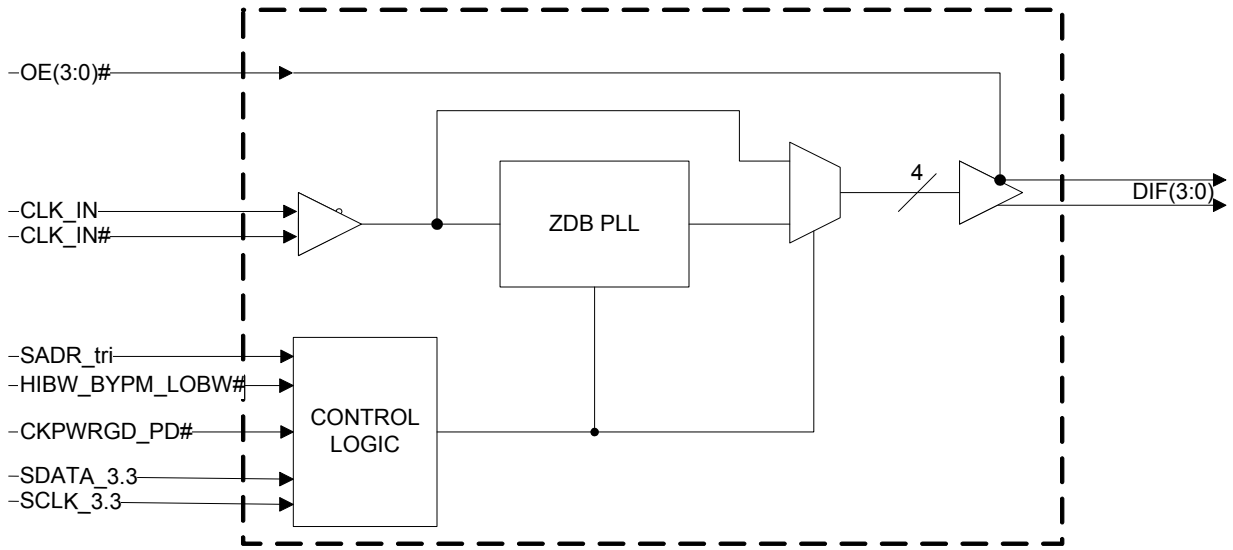
## Key Specifications

- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- Very low additive phase jitter in bypass mode

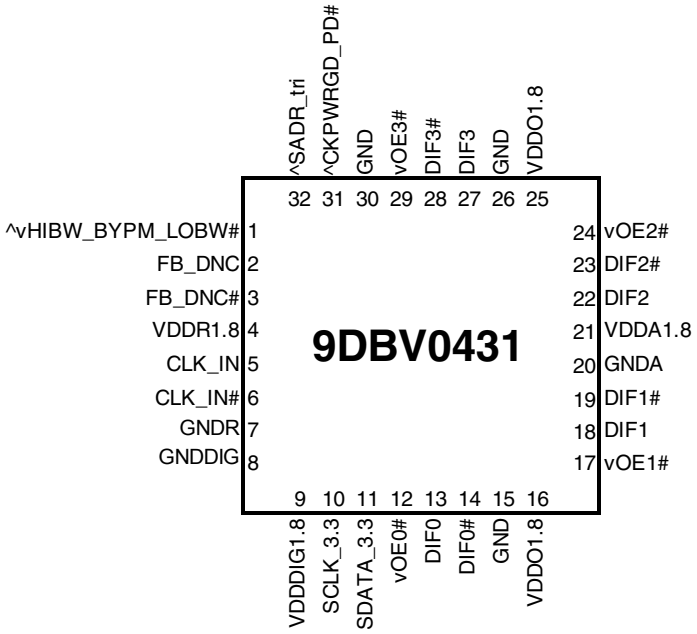
## Features/Benefits

- 1.8V operation; minimal power consumption
- OE# pins; support DIF power management
- HCSL compatible differential input; can be driven by common clock sources
- LP-HCSL differential clock outputs; reduced power and board space
- Programmable Slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- Pin/software selectable PLL bandwidth and PLL Bypass; minimize phase jitter for each application
- Outputs blocked until PLL is locked; clean system start-up
- Software selectable 50MHz or 125MHz PLL operation; useful for Ethernet applications
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 32-pin 5x5mm MLF; minimal board space
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment

## Block Diagram



# Pin Configuration




**32-pin MLF, 5x5 mm, 0.5mm pitch**

^ prefix indicates internal 120KOhm pull up resistor

^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

## SMBus Address Selection Table

| | SADR | Address | + Read/Write bit |
|---|---|---|---|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101011 | x |
| | M | 1101100 | x |
| | 1 | 1101101 | x |

## Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | | PLL |
|---|---|---|---|---|---|---|
| | | | | True O/P | Comp. O/P | |
| 0 | X | X | X | Low | Low | Off |
| 1 | Running | 0 | X | Low | Low | On[1] |
| 1 | Running | 1 | 0 | Running | Running | On[1] |
| 1 | Running | 1 | 1 | Low | Low | On[1] |

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

## Power Connections

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 4 | 7 | Input receiver analog |
| 9 | 8 | Digital Power |
| 16, 25 | 15,20,26,30 | DIF outputs |
| 21 | 20 | PLL Analog |

## Frequency Select Table

| FSEL Byte3 [4:3] | CLK_IN (MHz) | DIFx (MHz) |
|---|---|---|
| **00 (Default)** | 100.00 | CLK_IN |
| 01 | 50.00 | CLK_IN |
| 10 | 125.00 | CLK_IN |
| 11 | Reserved | Reserved |

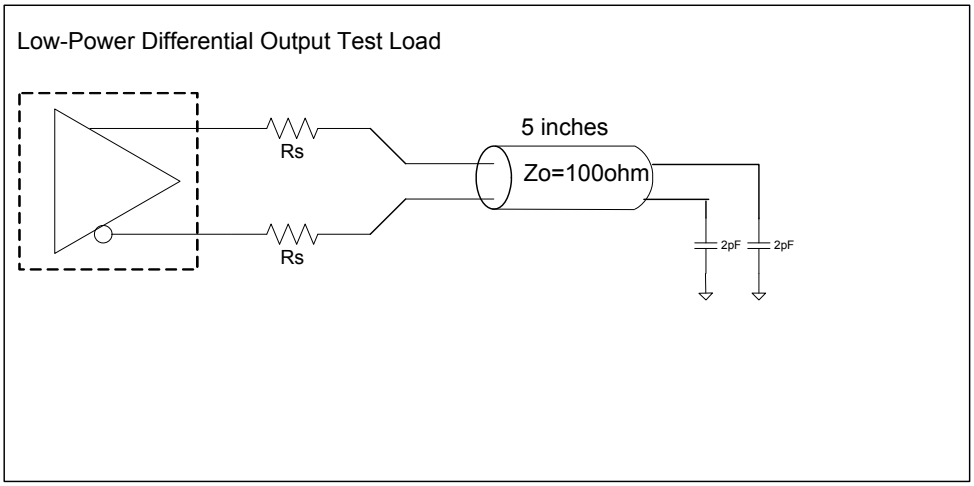
## PLL Operating Mode

| HiBW_BypM_LoBW# | MODE | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|---|---|---|---|
| 0 | PLL Lo BW | 00 | 00 |
| M | Bypass | 01 | 01 |
| 1 | PLL Hi BW | 11 | 11 |

## Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | ^vHIBW_BYPM_LOBW# | LATCHED IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 2 | FB_DNC | DNC | True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 3 | FB_DNC# | DNC | Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 4 | VDDR1.8 | PWR | 1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 5 | CLK_IN | IN | True Input for differential reference clock. |
| 6 | CLK_IN# | IN | Complementary Input for differential reference clock. |
| 7 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 8 | GNDDIG | GND | Ground pin for digital circuitry |
| 9 | VDDDIG1.8 | PWR | 1.8V digital power (dirty power) |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 13 | DIF0 | OUT | Differential true clock output |
| 14 | DIF0# | OUT | Differential Complementary clock output |
| 15 | GND | GND | Ground pin. |
| 16 | VDDO1.8 | PWR | Power supply for outputs, nominally 1.8V. |
| 17 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 18 | DIF1 | OUT | Differential true clock output |
| 19 | DIF1# | OUT | Differential Complementary clock output |
| 20 | GNDA | GND | Ground pin for the PLL core. |
| 21 | VDDA1.8 | PWR | 1.8V power for the PLL core. |
| 22 | DIF2 | OUT | Differential true clock output |
| 23 | DIF2# | OUT | Differential Complementary clock output |
| 24 | vOE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 25 | VDDO1.8 | PWR | Power supply for outputs, nominally 1.8V. |
| 26 | GND | GND | Ground pin. |
| 27 | DIF3 | OUT | Differential true clock output |
| 28 | DIF3# | OUT | Differential Complementary clock output |
| 29 | vOE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 30 | GND | GND | Ground pin. |
| 31 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 32 | ^SADR_tri | LATCHED IN | Tri-level latch to select SMBus Address. See SMBus Address Selection Table. |

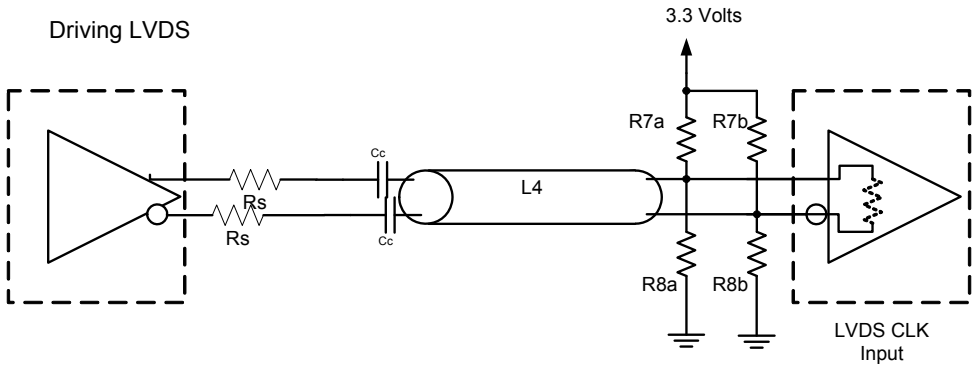
## Test Loads




**Alternate Differential Output Terminations**

| Rs | Zo | Units |
|---|---|---|
| 33 | 100 | Ohms |
| 27 | 85 | |

## Driving LVDS




**Driving LVDS inputs with the 9DBV0431**

| Component | Value | | Note |
|---|---|---|---|
| | Receiver has termination | Receiver does not have termination | |
| R7a, R7b | 10K ohm | 140 ohm | |
| R8a, R8b | 5.6K ohm | 75 ohm | |
| Cc | 0.1 uF | 0.1 uF | |
| Vcm | 1.2 volts | 1.2 volts | |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBV0431. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| 1.8V Supply Voltage | VDDxx | Applies to all VDD pins | -0.5 | | 2.5 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.5 | | $V_{DD}$+0.5V | V | 1, 3 |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins | | | 3.6V | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

## Electrical Characteristics–Clock Input Parameters

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High Voltage - DIF_IN | $V_{IHDIF}$ | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | $V_{ILDIF}$ | Differential inputs (single-ended measurement) | $V_{SS}$ - 300 | 0 | 300 | mV | 1,3 |
| Input Common Mode Voltage - DIF_IN | $V_{COM}$ | Common Mode Input Voltage | 300 | | 725 | mV | 1 |
| Input Amplitude - DIF_IN | $V_{SWING}$ | Peak to Peak value ($V_{IHDIF}$ - $V_{ILDIF}$) | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement | 0 | | 150 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero

[3] The device can be driven from a single ended clock by driving the true clock and biasing the complement clock input to the $V_{BIAS}$, where $V_{BIAS}$ is ($V_{IHHIGH}$ - $V_{IHLOW}$)/2

# Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| 1.8V Supply Voltage | VDD | Supply voltage for core, analog and LVCMOS outputs | 1.7 | 1.8 | 1.9 | V | 1 |
| Ambient Operating Temperature | $T_{COM}$ | Commmercial range | 0 | 25 | 70 | °C | 1 |
| | $T_{IND}$ | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 0.65 $V_{DD}$ | | $V_{DD}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus, low threshold and tri-level inputs | -0.3 | | 0.35 $V_{DD}$ | V | 1 |
| Schmitt Trigger Postive Going Threshold Voltage | $V_{T+}$ | Single-ended inputs, where indicated | 0.4 $V_{DD}$ | | 0.7 $V_{DD}$ | V | 1 |
| Schmitt Trigger Negative Going Threshold Voltage | $V_{T-}$ | Single-ended inputs, where indicated | 0.1 $V_{DD}$ | | 0.4 $V_{DD}$ | V | 1 |
| Hysteresis Voltage | $V_H$ | $V_{T+}$ - $V_{T-}$ | 0.1 $V_{DD}$ | | 0.4 $V_{DD}$ | V | 1 |
| Output High Voltage | $V_{IH}$ | Single-ended outputs, except SMBus. $I_{OH}$ = -2mA | $V_{DD}$-0.45 | | | V | 1 |
| Outputt Low Voltage | $V_{IL}$ | Single-ended outputs, except SMBus. $I_{OL}$ = -2mA | | | 0.45 | V | 1 |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD | -5 | | 5 | uA | 1 |
| | $I_{INP}$ | Single-ended inputs<br>$V_{IN}$ = 0 V; Inputs with internal pull-up resistors<br>$V_{IN}$ = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Input Frequency | $F_{ibyp}$ | Bypass mode | 1 | | 200 | MHz | 2 |
| | $F_{ipll100}$ | 100MHz PLL mode | 60 | 100.00 | 110 | MHz | 2 |
| | $F_{ipll125}$ | 125MHz PLL mode | 75 | 125.00 | 137.5 | MHz | 2 |
| | $F_{ipll62}$ | 50MHz PLL mode | 30 | 50.00 | 55 | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.6 | 1 | ms | 1,2 |
| Input SS Modulation Frequency | $f_{MODIN}$ | Allowable Frequency (Triangular Modulation) | 30 | 31.500 | 33 | kHz | 1 |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion<br>DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of single-ended control inputs | | | 5 | ns | 1,2 |
| Trise | $t_R$ | Rise time of single-ended control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | $V_{ILSMB}$ | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | $V_{IHSMB}$ | | 2.1 | | 3.6 | V | 1 |
| SMBus Output Low Voltage | $V_{OLSMB}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| SMBus Sink Current | $I_{PULLUP}$ | @ $V_{OL}$ | 4 | | | mA | 1 |
| Nominal Bus Voltage | $V_{DDSMB}$ | 3.3V bus voltage | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 400 | kHz | 1,5 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

# Electrical Characteristics–DIF 0.7V Low Power HCSL Outputs

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | Trf | Scope averaging on 3.0V/ns setting | 1.1 | 2 | 3 | V/ns | 1, 2, 3 |
| | | Scope averaging on 2.0V/ns setting | 1.9 | 3 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 7 | 20 | % | 1, 2, 4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 774 | 850 | mV | 1,7 |
| Voltage Low | $V_{LOW}$ | | -150 | 18 | 150 | | 1,7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 821 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -15 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | 1536 | | mV | 1,2,7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 414 | 550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 13 | 140 | mV | 1, 6 |

[1]Guaranteed by design and characterization, not 100% tested in production. $C_L$ = 2pF with $R_S$ = 33Ω for Zo = 50Ω (100Ω differential trace impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

# Electrical Characteristics–Current Consumption

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDAOP}$ | VDDA+VDDR, PLL Mode, @100MHz | | 11 | 15 | mA | 1 |
| | $I_{DDOP}$ | VDD1.8, All outputs active @100MHz | | 25 | 35 | mA | 1 |
| Powerdown Current | $I_{DDAPD}$ | VDDA+VDDR, PLL Mode, @100MHz | | | 1 | mA | 1,2 |
| | $I_{DDPD}$ | VDD1.8, Outputs Low/Low | | | 1.2 | mA | 1, 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

# Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characterisitics

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| PLL Bandwidth | BW | -3dB point in High BW Mode | 2 | 2.7 | 4 | MHz | 1,5 |
| | | -3dB point in Low BW Mode | 1 | 1.4 | 2 | MHz | 1,5 |
| PLL Jitter Peaking | $t_{JPEAK}$ | Peak Pass band Gain | | 1.2 | 2 | dB | 1 |
| Duty Cycle | $t_{DC}$ | Measured differentially, PLL Mode | 45 | 50.1 | 55 | % | 1 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially, Bypass Mode @100MHz | -1 | 0 | 1 | % | 1,3 |
| Skew, Input to Output | $t_{pdBYP}$ | Bypass Mode, $V_T$ = 50% | 3000 | 3600 | 4500 | ps | 1 |
| | $t_{pdPLL}$ | PLL Mode $V_T$ = 50% | 0 | 92 | 200 | ps | 1,4 |
| Skew, Output to Output | $t_{sk3}$ | $V_T$ = 50% | | 28 | 50 | ps | 1,4 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode | | 16 | 50 | ps | 1,2 |
| | | *Additive* Jitter in Bypass Mode | | 0.1 | 25 | ps | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

[5] The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

# Electrical Characteristics–Phase Jitter Parameters

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|---|---|---|---|---|---|---|---|---|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 34 | 52 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.9 | 1.4 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2.2 | 2.5 | 3.1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.5 | 0.6 | 1 | ps (rms) | 1,2,4 |
| | $t_{jphSGMII}$ | 125MHz, 1.5MHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 1.9 | 2 | NA | ps (rms) | 1,6 |
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 0.6 | 5 | N/A | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.1 | 0.3 | N/A | ps (rms) | 1,2,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.05 | 0.1 | N/A | ps (rms) | 1,2,5 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.05 | 0.1 | N/A | ps (rms) | 1,2,4, 5 |
| | $t_{jphSGMII}$ | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 0.15 | 0.3 | N/A | ps (rms) | 1,6 |

[1] Applies to all outputs, with device driven by 9FG432AKLF or equivalent.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final ratification by PCI SIG.

[5] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

[6] Applies to all differential outputs

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **IDT (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Note: SMBus address is latched on SADR pin.**

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **IDT (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: Output Enable Register** [1]

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 1 |
| **Bit 6** | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 5** | DIF OE2 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 4** | Reserved | | | | | 1 |
| **Bit 3** | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 0** | Reserved | | | | | 1 |

1. A low on these bits will overide the OE# pin and force the differential output Low/Low

**SMBus Table: PLL Operating Mode and Output Amplitude Control Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | PLLMODERB1 | PLL Mode Readback Bit 1 | **R** | See PLL Operating Mode Table | | Latch |
| **Bit 6** | PLLMODERB0 | PLL Mode Readback Bit 0 | **R** | | | Latch |
| **Bit 5** | PLLMODE_SWCNTRL | Enable SW control of PLL Mode | RW | Values in B1[7:6] set PLL Mode | Values in B1[4:3] set PLL Mode | 0 |
| **Bit 4** | PLLMODE1 | PLL Mode Control Bit 1 | RW[1] | See PLL Operating Mode Table | | 0 |
| **Bit 3** | PLLMODE0 | PLL Mode Control Bit 0 | RW[1] | | | 0 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.7V | 1 |
| **Bit 0** | AMPLITUDE 0 | | RW | 10= 0.8V | 11 = 0.9V | 0 |

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 1 |
| **Bit 6** | SLEWRATESEL DIF3 | Slew Rate Selection | RW | 2 V/ns | 3 V/ns | 1 |
| **Bit 5** | SLEWRATESEL DIF2 | Slew Rate Selection | RW | 2 V/ns | 3 V/ns | 1 |
| **Bit 4** | Reserved | | | | | 1 |
| **Bit 3** | SLEWRATESEL DIF1 | Slew Rate Selection | RW | 2 V/ns | 3 V/ns | 1 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | SLEWRATESEL DIF0 | Slew Rate Selection | RW | 2 V/ns | 3 V/ns | 1 |
| **Bit 0** | Reserved | | | | | 1 |

**SMBus Table: Frequency Select Control Register**

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 1 |
| **Bit 6** | Reserved | | | | | 1 |
| **Bit 5** | FREQ_SEL_EN | Enable SW selection of frequency | RW | SW frequency change disabled | SW frequency change enabled | 0 |
| **Bit 4** | FSEL1 | Freq. Select Bit 1 | RW[1] | See Frequency Select Table | | 0 |
| **Bit 3** | FSEL0 | Freq. Select Bit 0 | RW[1] | | | 0 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | Reserved | | | | | 1 |
| **Bit 0** | SLEWRATESEL FB | Adjust Slew Rate of FB | RW | 2 V/ns | 3 V/ns | 1 |

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

**Byte 4 is Reserved and reads back 'hFF**

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | RID3 | Revision ID | **R** | A rev = 0000 | | 0 |
| **Bit 6** | RID2 | | **R** | | | 0 |
| **Bit 5** | RID1 | | **R** | | | 0 |
| **Bit 4** | RID0 | | **R** | | | 0 |
| **Bit 3** | VID3 | VENDOR ID | **R** | 0001 = IDT | | 0 |
| **Bit 2** | VID2 | | **R** | | | 0 |
| **Bit 1** | VID1 | | **R** | | | 0 |
| **Bit 0** | VID0 | | **R** | | | 1 |

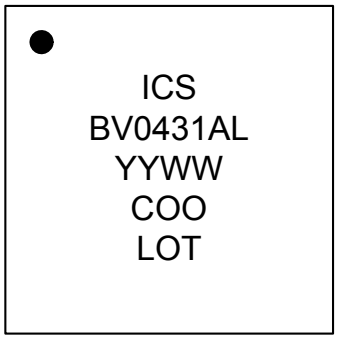
**SMBus Table: Device Type/Device ID**

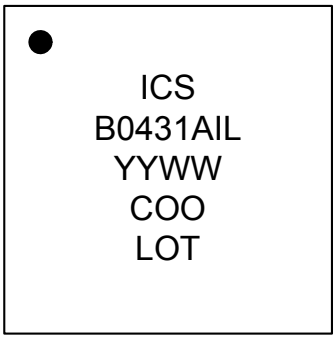
| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Device Type1 | Device Type | **R** | 00 = FGV, 01 = DBV, 10 = DMV, 11= Reserved | | 0 |
| **Bit 6** | Device Type0 | | **R** | | | 1 |
| **Bit 5** | Device ID5 | Device ID | **R** | 000100 binary or 04 hex | | 0 |
| **Bit 4** | Device ID4 | | **R** | | | 0 |
| **Bit 3** | Device ID3 | | **R** | | | 0 |
| **Bit 2** | Device ID2 | | **R** | | | 1 |
| **Bit 1** | Device ID1 | | **R** | | | 0 |
| **Bit 0** | Device ID0 | | **R** | | | 0 |

**SMBus Table: Byte Count Register**

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 0 |
| **Bit 6** | Reserved | | | | | 0 |
| **Bit 5** | Reserved | | | | | 0 |
| **Bit 4** | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| **Bit 3** | BC3 | | RW | | | 1 |
| **Bit 2** | BC2 | | RW | | | 0 |
| **Bit 1** | BC1 | | RW | | | 0 |
| **Bit 0** | BC0 | | RW | | | 0 |

## Marking Diagrams




Notes:

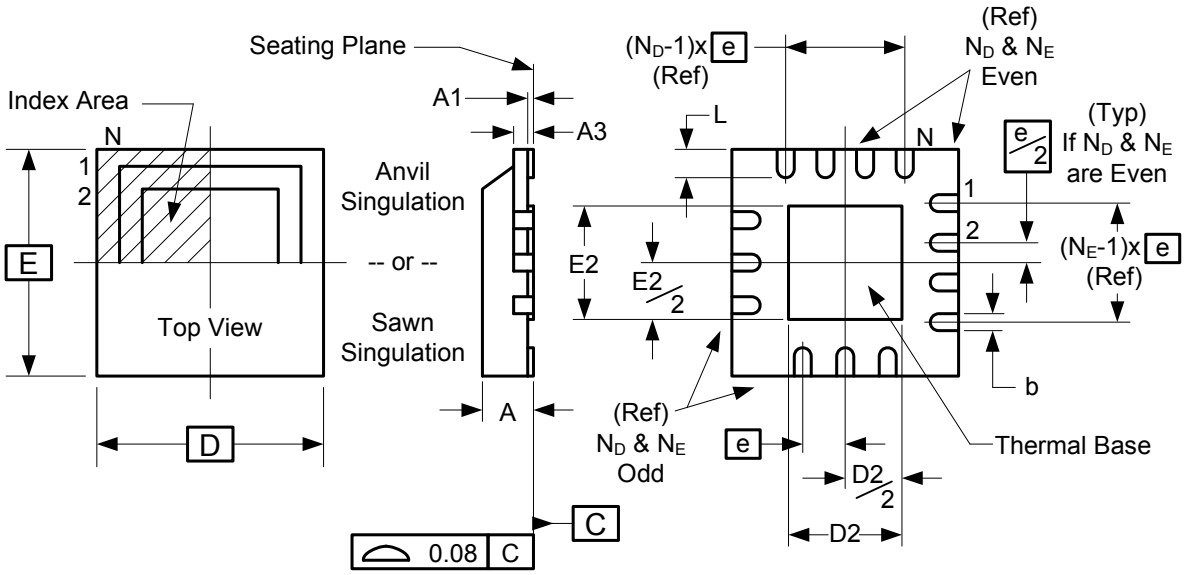
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “L” denotes RoHS compliant package.
6. “I” denotes industrial temperature range device.

## Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to Case | NLG32 | 42 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to Base | | 2.4 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to Air, still air | | 39 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow | | 33 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow | | 28 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow | | 27 | °C/W | 1 |

[1]ePad soldered to board

## Package Outline and Package Dimensions (NLG32)




| | Millimeters | |
|---|---|---|
| **Symbol** | **Min** | **Max** |
| A | 0.80 | 1.00 |
| A1 | 0 | 0.05 |
| A3 | 0.20 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 5.00 x 5.00 | |
| D2 MIN./MAX. | 3.00 | 3.30 |
| E2 MIN./MAX. | 3.00 | 3.30 |
| L MIN./MAX. | 0.30 | 0.50 |
| N | 32 | |
| $N_D$ | 8 | |
| $N_E$ | 8 | |

## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 9DBV0431AKLF | Trays | 32-pin MLF | 0 to +70° C |
| 9DBV0431AKLFT | Tape and Reel | 32-pin MLF | 0 to +70° C |
| 9DBV0431AKILF | Trays | 32-pin MLF | -40 to +85° C |
| 9DBV0431AKILFT | Tape and Reel | 32-pin MLF | -40 to +85° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

**"A" is the device revision designator (will not correlate with the datasheet revision).**

## Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|---|---|---|---|---|
| 0.1 | RDW | 5/12/2012 | Initial Release | - |
| 0.2 | RDW | 6/21/2012 | 1. SMBus Bytes 0 and 2 modified per design. | |
| 0.3 | RDW | 6/22/2012 | 1. Changed pins 16 & 25 from VDDIO to VDD1.8<br>2. Updated/Corrected Power Connections Table.<br>3. Removed references to VDDIO in electrical tables. | |
| 0.4 | RDW | 7/6/2012 | 1. Extensive changes to page 1 text: Description, Recommended Application, Output Features, Features/Benefits, DS Title.<br>2. Indicated default value in Frequency Select Table.<br>3. Pins 2,3 changed from FB,FB# to FB_DNC,FB_DNC# to indicate that these pins are Do Not Connect (DNC).<br>4. Default value of Frequency Select Table highlighted. | 1-3 |
| A | RDW | 8/13/2012 | 1. Removed "Differential" from DS title and Recommended Application, corrected typo's in Description.<br>2. Corrected spelling error in pullup/pulldown text under pinout<br>3. Updated all electrical tables and added "Industry Limit" column to "Phase Jitter Parameters".<br>4. Updated Byte3[0] to be consistent with Byte 2. Updated Byte6[7:6] definition.<br>5. Added thermal data to page 12.<br>6. Added NLG32 to "Package Outline and Package Dimensions" on page 13.<br>7. Move to final | 1,2,5-8,10, 12,13 |

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