Differential-to-LVDS Fanout Buffer w/Divider and Glitchless Switch

ICS854S1208I

DATA SHEET

General Description

The ICS854S1208I is a low skew, 8 output LVDS Fanout Buffer with selectable divider. The ICS854S1208I has 2 selectable inputs that accept a variety of differential input types. The device provides the capability to suppress any glitch at the outputs of the device during an input clock switch to enhance clock redundancy in fault tolerant applications.

The divide select inputs, DIV_SELA and DIV_SELB, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The output enable pins assigned to each output, support enabling and disabling each output individually.

The ICS854S1208I is characterized at full 3.3V or 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS854S1208I ideal for high performance applications.

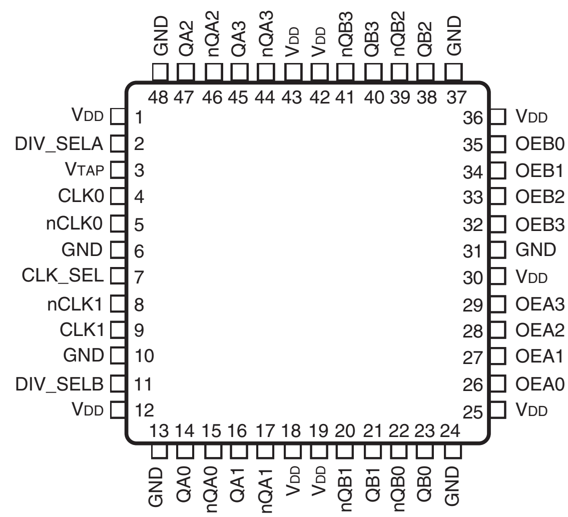
Features

- Eight differential LVDS output pairs
  Each output has individual synchronous output enable
- Two selectable differential CLKx, nCLKx input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Maximum output frequency: 1.5GHz
- Independent bank control for ÷1 or ÷2 operation
- Glitchless output behavior during input switch
- Output skew: 40ps (maximum)
- Bank skew: 35ps (maximum)
- Full 3.3V or 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Supply Mode Operation Table

3.3V Operation	2.5V Operation
V_{DD} = 3.3V	V_{DD} = 2.5V
V_{TAP} = Float	V_{TAP} = 2.5V

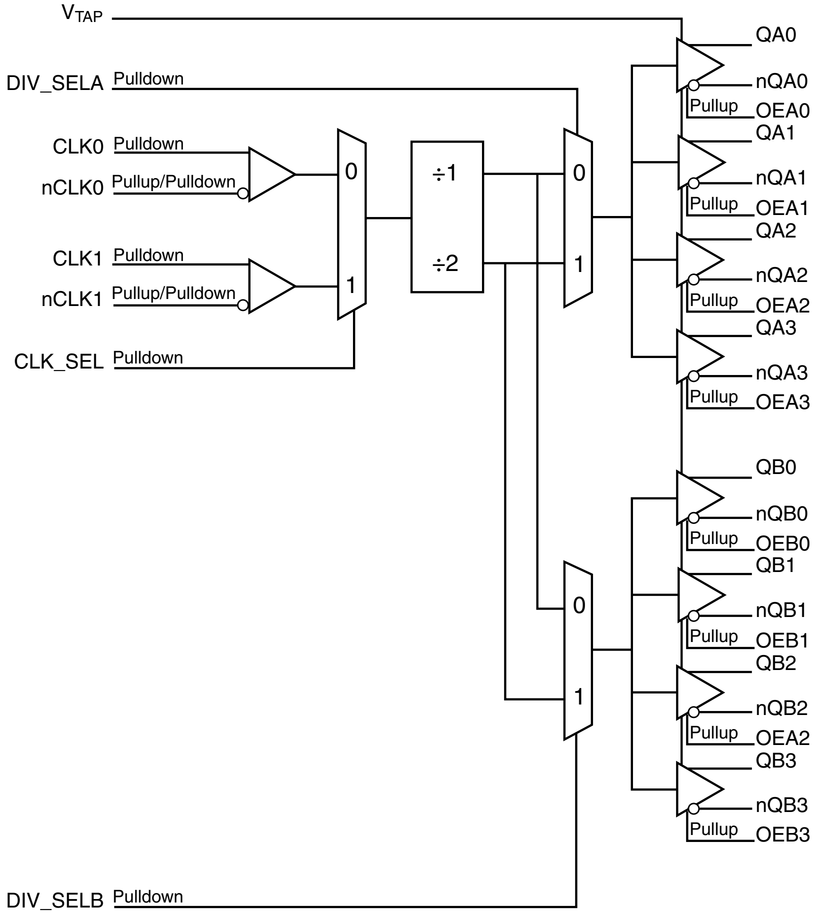
Pin Assignment



ICS854S1208I

48-Pin TQFP, E-Pad
7mm x 7mm x 1mm package body
Y Package
Top View

Block Diagram



Function Description

The ICS854S1208I has a glitch free input mux that is controlled by the CLK_SEL pin. It is designed to switch between 2 input clocks whether running or not. In the case where both clocks are running, when CLK_SEL changes, the output clocks go low after one cycle of the output clock (nominally). The outputs then stay low for one cycle of the new input clock (nominally) and then begin to follow the new input clock. This is shown in *Figure 1A.*

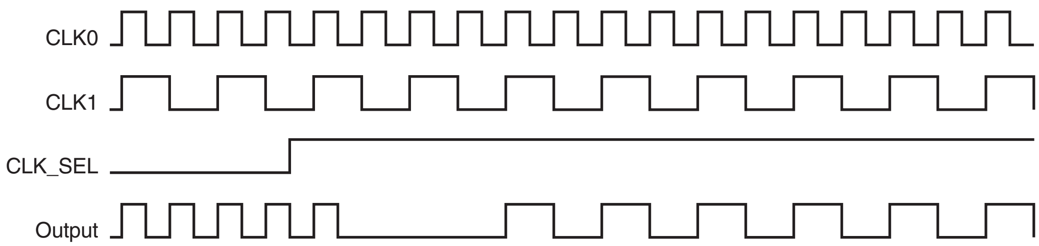


Figure 1A. CLK_SEL Timing Diagram

Another case is where one of the inputs was selected and running but has since stopped (either high or low). If a CLK_SEL event happens after a clock has stopped, the output change can take effect up to 1µs after the input clock stopped. The output will go low and then follow the second period of the new clock input. Figure 1B shows an example of this.

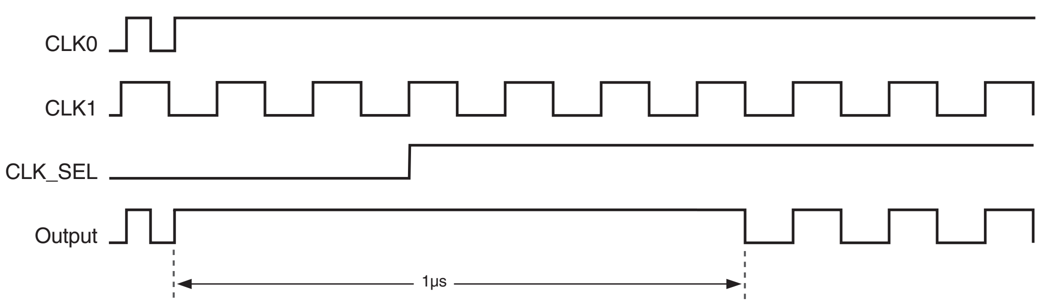


Figure 1B. CLK_SEL with Bad Input Timing Diagram

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 12, 18, 19, 25, 30, 36, 42, 43	V_{DD}	Power		Power supply pins.
2	DIV_SELA	Input	Pulldown	Controls frequency division for QA[0:3], nQA[0:3] outputs. LVCMOS / LVTTL interface levels.
3	V_{TAP}	Power		Power supply mode. See *Supply Mode Operation Table* on page 1.
4	CLK0	Input	Pulldown	Non-inverting differential clock input.
5	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
6, 10, 13, 24, 31, 37, 48	GND	Power		Power supply ground.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1/nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels.
8	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
9	CLK1	Input	Pulldown	Non-inverting differential clock input.
11	DIV_SELB	Input	Pulldown	Controls frequency division for QB[0:3], nQB[0:3] outputs. LVCMOS / LVTTL interface levels.
14, 15	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
16, 17	QA1, nQA1	Output		Differential output pair. LVDS interface levels.
20, 21	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
22, 23	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
26	OEA0	Input	Pullup	Output enable for QA0 output pair. LVCMOS/LVTTL interface levels. See Table 3A.
27	OEA1	Input	Pullup	Output enable for QA1 output pair. LVCMOS/LVTTL interface levels. See Table 3A.
28	OEA2	Input	Pullup	Output enable for QA2 output pair. LVCMOS/LVTTL interface levels. See Table 3A.
29	OEA3	Input	Pullup	Output enable for QA3 output pair. LVCMOS/LVTTL interface levels. See Table 3A.
32	OEB3	Input	Pullup	Output enable for QB3 output pair. LVCMOS/LVTTL interface levels. See Table 3B.
33	OEB2	Input	Pullup	Output enable for QB2 output pair. LVCMOS/LVTTL interface levels. See Table 3B.
34	OEB1	Input	Pullup	Output enable for QB1 output pair. LVCMOS/LVTTL interface levels. See Table 3B.
35	OEB0	Input	Pullup	Output enable for QB0 output pair. LVCMOS/LVTTL interface levels. See Table 3B.
38, 39	QB2, nQB2	Output		Differential output pair. LVDS interface levels.
40, 41	QB3, nQB3	Output		Differential output pair. LVDS interface levels.
44, 45	nQA3, QA3	Output		Differential output pair. LVDS interface levels.
46, 47	nQA2, QA2	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. OEAx Function Table

Inputs	Outputs	
OEA[0:3]	QA[0:3]	nQA[0:3]
0	LOW	HIGH
1 (default)	Active	Active

Table 3B. OEBx Function Table

Inputs	Outputs	
OEB[0:3]	QB[0:3]	nQB[0:3]
0	LOW	HIGH
1 (default)	Active	Active

Table 3C. DIV_SELA Function Table

Input	
DIV_SELA	Frequency Division
0 (default)	÷1
1	÷2

Table 3D. DIV_SELB Function Table

Input	
DIV_SELB	Frequency Division
0 (default)	÷1
1	÷2

Table 3E. CLK_SEL Function Table

Input	
CLK_SEL	Input Selection
0 (default)	CLK0, nCLK0
1	CLK1, nCLK1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{TAP}	Power Supply Mode		Float			V
I_{DD}	Power Supply Current				305	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{TAP}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				290	mA
I_{TAP}	Power Supply Current				2.2	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% or V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2.2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	DIV_SELx, CLK_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		OEA[3:0], OEB[3:0]	V_{DD} = V_{IN} = 3.465V or 2.625V			10	µA
I_{IL}	Input Low Current	DIV_SELx, CLK_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		OEA[3:0], OEB[3:0]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 4D. Differential DC Characteristics, V_{DD} = 3.3V ± 5% or V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, nCLK0, nCLK1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		nCLK0, nCLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4E. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2		1.47	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4F. LVDS DC Characteristics, V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15		1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				1.5	GHz
t_{PD}	Propagation Delay; NOTE 1		0.7		1.75	ns
*t*sk(o)	Output Skew; NOTE 2, 3				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				400	ps
*t*sk(b)	Bank Skew; NOTE 3, 5				35	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	55		250	ps
odc	Output Duty Cycle	$f \leq$ 750MHz	44		56	%
t_{EN}	Output Enable Time; NOTE 6				10	ns
t_{DIS}	Output Disable Time; NOTE 6				10	ns

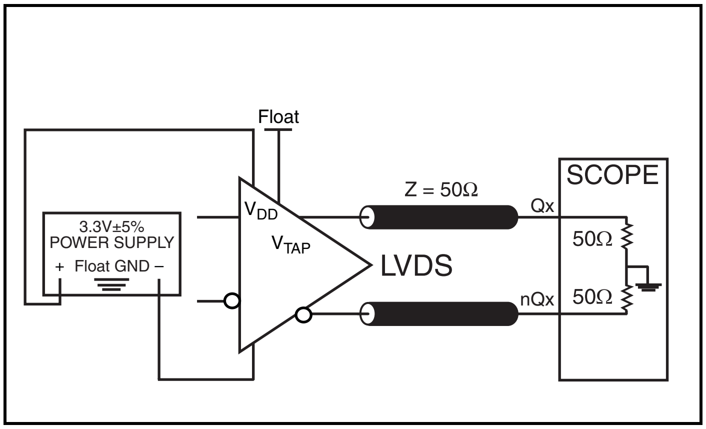
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential cross points.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the differential cross points.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltage, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at the differential cross points.
NOTE 5: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 5B. AC Characteristics, V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C to 85°C

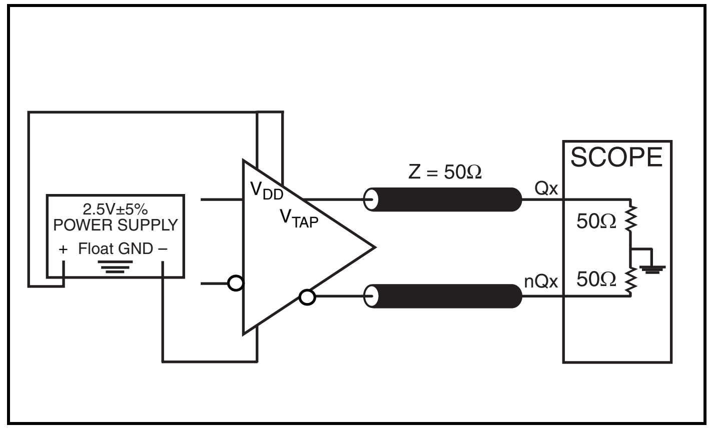
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				1.5	GHz
t_{PD}	Propagation Delay; NOTE 1		0.6		1.8	ns
*t*sk(o)	Output Skew; NOTE 2, 3				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				400	ps
*t*sk(b)	Bank Skew; NOTE 3, 5				35	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		275	ps
odc	Output Duty Cycle	$f \leq$ 750MHz	44		56	%
t_{EN}	Output Enable Time; NOTE 6				10	ns
t_{DIS}	Output Disable Time; NOTE 6				10	ns

For NOTES, see Table 5A above.

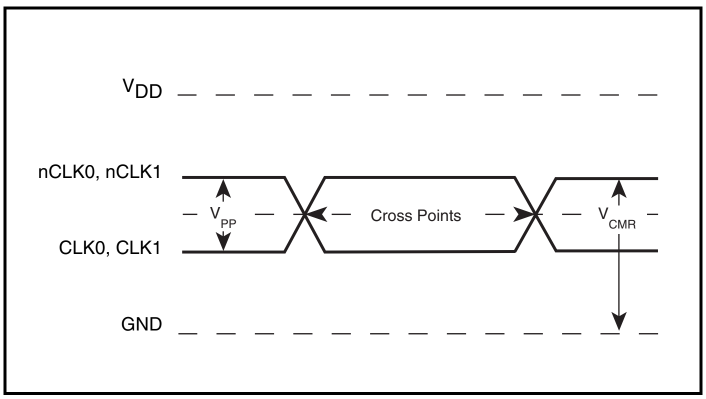
Parameter Measurement Information



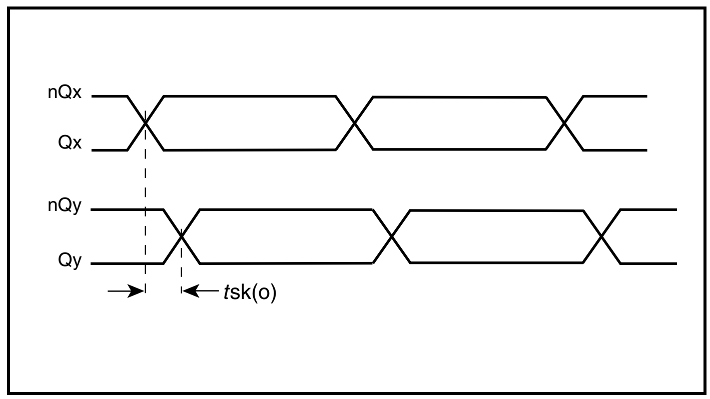
3.3V LVDS Output Load AC Test Circuit



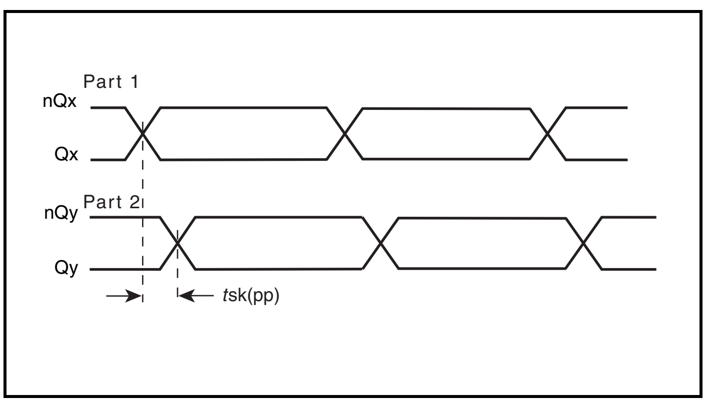
2.5V LVDS Output Load AC Test Circuit



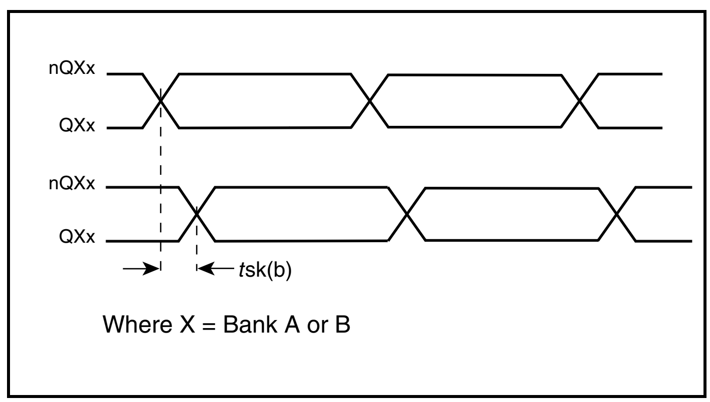
Differential Input Level



Output Skew

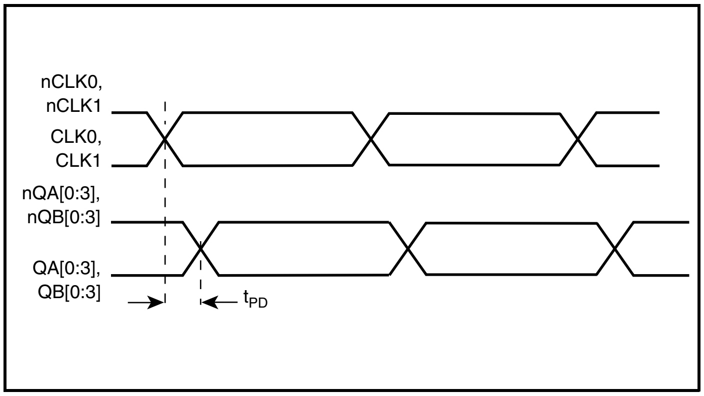


Part-to-Part Skew

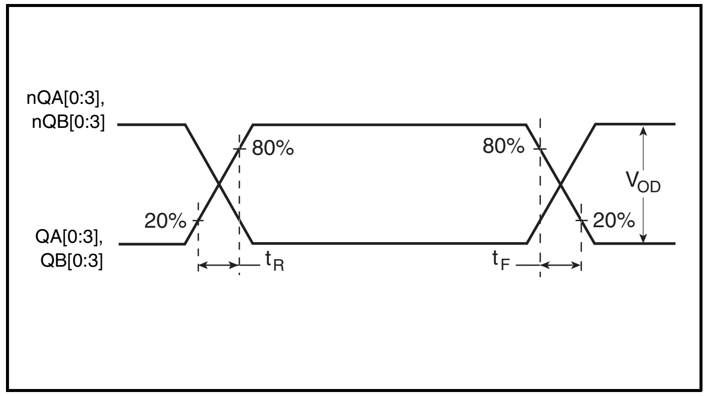


Bank Skew

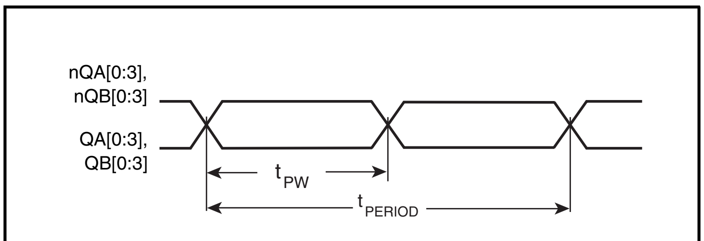
Parameter Measurement Information, continued



Propagation Delay

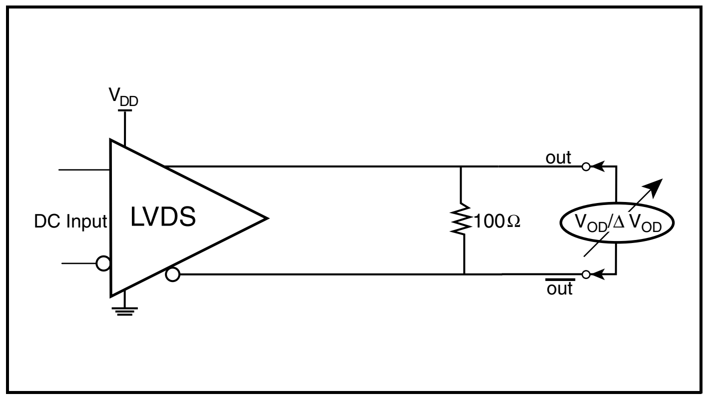


Output Rise/Fall Time

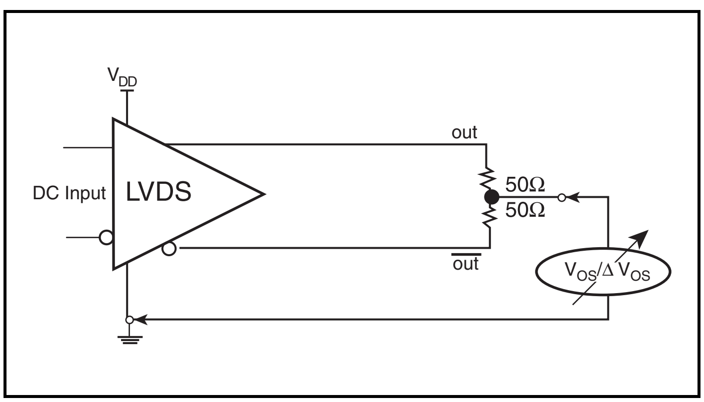


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

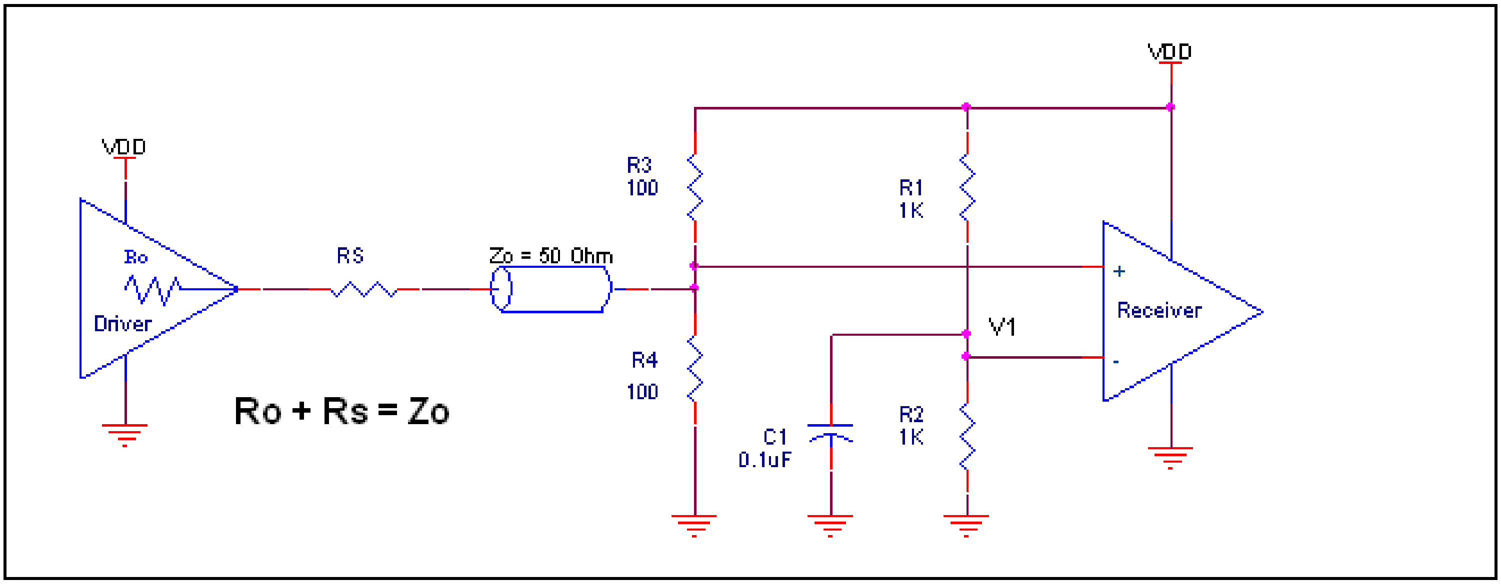


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications requiring only one differential input, the unused CLK and nCLK input can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK pin to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

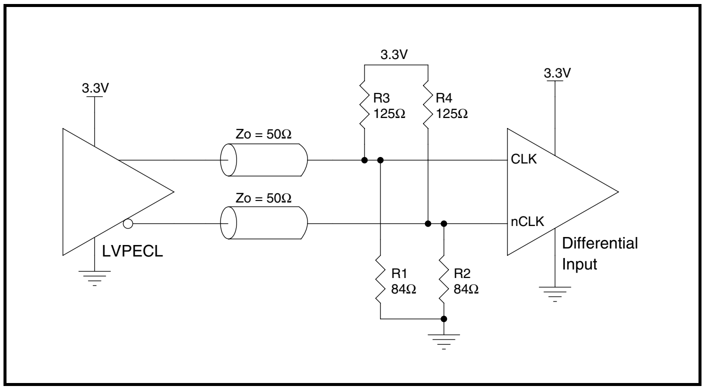
Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.



3A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

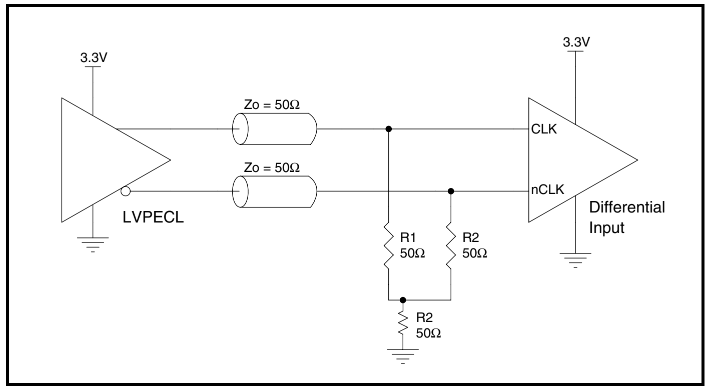


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

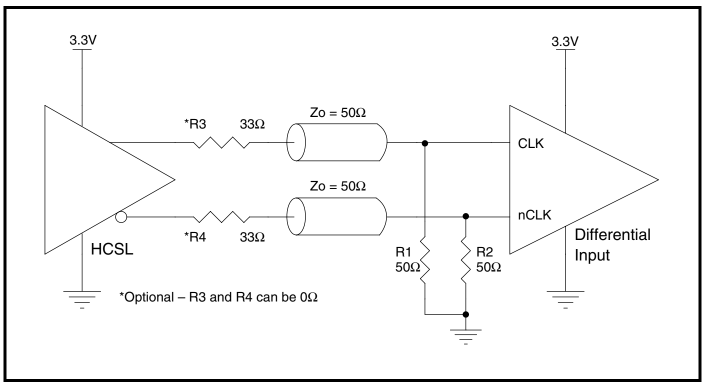


Figure 3C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

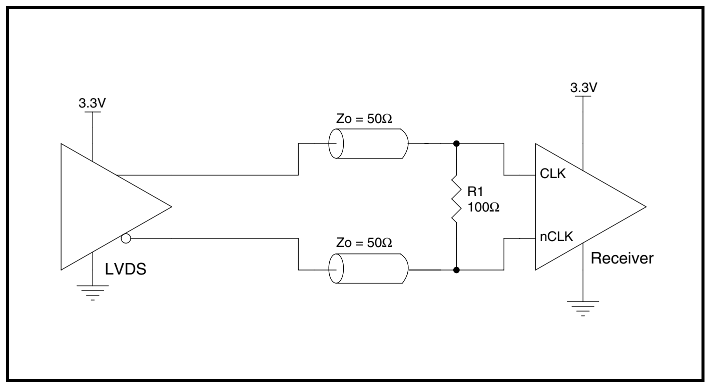


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

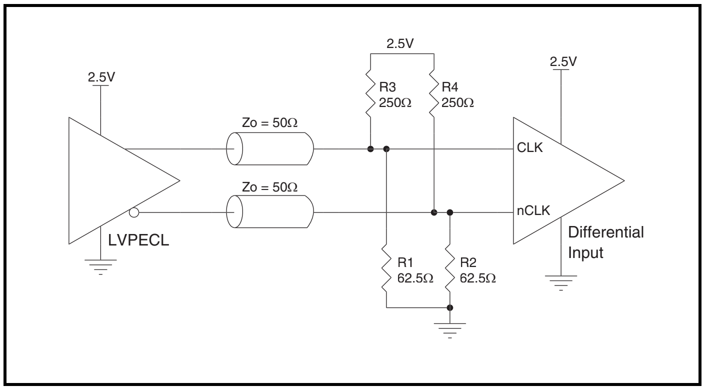


Figure 4A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

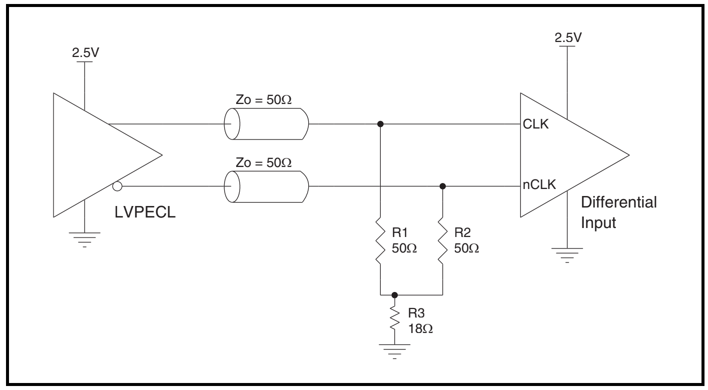


Figure 4B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

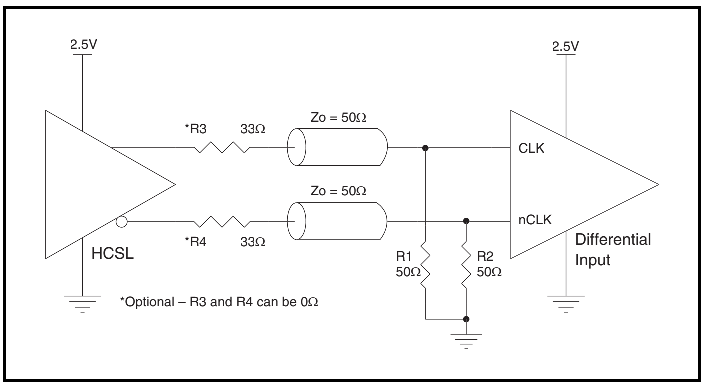


Figure 4C. CLK/nCLK Input Driven by a 2.5V HCSL Driver

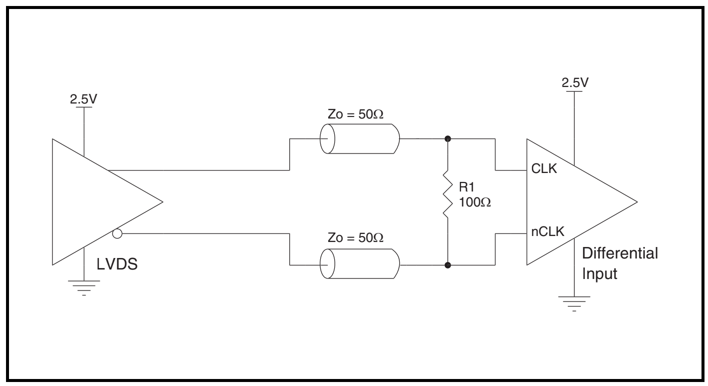


Figure 4D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 5A.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 5A can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

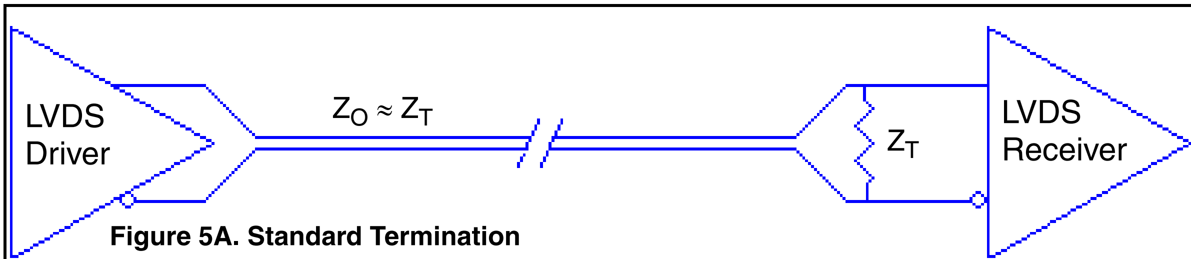


Figure 5A. Standard Termination

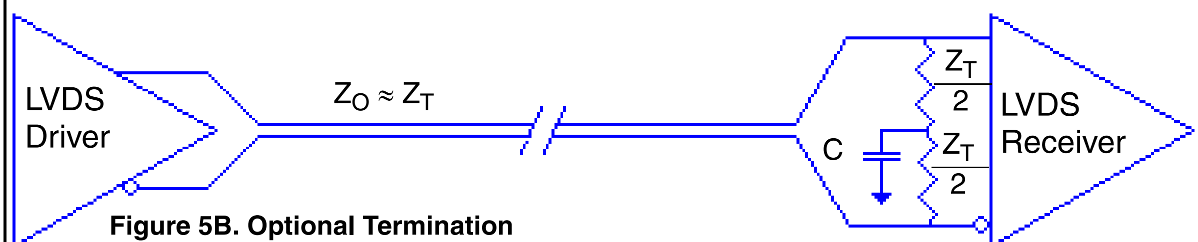


Figure 5B. Optional Termination

LVDS Driver Termination

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S1208I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S1208I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Max power dissipation occurs at -40°C.
Max I_{DD} at -40°C = 305mA

- $Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 305mA = **1056.825mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 6 below.

Max I_{DD} at 85°C = 287.8mA.
Max power at 85°C = 3.465V * 287.8mA = 997.227mW.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.997W * 33.1°C/W = 118°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 48 Lead TQFP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	27.2°C/W	25.7°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 48 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	27.2°C/W	25.7°C/W

Transistor Count

The transistor count for ICS854S1208I is: 9878

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead TQFP, E-Pad

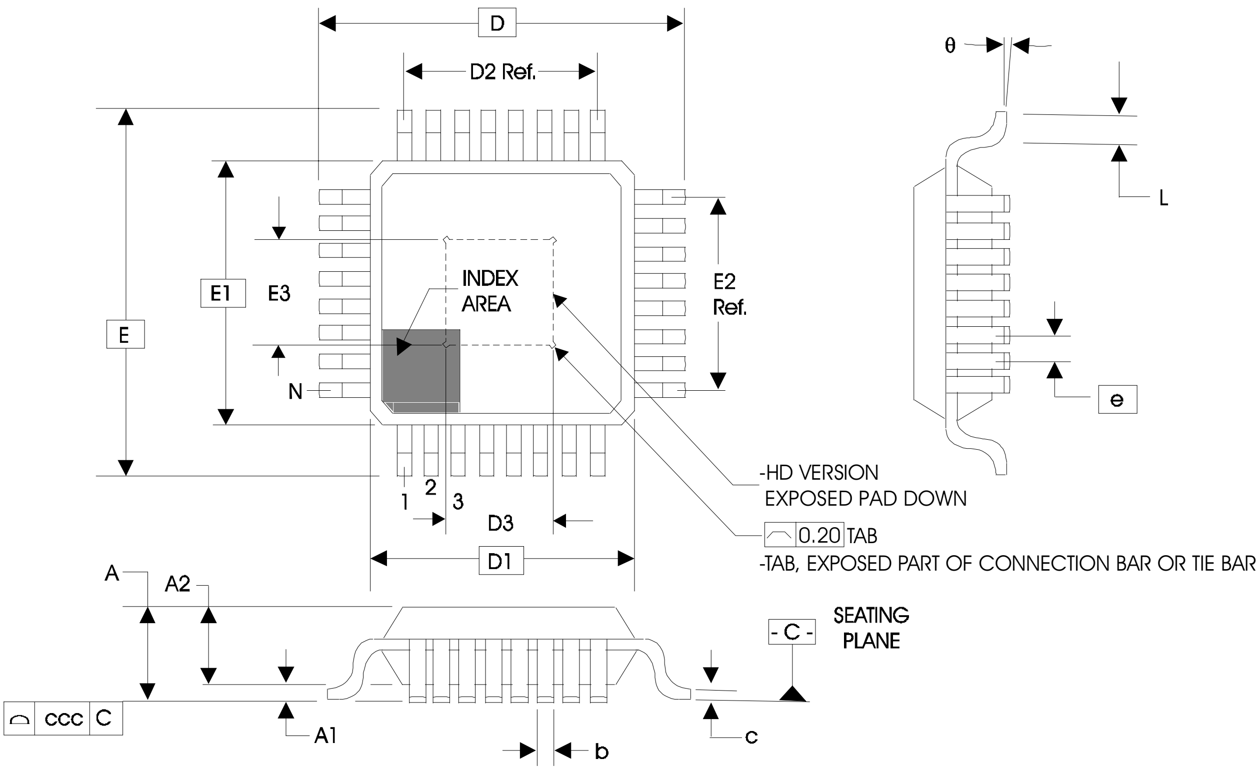


Table 8. Package Dimensions for 48 Lead TQFP, E-Pad

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
D3 & E3		3.5	
e		0.5 Basic	
L	0.45	0.60	0.75
ccc			0.08
θ	0°		7°

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S1208AYILF	ICS4S1208AIL	“Lead-Free” 48 Lead TQFP, E-Pad	Tray	-40°C to 85°C
854S1208AYILFT	ICS4S1208AIL	“Lead-Free” 48 Lead TQFP, E-Pad	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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