Low Skew, 1-to-6, Crystal Oscillator/LVCMOS-TO-3.3V, 2.5V LVPECL/LVCMOS Fanout Buffer

8536I-33

DATA SHEET

General Description

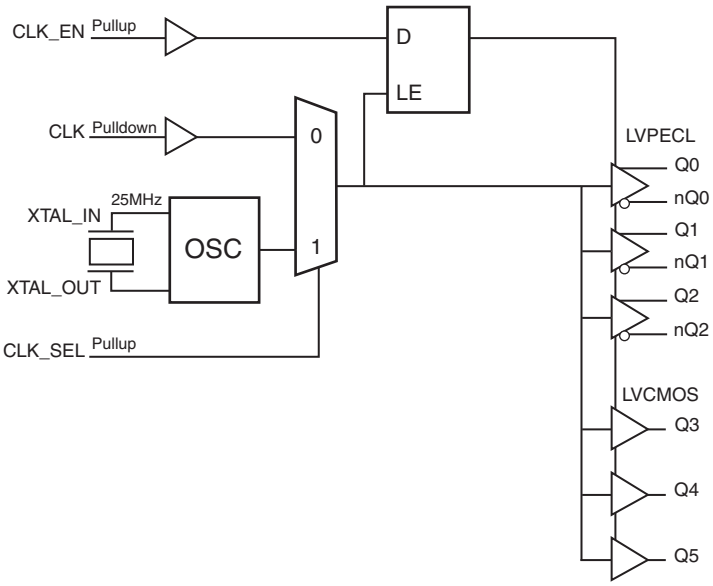
The 8536I-33 is a low skew, high performance 1-to-6 Crystal Oscillator/LVCMOS-to-3.3V, 2.5V LVPECL/LVCMOS fanout buffer. The 8536I-33 has selectable single ended clock or crystal inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8536I-33 ideal for those applications demanding well defined performance and repeatability.

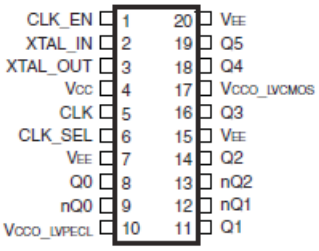
Features

- Three differential LVPECL outputs, and three single ended LVCMOS outputs
- Selectable LVCMOS/LVTTL CLK or crystal inputs
- CLK can accept the following input levels: LVCMOS, LVTTL
- Crystal frequency: 25MHz
- Maximum output frequency: 266MHz
- Output skew: 80ps (maximum)
- Part-to-part skew: 800ps (maximum)
- Propagation delay: 1.95ns (maximum)
- Additive phase jitter, RMS: 0.32ps (typical), LVPECL output
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8536I-33
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ0 output is forced high. LVCMOS / LVTTL interface levels.
2, 3	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
4	V_{CC}	Power		Positive supply pins.
5	CLK	Input	Pulldown	Single-ended clock input. LVCMOS / LVTTL interface levels.
6	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects XTAL inputs. When LOW, selects CLK input. LVCMOS / LVTTL interface levels.
7, 15, 20	V_{EE}	Power		Negative supply pin.
8, 9	Q0, nQ0	Output		Differential clock outputs. LVPECL interface levels.
10	V_{CCO_LVPECL}	Power		Output power supply mode for LVPECL clock outputs.
11, 12	Q1, nQ1	Output		Differential clock outputs. LVPECL interface levels.
13, 14	nQ2, Q2	Output		Differential clock outputs. LVPECL interface levels.
16, 18, 19	Q3, Q4, Q5	Output		Single ended clock outputs. LVCMOS / LVTTL interface levels.
17	V_{CCO_LVCMOS}	Power		Output power supply mode for LVCMOS / LVTTL clock outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance (per output)	Q3:Q5	V_{CC}, V_{CCO_LVCMOS} = 3.465V		8		pF
			V_{CC}, V_{CCO_LVCMOS} = 2.625V		5		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	Q3:Q5	V_{CC}, V_{CCO_LVCMOS} = 3.465V		15		Ω
		Q3:Q5	V_{CC}, V_{CCO_LVCMOS} = 2.625V		20		Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs		
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q2**	**nQ0:nQ2**	**Q3:Q5**
0	0	CLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW
0	1	XTAL_IN, XTAL_OUT	Disabled; LOW	Disabled; HIGH	Disabled; LOW
1	0	CLK	Enabled	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in *Figure* 1.
In the active mode, the state of the outputs are a function of the CLK input as described in Table 3B.

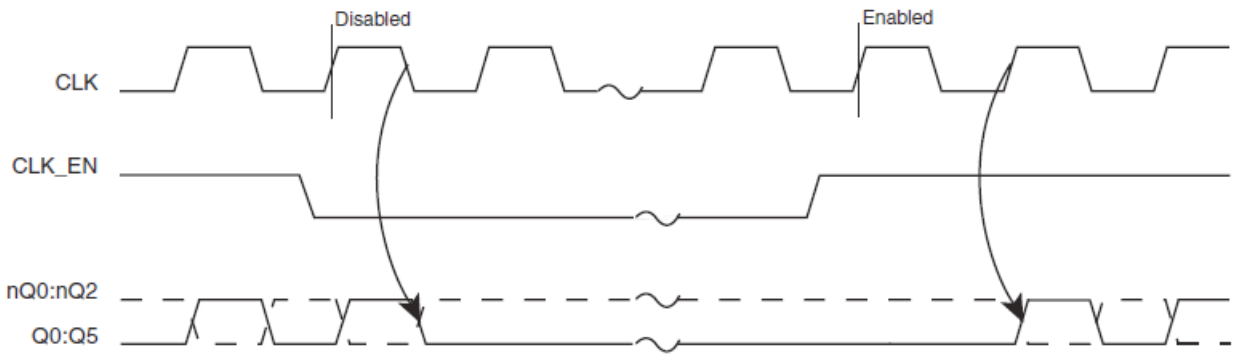


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs	Outputs		
CLK	**Q0:Q2**	**nQ0:nQ2**	**Q3:Q5**
0	LOW	HIGH	LOW
1	HIGH	LOW	HIGH

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I (LVCMOS)	-0.5V to V_{CC} + 0.5 V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_LVCMOS} + 0.5V
Inputs, V_I (LVPECL)	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	91.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVPECL} = V_{CCO\_LVCMOS} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCO_LVPECL}, V_{CCO_LVCMOS}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				80	mA
I_{CCO_LVPECL}	Power Supply Current				25	mA
I_{CCO_LVCMOS}	Power Supply Current				45	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVPECL} = V_{CCO\_LVCMOS} = 2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CCO_LVPECL}, V_{CCO_LVCMOS}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				80	mA
I_{CCO_LVPECL}	Power Supply Current				30	mA
I_{CCO_LVCMOS}	Power Supply Current				45	mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
V_{HYS}	Input Hysteresis	CLK_EN, CLK_SEL		100			mV
I_{IH}	Input High Current	CLK	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		CLK_EN, CLK_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		CLK_EN, CLK_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVCMOS} = 3.465V	2.6			V
			V_{CCO_LVCMOS} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVCMOS} = 3.465 or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVCMOS}/2. See Parameter Measurement Information Section. "LVCMOS Output Load Test circuit" diagrams.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = V_{CCO_LVPECL} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVPECL} - 1.4		V_{CCO_LVPECL} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVPECL} -2.0		V_{CCO_LVPECL} -1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVPECL} - 2V.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = V_{CCO_LVPECL} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVPECL} - 1.4		V_{CCO_LVPECL} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVPECL} -2.0		V_{CCO_LVPECL} -1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVPECL} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. LVPECL AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		1.2		1.95	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.35		ps
tsk(b)	Bank Skew; NOTE 2, 5				55	ps
tsk(o)	Output Skew; NOTE 3, 5				80	ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 5				800	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		46		54	%

All parameters measured at $f \leq 266$MHz unless noted otherwise.
NOTE 1: Measured from the $V_{CC}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the LVPECL output differential cross points.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the LVPECL output differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. LVPECL AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		1.3		2	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.32		ps
tsk(b)	Bank Skew; NOTE 2, 5				65	ps
tsk(o)	Output Skew; NOTE 3, 5				80	ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 5				425	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		800	ps
odc	Output Duty Cycle		46		54	%

All parameters measured at $f \leq 266$MHz unless noted otherwise.
NOTE 1: Measured from the $V_{CC}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the LVPECL output differential cross points.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the LVPECL output differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6C. LVCMOS AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		2.4		3.5	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.35		ps
tsk(b)	Bank Skew; NOTE 2, 5				65	ps
tsk(o)	Output Skew; NOTE 3, 5				80	ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 5		0.730		800	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	0.3		1.15	ns
odc	Output Duty Cycle		46		54	%

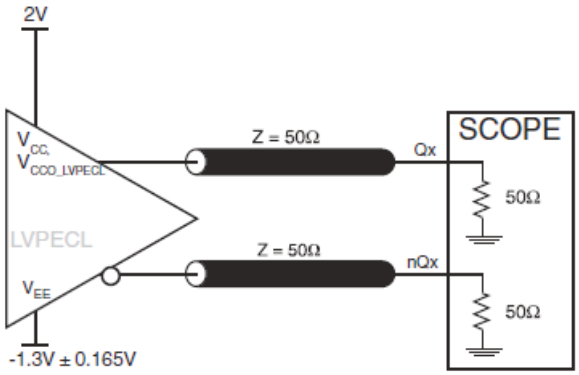
All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from the V_{CC}/2 of the input to V_{CCO_LVCMOS}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{CCO_LVCMOS}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{CCO_LVCMOS}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6D. LVCMOS AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS}$ = 2.5V±5%, T_A = -40°C TO 85°C

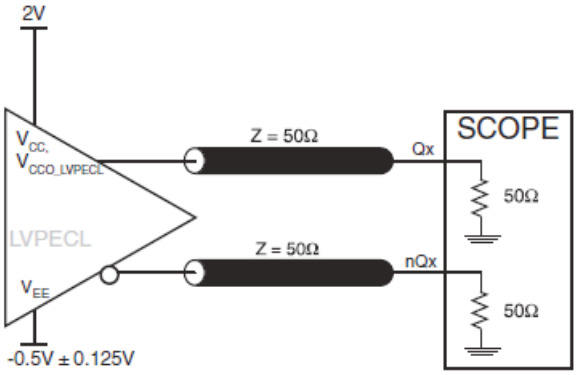
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		2.5		3.75	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.32		ps
tsk(b)	Bank Skew; NOTE 2, 5				75	ps
tsk(o)	Output Skew; NOTE 3, 5				80	ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 5				800	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	0.425		1.85	ns
odc	Output Duty Cycle		46		54	%

All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from the V_{CC}/2 of the input to V_{CCO_LVCMOS}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{CCO_LVCMOS}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{CCO_LVCMOS}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

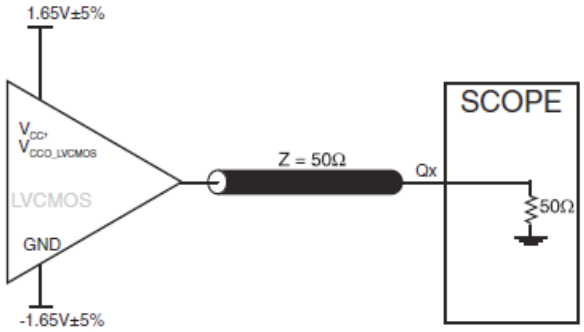
Parameter Measurement Information



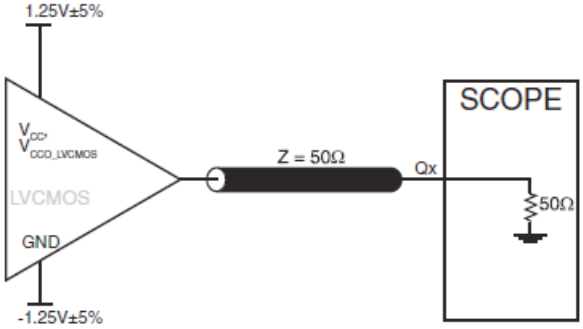
3.3V LVPECL Output Load AC Test Circuit



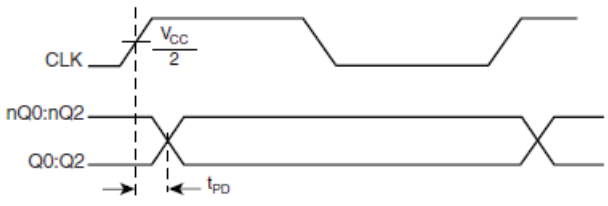
2.5V LVPECL Output Load AC Test Circuit



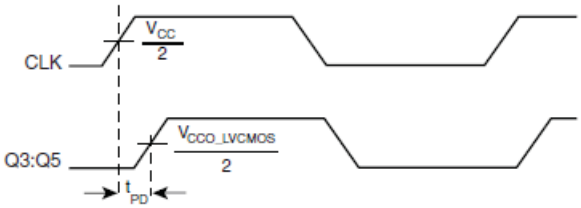
3.3V LVCMOS Output Load AC Test Circuit



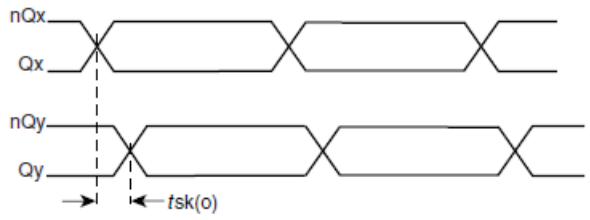
2.5V LVCMOS Output Load AC Test Circuit



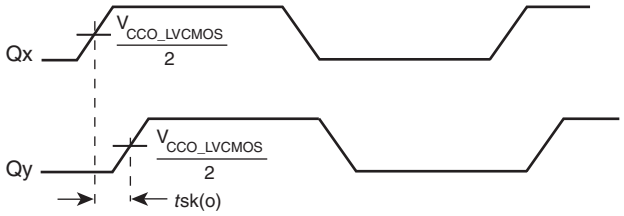
LVPECL Propagation Delay



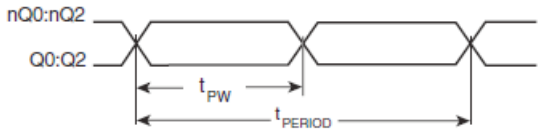
LVCMOS Propagation Delay



LVPECL Output Skew

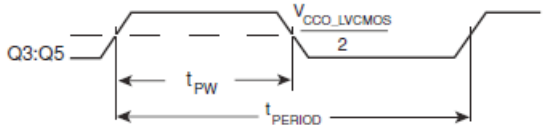


LVCMOS Output Skew



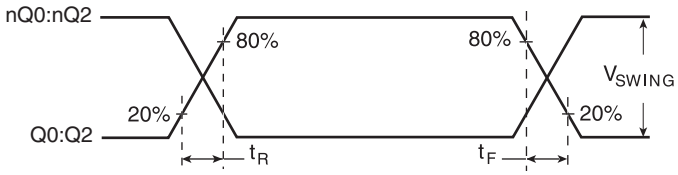
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVPECL Output Duty Cycle/Pulse Width/Period

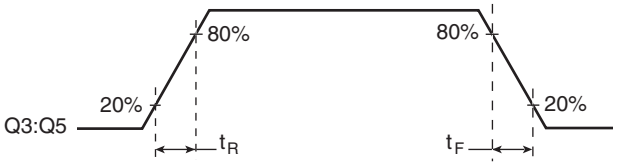


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

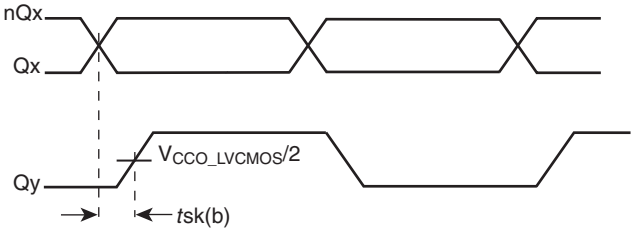
LVCMOS Output Duty Cycle/Pulse Width/Period



LVPECL Output Rise/Fall Time



LVCMOS Output Rise/Fall Time



Bank Skew

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 8536I-33 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters speci-fied in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

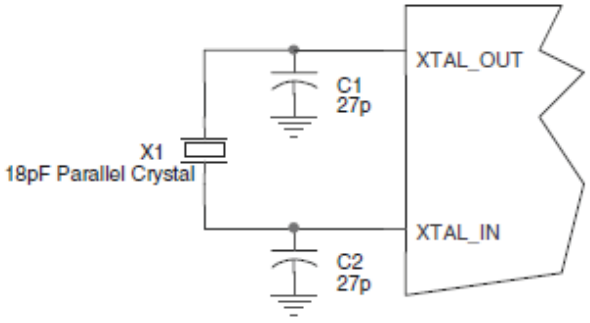


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

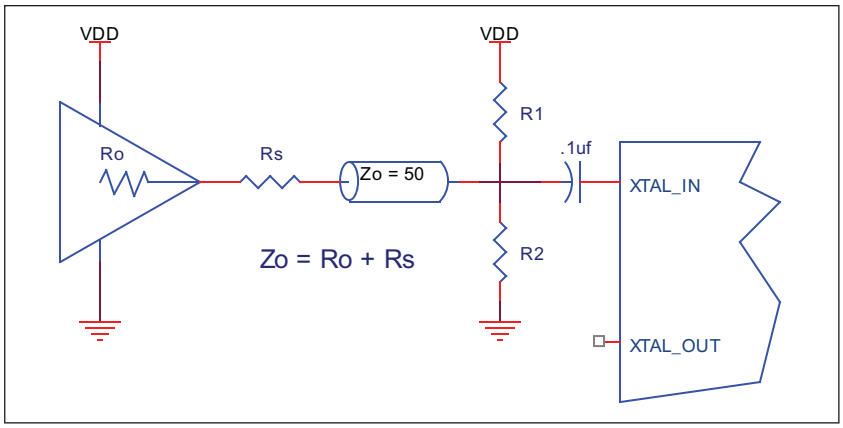


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

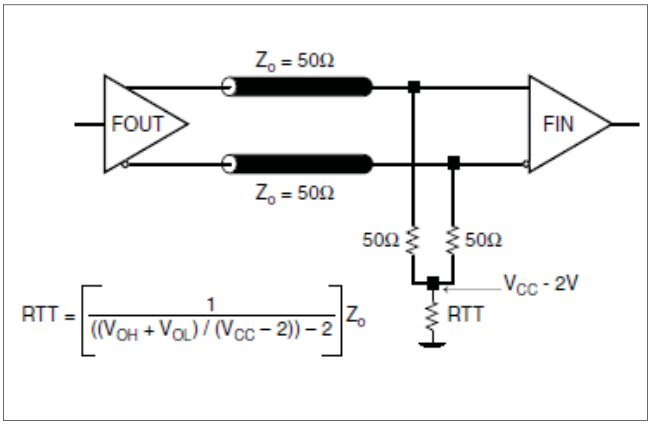


Figure 4A. LVPECL Output Termination

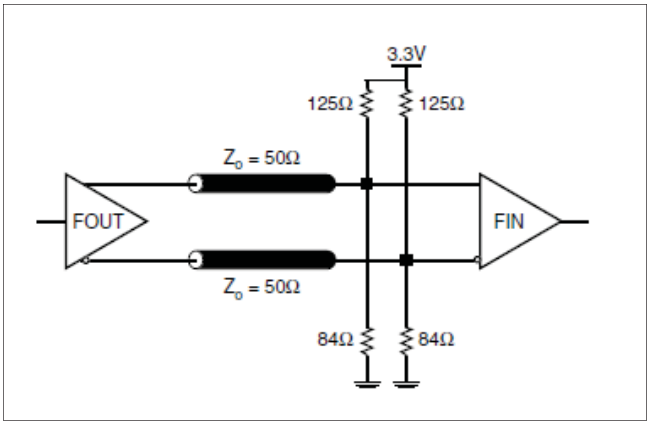


Figure 4B. LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{cc} – 2V. For V_{cco} = 2.5V, the V_{cco_lvcmos} – 2V is very close to _LVCMOSground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

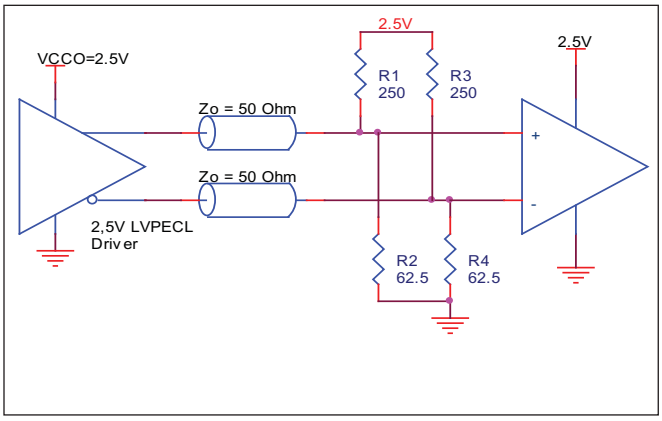


Figure 5A. 2.5V LVPECL Driver Termination Example

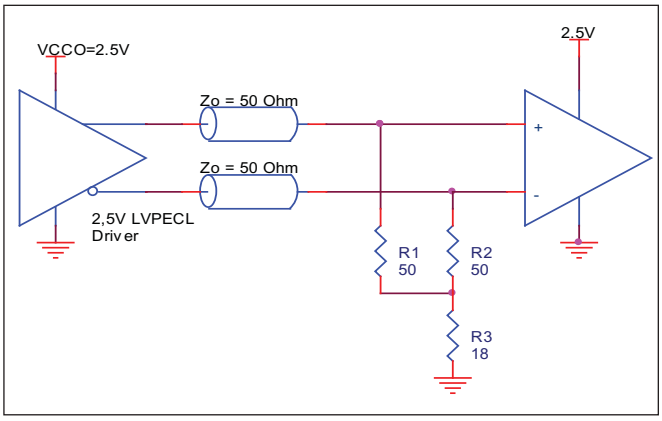


Figure 5B. 2.5V LVPECL Driver Termination Example

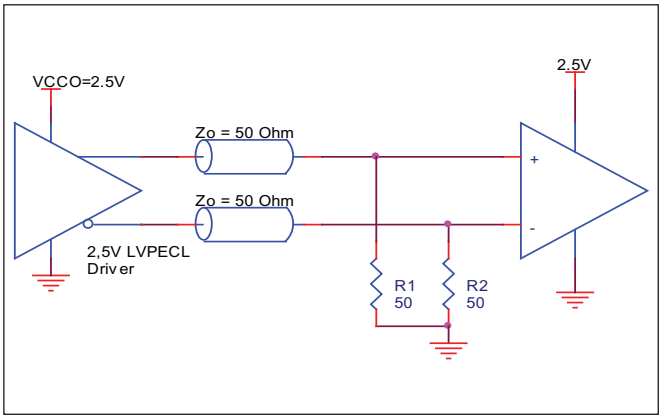


Figure 5C. 2.5V LVPECL Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8536I-33.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 8536I-33 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

Core and LVPECL Output Power Dissipation

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 80mA = **277.2mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30mW = **90mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{CCO_LVCMOS}/2

  Output Current I_{OUT} = V_{CCO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω] = **26.7mA**

- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 15Ω * (26.7mA)^2 = **10.7mW per output**

- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 10.7mW * 3 = **32.1mW**

Total Power Dissipation

- **Total Power**
  = Power (LVPECL) + Total Power (R_{OUT})
  = 277.2mW + 90mW + 32.1mW
  = 399.3mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.3993W * 91.1°C/W = 121.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

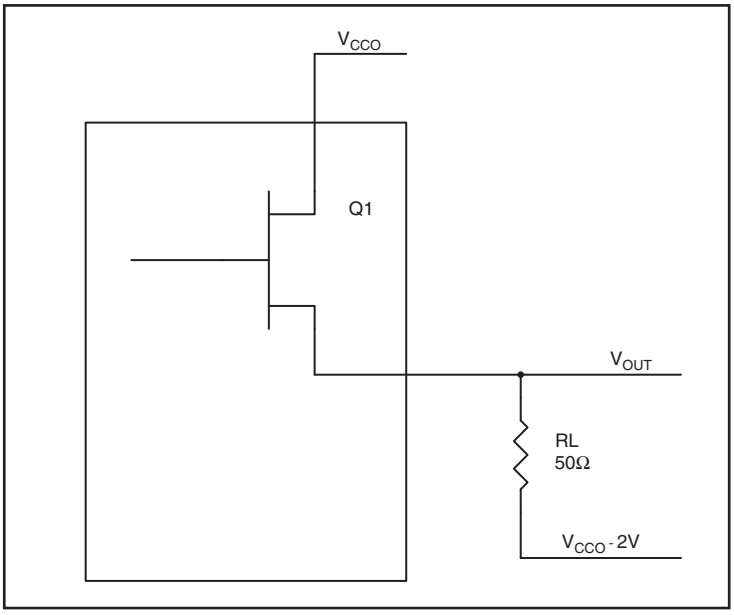


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 20 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

Transistor Count

The transistor count for 8536I-33 is: 550

Package Outline & Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

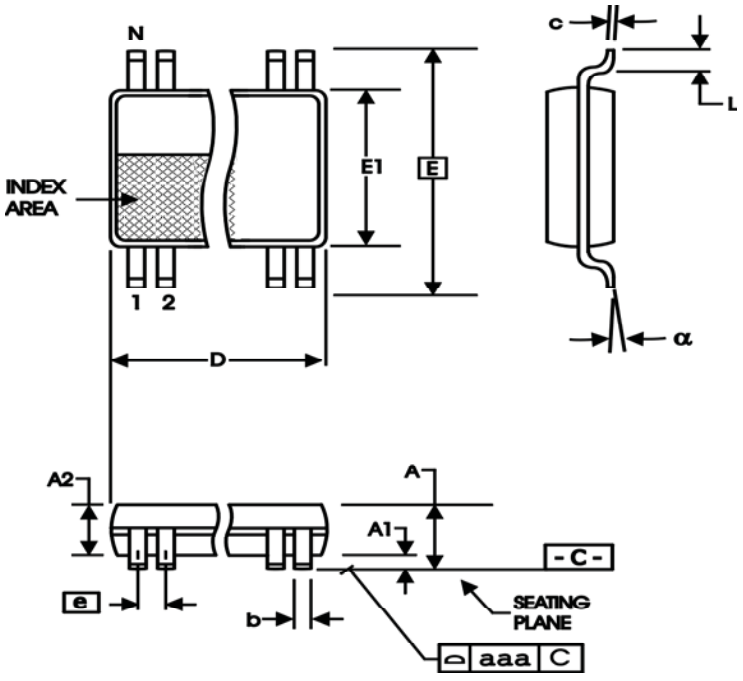


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8536CGI-33LF	ICS8536CI33L	20 lead “Lead-Free” TSSOP	tube	-40°C to 85°C
8536CGI-33LFT	ICS8536CI33L	20 lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T1	1 2	Pin Assignment - corrected pins 13 & 14. Pin Description Table - corrected pin 13 & 14.	6/25/08
B	T10	17	Ordering Information - removed leaded devices. Update data sheet format.	7/10/15

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