



FemtoClock® Crystal-to-3.3V LVPECL Clock Generator

ICS843031

DATA SHEET

GENERAL DESCRIPTION

The ICS843031 is a 1 Gigabit Ethernet Clock Generator. The ICS843031 can synthesize 1 Gigabit Ethernet, SONET, or Serial ATA reference clock frequencies with the appropriate choice of crystal and output divider. The ICS843031 has excellent phase jitter performance and is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

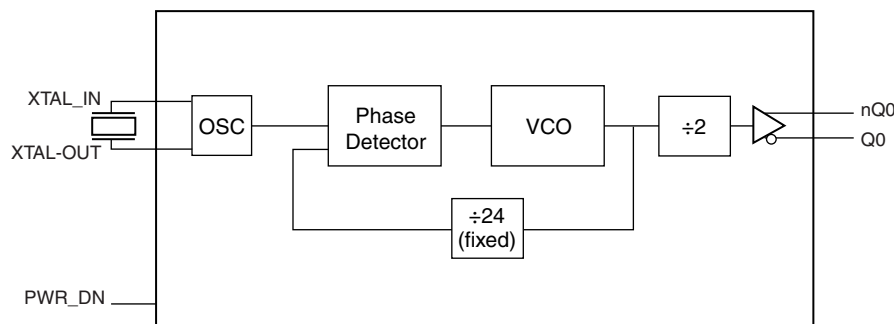
FEATURES

- One differential 3.3V LVPECL output
- Crystal oscillator interface designed for 18pF parallel resonant crystals
- Output frequency range: 290MHz - 350MHz
- VCO frequency range: 580MHz - 700MHz
- RMS phase jitter @312.5MHz (1.875MHz - 20MHz): 0.475ps (typical)
- RMS phase jitter @318.75MHz (1.875MHz - 20MHz): 0.475ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

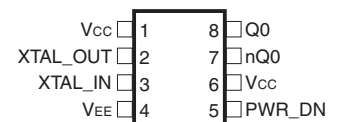
FREQUENCY TABLE

| Inputs | | M/N Ratio (Multiplier) | Output Frequency (MHz) |
|-------------------------|--|------------------------|------------------------|
| Crystal Frequency (MHz) | | | |
| 25.92 | | 12 | 311.04 |
| 26.04166 | | 12 | 312.5 |
| 26.5625 | | 12 | 318.75 |

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS843031

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|----------------------|--------|--------|--|
| 1, 6 | V _{CC} | Power | | Core supply pin. |
| 2, 3 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 4 | V _{EE} | Power | | Negative supply pin. |
| 5 | PWR_DN | Input | Pullup | Output state control input. High impedance when LOW (oscillator stops). LVCMOS/LVTTL interface levels. |
| 7, 8 | nQ0, Q0 | Output | | Differential clock outputs. LVPECL interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 101.7°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | PWR_DN = 1 | | | 105 | mA |
| | | PWR_DN = 0 | | | <1 | mA |

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | PWR_DN $V_{CC} = V_{IN} = 3.465V$ | | | 5 | μA |
| I_{IL} | Input Low Current | PWR_DN $V_{CC} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |

TABLE 3C. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50 Ω to $V_{CC} - 2V$.

TABLE 4. CRYSTAL CHARACTERISTICS

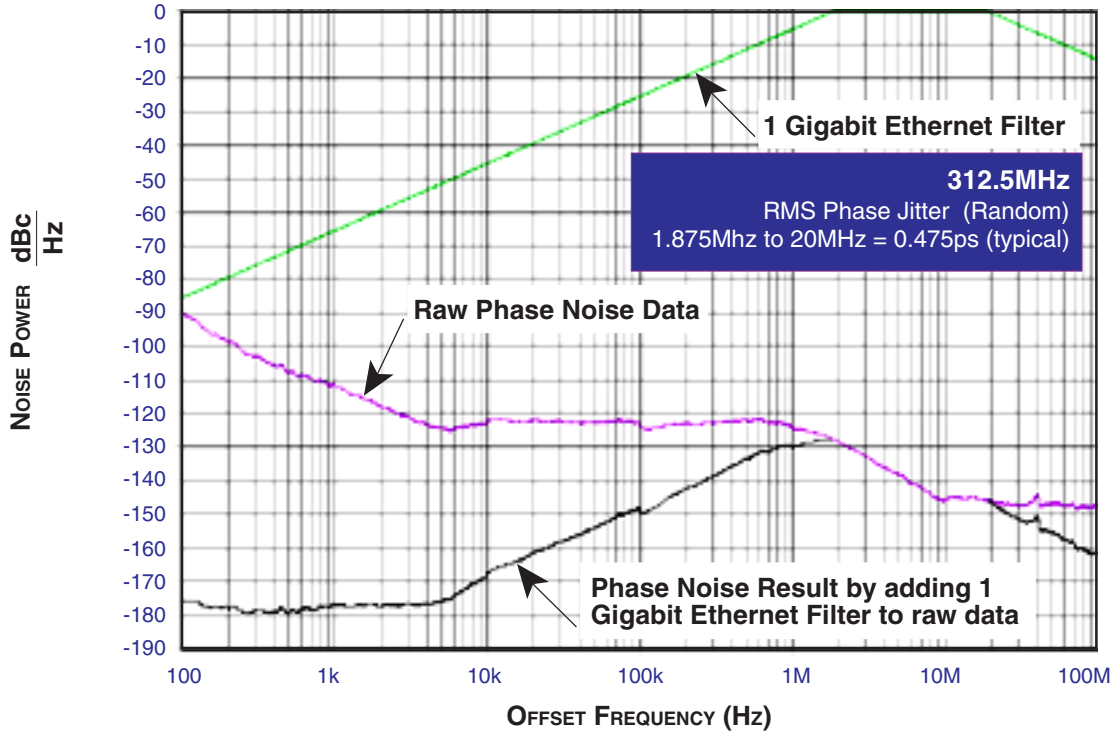
| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 12 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

TABLE 5. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

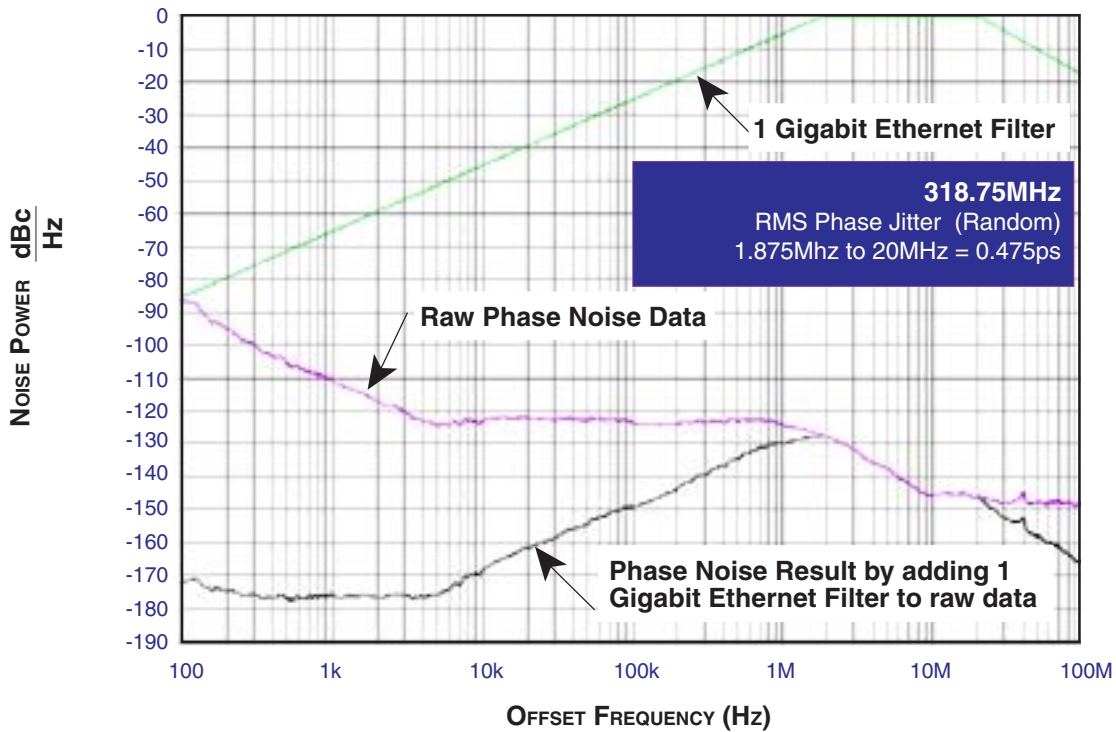
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | 290 | | 350 | MHz |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | 312.5MHz, Integration Range: 1.875MHz to 20MHz | | 0.475 | | ps |
| | | 318.75MHz, Integration Range: 1.875MHz to 20MHz | | 0.475 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 600 | ps |
| odc | Output Duty Cycle | | 46 | | 54 | % |

NOTE 1: Please refer to the Phase Noise Plot.

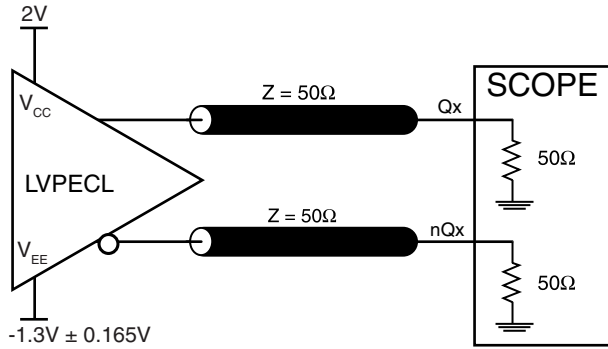
TYPICAL PHASE NOISE AT 312.5MHz



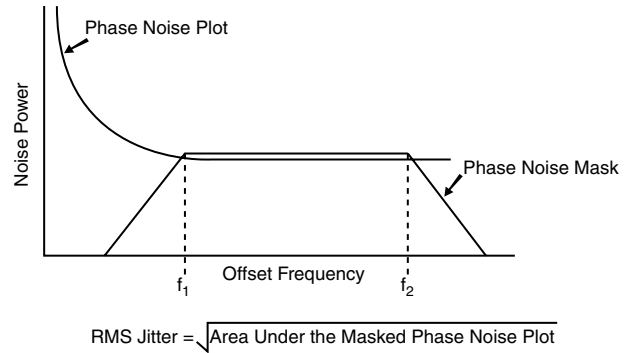
TYPICAL PHASE NOISE AT 318.75MHz



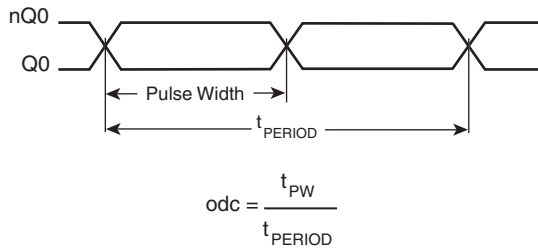
PARAMETER MEASUREMENT INFORMATION



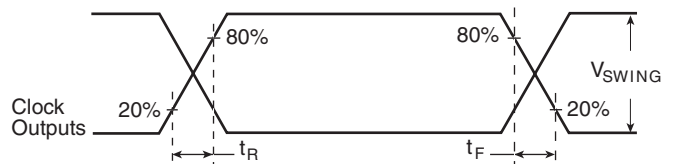
3.3V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

The ICS843031 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 26.04167MHz, 18pF

parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

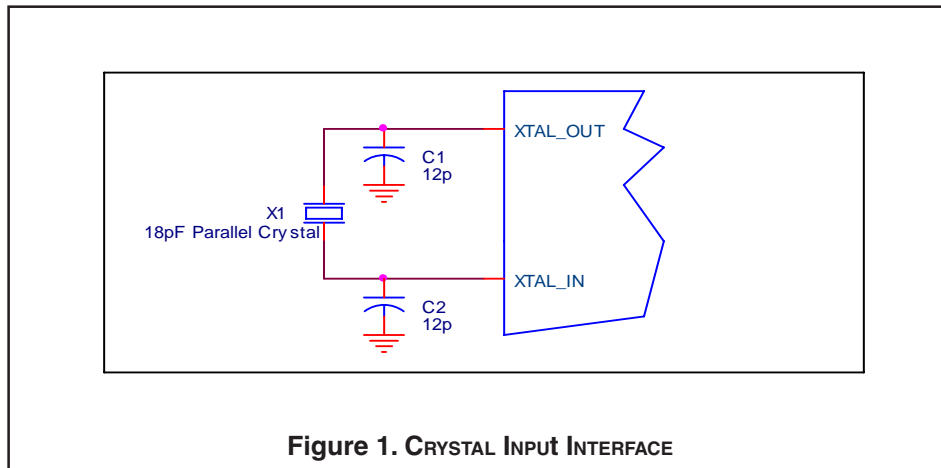


Figure 1. CRYSTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

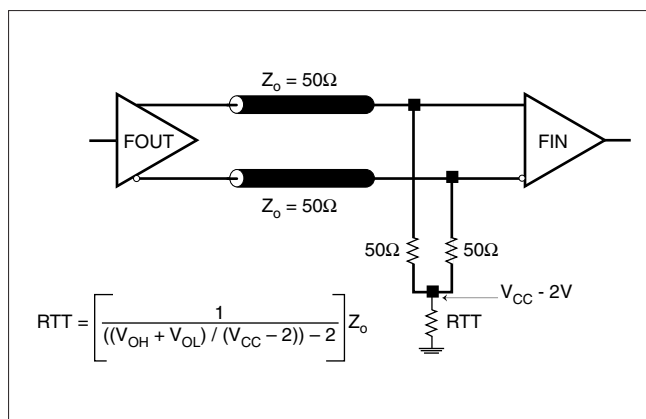


FIGURE 2A. LVPECL OUTPUT TERMININATION

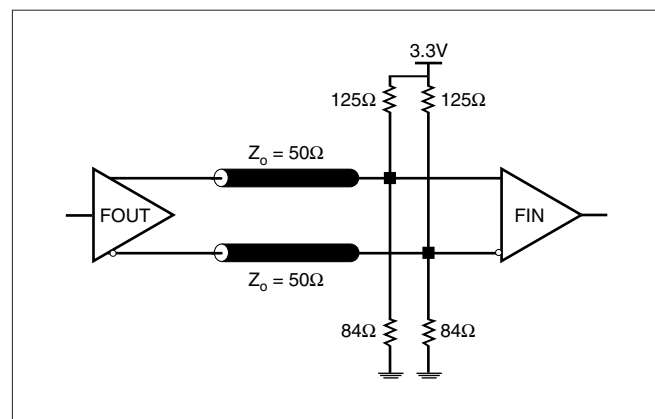


FIGURE 2B. LVPECL OUTPUT TERMININATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843051. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843051 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_TYP} = 3.465V * 105mA = 363.83mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 363.8mW + 30mW = 393.8mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.394W * 90.5^\circ\text{C/W} = 105.65^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

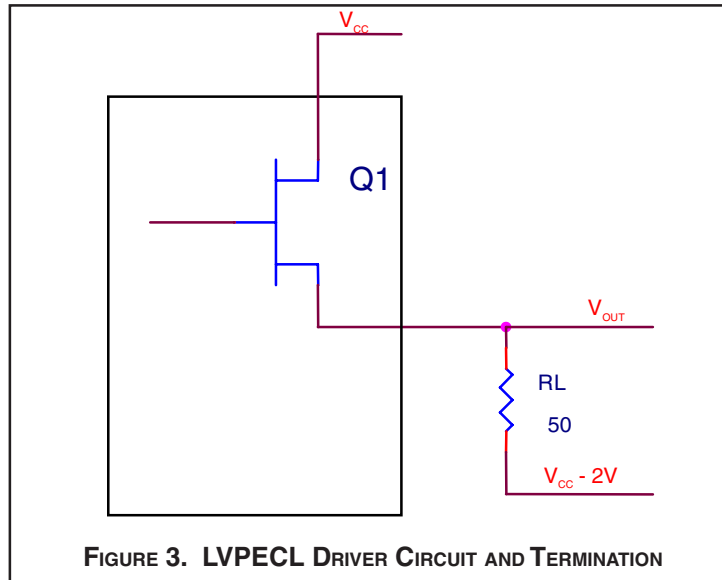
TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 4.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = \mathbf{30mW}$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

TRANSISTOR COUNT

The transistor count for ICS843031 is: 2360

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

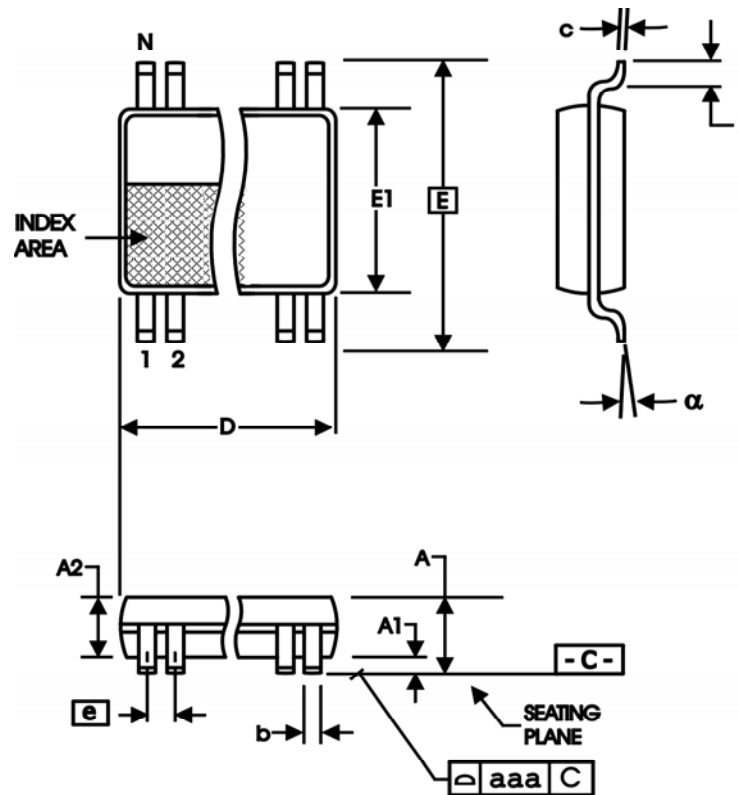


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|--------------------------|--------------------|-------------|
| 843031AG | 3031A | 8 lead TSSOP | tube | 0°C to 70°C |
| 843031AGT | 3031A | 8 lead TSSOP | 2500 tape & reel | 0°C to 70°C |
| 843031AGLF | 031AL | 8 lead "Lead-Free" TSSOP | tube | 0°C to 70°C |
| 843031AGLFT | 031AL | 8 lead "Lead-Free" TSSOP | 2500 tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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| REVISION HISTORY SHEET | | | | |
|------------------------|-------|---------|---|-----------|
| Rev | Table | Page | Description of Change | Date |
| A | T9 | 1 12 | Features Section - deleted duplicate phase jitter bullet. Ordering Information Table - deleted ICS prefix from part order number. Added LF marking. Updated header/footer with IDT logo. | 10/5/2011 |
| | | | | |
| | | | | |

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