SYNCHRONOUS ETHERNET WAN PLL and Clock Generation for IEEE-1588

Product Brief
IDT82V3399

FEATURES

HIGHLIGHTS

- Single chip PLL:
  - Features 0.5 mHz to 560 Hz bandwidth
  - Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
  - Exceeds GR-253-CORE (OC-192) and ITU-T G.813 (STM-64) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments
  - Provides clocks for 1 Gigabit and 10 Gigabit Ethernet applications
  - It supports clock generation for IEEE-1588 application

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, 4E, 4, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Provides SONET clocks with less than 1.3ps of RMS Phase Jitter (12 kHz - 20 MHz)
- Supports 1PPS input and output
- Employs PLL architecture to feature excellent jitter performance and minimize the number of the external components
- Integrates T0 DPLL and T4 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports programmable DPLL bandwidth (0.5 mHz to 560 Hz in 19 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Supports hitless reference switching to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Provides OUT1~OUT6 output clocks whose frequencies cover from 1 Hz (1PPS) to 644.53125 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, for CMOS outputs
  - Includes 25 MHz,125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, 322.265625 MHz and 644.53125 MHz for differential outputs
- Provides IN1~IN6 input clocks whose frequencies cover from 1 Hz (1PPS) to 625 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS inputs
  - Includes 25 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential inputs
- Internal DCO can be controlled by an external processor to be used for IEEE-1588 clock generation
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. It supports Free- Run, Locked and Holdover modes
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz, or 8 kHz frame sync input signal, and a 2 kHz or 8 kHz frame sync output signal
- Provides a 1PPS sync input signal and a 1PPS sync output signal
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262. ITU-T G.813 and ITU-T G.783 recommendations

OTHER FEATURES

- I2C and Serial microprocessor interface modes
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 72-pin QFN package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipment
- Synchronous Ethernet equipment
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and terabit IP switches / routers
- IP and ATM core switches and access equipment
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipment

DESCRIPTION

The IDT82V3399 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 3, 4E, 4, SMC, EEC-Option1, EEC-Option2 clocks in SONET / SDH / Synchronous Ethernet equipment, DWDM and Wireless base station.

The device supports several types of input clock sources: recovered clock from Synchronous Ethernet, STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

The device consists of T0 and T4 paths. The T0 path is a high quality and highly configurable path to provide system clock for node timing synchronization within a SONET / SDH / Synchronous Ethernet network. The T4 path is simpler and less configurable for equipment synchronization. The T4 path locks independently from the T0 path or locks to the T0 path.

An input clock is automatically or manually selected for T0 and T4 path. Both the T0 and T4 paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

There are 2 high performance APLLs that can be used for low jitter SONET and Ethernet Clocks

The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz in 19 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A highly stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports I2C and serial microprocessor interface modes.

In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure.

FUNCTIONAL BLOCK DIAGRAM

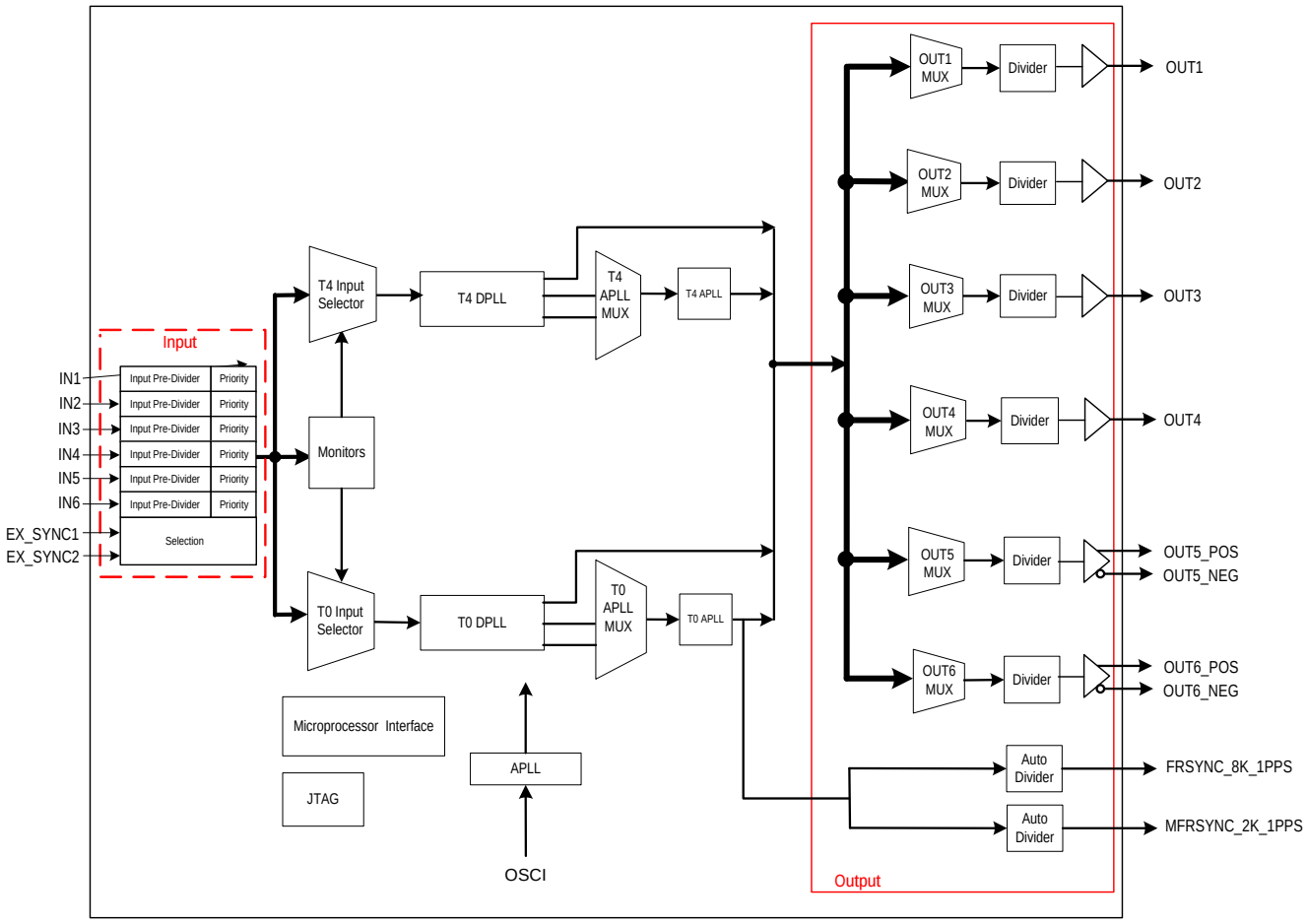
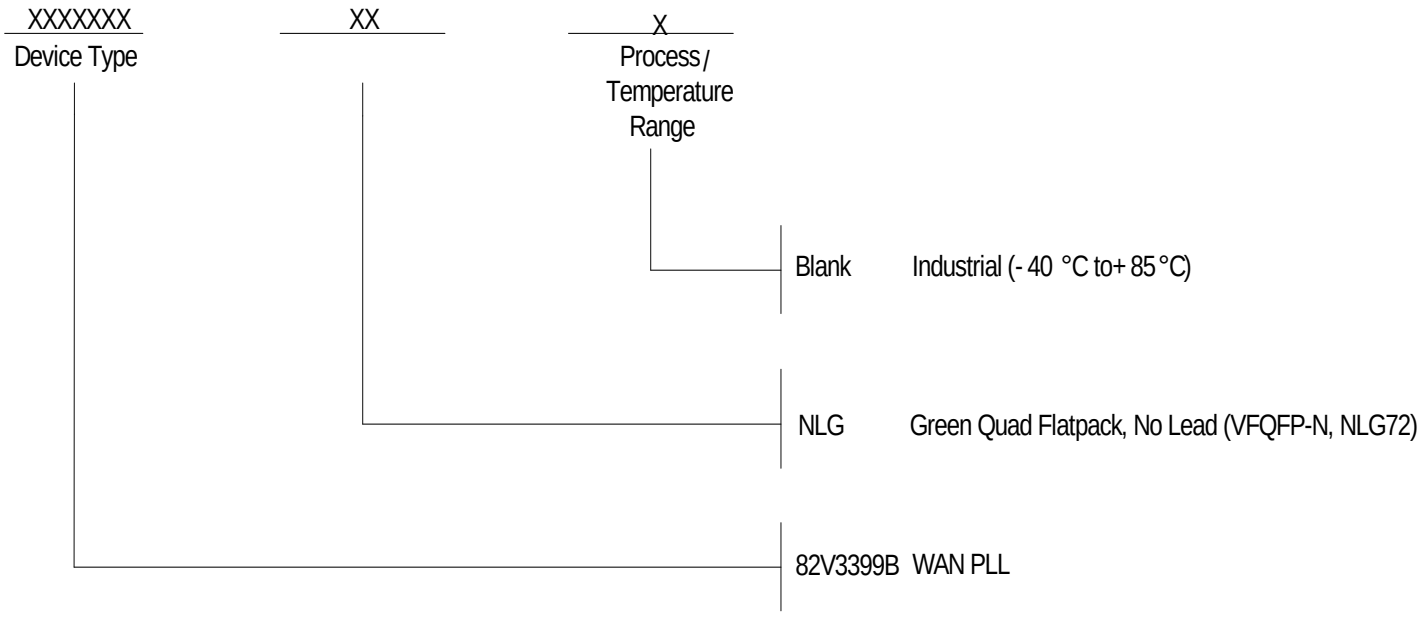


Figure 1. Functional Block Diagram

ORDERING INFORMATION



REVISION HISTORY

March 5, 2012: Initial Release

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