



## FAST CMOS 18-BIT REGISTER

**IDT74FCT162823AT/CT**

### FEATURES:

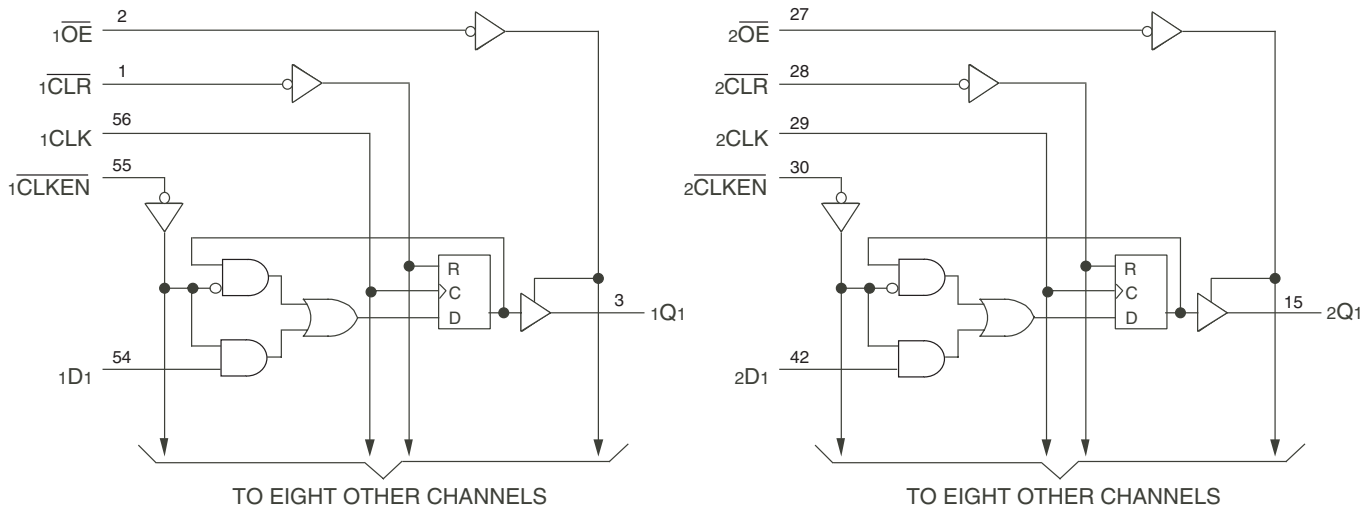
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- $V_{CC} = 5V \pm 10\%$
- Balanced Output Drivers of  $\pm 24mA$
- Reduced system switching noise
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.6V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

### DESCRIPTION:

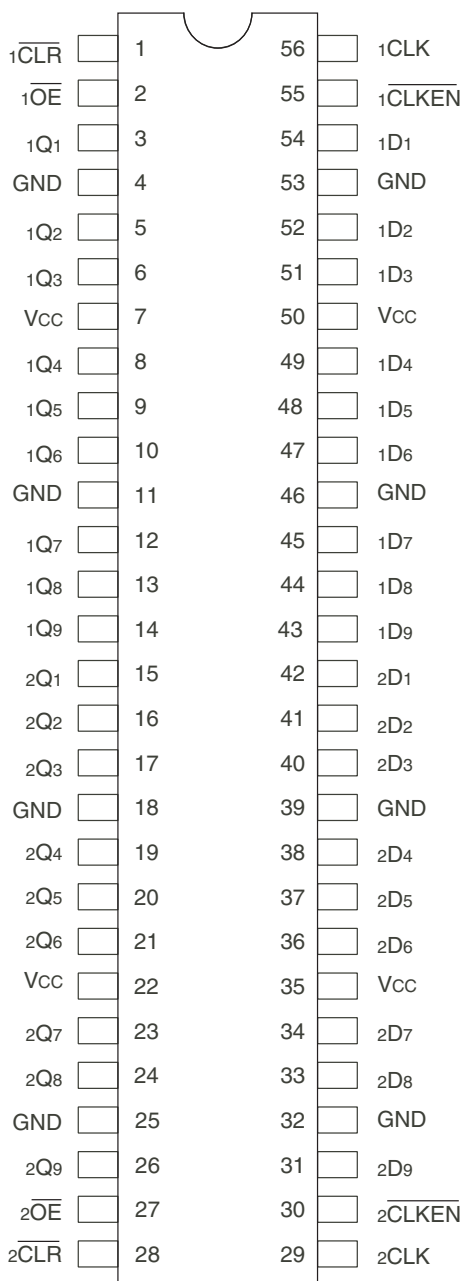
The FCT162823T 18-bit bus interface register is built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable ( $\overline{xCLKEN}$ ) and clear ( $\overline{xCLR}$ ) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162823T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The FCT162823T is a plug-in replacement for the FCT16823T and ABT16823T for on-board interface applications.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                           | Description                          | Max                          | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to 7                    | V    |
| V <sub>TERM</sub> <sup>(3)</sup> | Terminal Voltage with Respect to GND | -0.5 to V <sub>CC</sub> +0.5 | V    |
| T <sub>STG</sub>                 | Storage Temperature                  | -65 to +150                  | °C   |
| I <sub>OUT</sub>                 | DC Output Current                    | -60 to +120                  | mA   |

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Outputs and I/O terminals for FCT162XXX.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 3.5  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 3.5  | 8    | pF   |

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Pin Names                   | Description                            |
|-----------------------------|--|
| xD <sub>x</sub>             | Data Inputs                            |
| xCLK                        | Clock Inputs                           |
| x $\overline{\text{CLKEN}}$ | Clock Enable Inputs (Active LOW)       |
| x $\overline{\text{CLR}}$   | Asynchronous clear Inputs (Active LOW) |
| x $\overline{\text{OE}}$    | Output Enable Inputs (ActiveLOW)       |
| xO <sub>x</sub>             | 3-State Outputs                        |

## FUNCTION TABLE<sup>(1)</sup>

| Inputs                   |                           |                             |      |                 | Outputs          | Function |
|--------------------------|---------------------------|-----------------------------|------|-----------------|------------------|----------|
| x $\overline{\text{OE}}$ | x $\overline{\text{CLR}}$ | x $\overline{\text{CLKEN}}$ | xCLK | xD <sub>x</sub> | xQ <sub>x</sub>  |          |
| H                        | X                         | X                           | X    | X               | Z                | High Z   |
| L                        | L                         | X                           | X    | X               | L                | Clear    |
| L                        | H                         | H                           | X    | X               | Q <sup>(2)</sup> | Hold     |
| H                        | H                         | L                           | ↑    | L               | Z                | Load     |
| H                        | H                         | L                           | ↑    | H               | Z                |          |
| L                        | H                         | L                           | ↑    | L               | L                |          |
| L                        | H                         | L                           | ↑    | H               | H                |          |

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance
- Output level before indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol    | Parameter   | Test Conditions <sup>(1)</sup>                 |                     | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|---|--|---------------------|------|---------------------|---------|---------------|
| $V_{IH}$  | Input HIGH Level  | Guaranteed Logic HIGH Level                    |                     | 2    | —                   | —       | V             |
| $V_{IL}$  | Input LOW Level   | Guaranteed Logic LOW Level                     |                     | —    | —                   | 0.8     | V             |
| $I_{IH}$  | Input HIGH Current (Input pins) <sup>(4)</sup>                        | $V_{CC} = \text{Max.}$                         | $V_i = V_{CC}$      | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
|           | Input HIGH Current (I/O pins) <sup>(4)</sup>                          |  | $V_i = \text{GND}$  | —    | —                   | $\pm 1$ |               |
| $I_{IL}$  | Input LOW Current (Input pins) <sup>(4)</sup>                         |  | $V_o = 2.7\text{V}$ | —    | —                   | $\pm 1$ |               |
|           | Input LOW Current (I/O pins) <sup>(4)</sup>                           |  | $V_o = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $I_{OZH}$ | High Impedance Output Current<br>(3-State Output pins) <sup>(4)</sup> | $V_{CC} = \text{Max.}$                         | $V_o = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZL}$ |   |  | $V_o = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $V_{IK}$  | Clamp Diode Voltage   | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$  |                     | —    | -0.7                | -1.2    | V             |
| $I_{OS}$  | Short Circuit Current   | $V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$ |                     | -80  | -140                | -250    | mA            |
| $V_H$     | Input Hysteresis  | —  |                     | —    | 100                 | —       | mV            |
| $I_{CCL}$ | Quiescent Power Supply Current  | $V_{CC} = \text{Max}$                          |                     | —    | 5                   | 500     | $\mu\text{A}$ |
| $I_{CCH}$ |   | $V_{IN} = \text{GND or } V_{CC}$               |                     |      |                     |         |               |
| $I_{CCZ}$ |   |  |                     |      |                     |         |               |

## OUTPUT DRIVE CHARACTERISTICS

| Symbol    | Parameter           | Test Conditions <sup>(1)</sup>  |                         | Min. | Typ. <sup>(2)</sup> | Max. | Unit |
|-----------|---------------------|---|-------------------------|------|---------------------|------|------|
| $I_{ODL}$ | Output LOW Current  | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$ |                         | 60   | 115                 | 200  | mA   |
| $I_{ODH}$ | Output HIGH Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$ |                         | -60  | -115                | -200 | mA   |
| $V_{OH}$  | Output HIGH Voltage | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$                    | $I_{OH} = -24\text{mA}$ | 2.4  | 3.3                 | —    | V    |
| $V_{OL}$  | Output LOW Voltage  | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$                    | $I_{OL} = 24\text{mA}$  | —    | 0.3                 | 0.55 | V    |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter   | Test Conditions <sup>(1)</sup>   | Min.                                       | Typ. <sup>(2)</sup> | Max. | Unit                            |    |
|-----------------|---|--|--|---------------------|------|---------------------------------|----|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC} = \text{Max.}$<br>$V_{IN} = 3.4V^{(3)}$  | —  | 0.5                 | 1.5  | mA                              |    |
| $I_{CCD}$       | Dynamic Power Supply Current <sup>(4)</sup>       | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$\overline{xOE} = \overline{xCLKEN} = \text{GND}$<br>One Input Toggling<br>50% Duty Cycle  | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —                   | 75   | 120<br>$\mu\text{A}/\text{MHz}$ |    |
| $I_C$           | Total Power Supply Current <sup>(6)</sup>         | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{xOE} = \overline{xCLKEN} = \text{GND}$<br>at $f_i = 5\text{MHz}$<br>50% Duty Cycle<br>One Bit Toggling         | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —                   | 0.8  | 1.7                             | mA |
|                 |   |  | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —                   | 1.3  | 3.2                             |    |
|                 |   | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{xOE} = \overline{xCLKEN} = \text{GND}$<br>at $f_i = 2.5\text{MHz}$<br>50% Duty Cycle<br>Eighteen Bits Toggling | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —                   | 4.2  | 7.1 <sup>(5)</sup>              |    |
|                 |   |  | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —                   | 9.2  | 22.1 <sup>(5)</sup>             |    |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

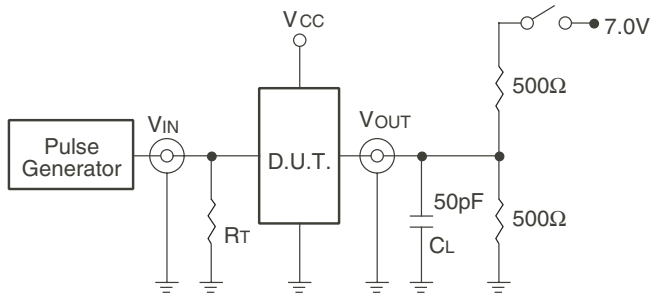
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol                               | Parameter                               | Condition <sup>(1)</sup>               | FCT162823AT         |      | FCT162823CT         |      | Unit |
|--------------------------------------|---|--|---------------------|------|---------------------|------|------|
|                                      |   |  | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>xCLKx to xOx       | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 10   | 1.5                 | 4.7  | ns   |
|                                      |   | CL = 300pF <sup>(4)</sup><br>RL = 500Ω | 1.5                 | 20   | 1.5                 | 8    |      |
| t <sub>PHL</sub>                     | Propagation Delay<br>xCLR to xOx        | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 14   | 1.5                 | 4.7  | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>xOE to xOx        | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 12   | 1.5                 | 4.4  | ns   |
|                                      |   | CL = 300pF <sup>(4)</sup><br>RL = 500Ω | 1.5                 | 23   | 1.5                 | 9    |      |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>xOE to xOx       | CL = 50pF <sup>(4)</sup><br>RL = 500Ω  | 1.5                 | 7    | 1.5                 | 3.6  | ns   |
|                                      |   | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 8    | 1.5                 | 3.6  |      |
| t <sub>SU</sub>                      | Set-up Time HIGH or LOW xDx to xCLK     | CL = 50pF<br>RL = 500Ω                 | 3                   | —    | 1.5                 | —    | ns   |
| t <sub>H</sub>                       | Hold Time HIGH or LOW, xDx to xCLK      |  | 1.5                 | —    | 0                   | —    | ns   |
| t <sub>SU</sub>                      | Set-up Time HIGH or LOW, xCLKEN to xCLK |  | 3                   | —    | 2.5                 | —    | ns   |
| t <sub>H</sub>                       | Hold Time HIGH or LOW, xCLKEN to xCLK   |  | 0                   | —    | 0                   | —    | ns   |
| t <sub>w</sub>                       | xCLK Pulse Width HIGH or LOW            |  | 6                   | —    | 3                   | —    | ns   |
| t <sub>w</sub>                       | xCLR Pulse Width LOW                    |  | 6                   | —    | 3                   | —    | ns   |
| t <sub>REM</sub>                     | Recovery Time, xCLR to xCLK             |  | 6                   | —    | 3                   | —    | ns   |
| t <sub>SK(o)</sub>                   | Output Skew <sup>(3)</sup>              |  | —                   | 0.5  | —                   | 0.5  | ns   |

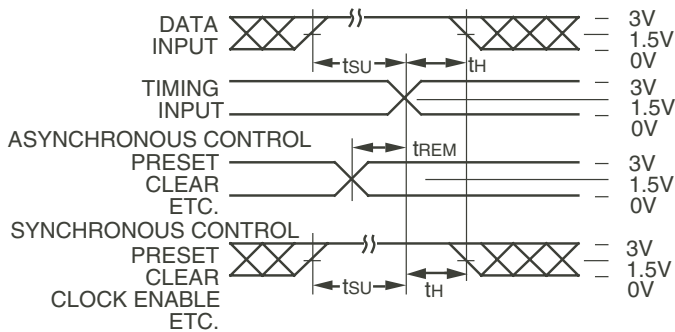
### NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This condition is guaranteed but not tested.

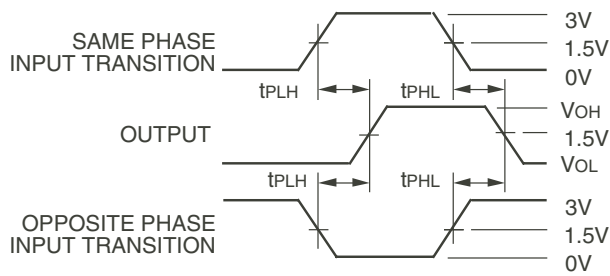
## TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



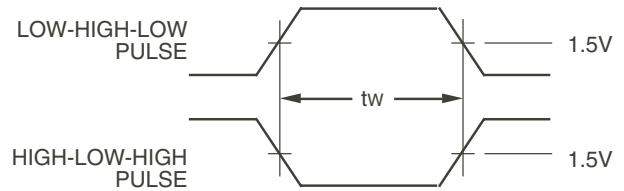
Propagation Delay

## SWITCH POSITION

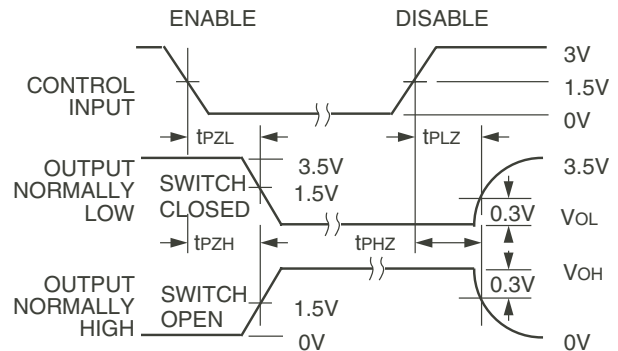
| Test                                    | Switch |
|---|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

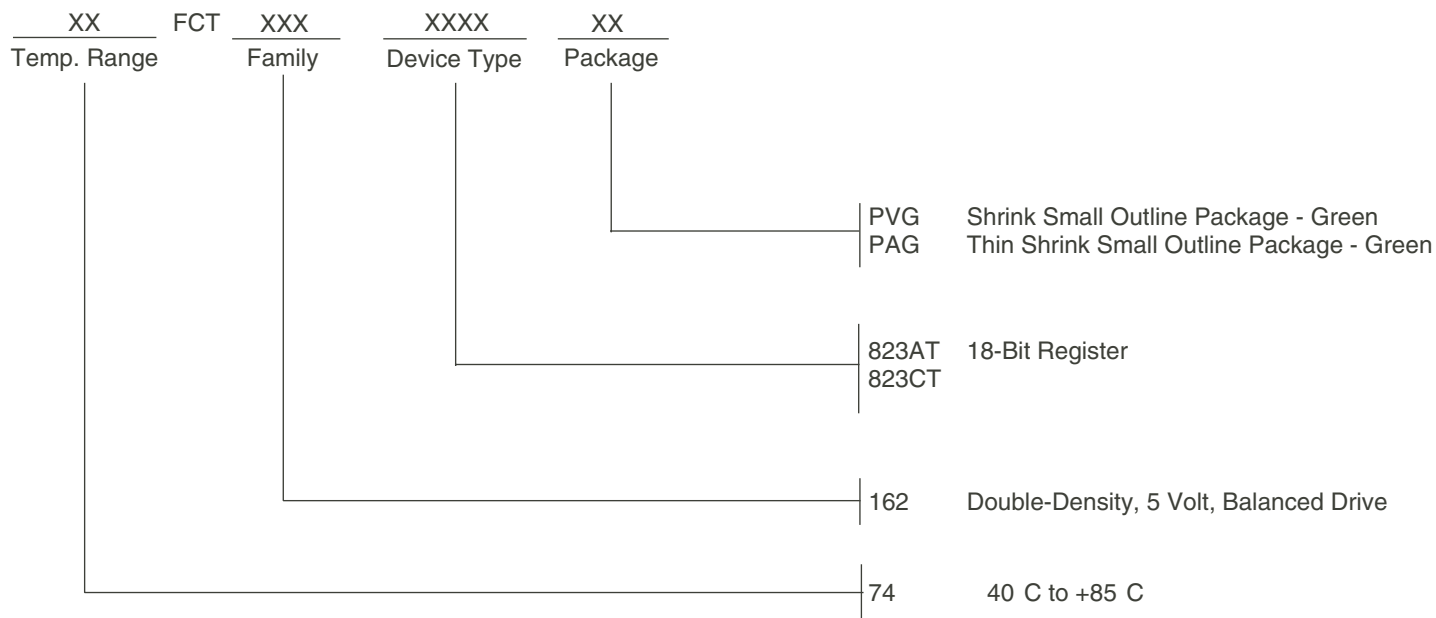


Enable and Disable Times

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_r \leq$  2.5ns;  $t_f \leq$  2.5ns.

## ORDERING INFORMATION



## Datasheet Document History

09/06/09 Pg. 7 Updated the ordering information by removing the "IDT" notation and non RoHS part.



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