

Description

The 5P49V6968 is a programmable clock generator that is intended for high-performance consumer, networking, industrial, computing, and data communications applications. This is IDT's sixth generation of programmable clock technology (VersaClock 6E).

The 5P49V6968 generates the frequencies from a single reference clock, which can originate from one of the two redundant clock inputs. A glitchless manual switchover function allows one of the redundant clocks to be selected during normal operation.

Two select pins allow up to four different configurations to be programmed, and can be used for different operating modes.

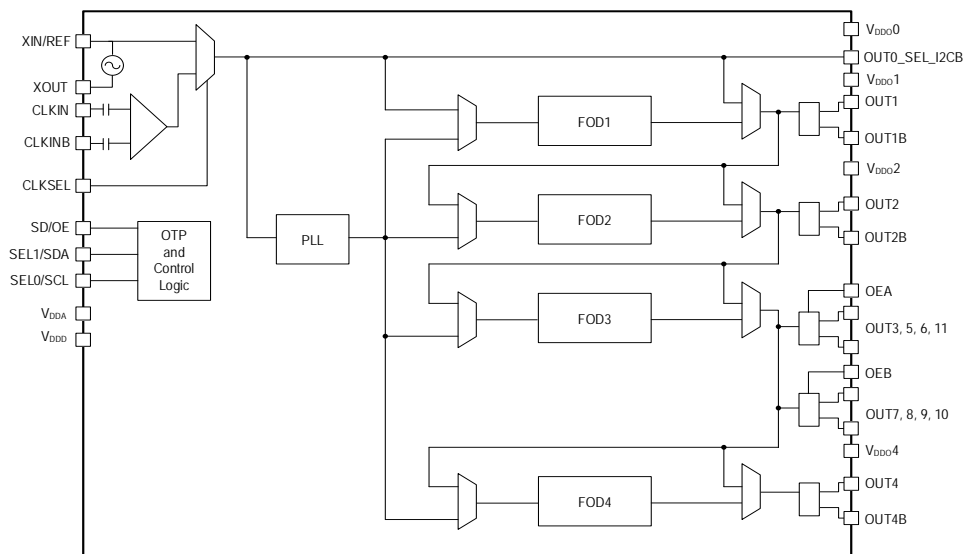
Typical Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0/4.0
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- Datacenter

Features

- Flexible 1.8V, 2.5V, and 3.3V power rails
- High-performance, low phase noise PLL, < 0.5ps RMS typical phase jitter on outputs
- Four banks of internal OTP memory
 - In-system or factory programmable
- I²C serial programming interface
 - 0xD0 or 0xD4 I²C address options allow multiple devices to be configured in a same system
- Reference LVCMOS output clock
- Three universal configurable outputs (OUT1, 2, 4):
 - Differential (LVPECL, LVDS, or HCSL) 1kHz to 350MHz
 - Two single-ended (in-phase or 180 degrees out of phase) 1kHz to 200MHz
 - I/O VDDs can be mixed and matched, supporting 1.8V (LVDS and LVCMOS), 2.5V, or 3.3V
 - Independent spread spectrum on each output pair
- Eight additional LPHCSL outputs (OUT 3, 5–11)
 - 1.8V low power supply
 - 1kHz to 200MHz
- Programmable output enable or power-down mode
- Redundant clock inputs with manual switchover
- Available in 6 × 6 mm 48-VFQFPN package
- -40° to +85°C industrial temperature operation

Block Diagram

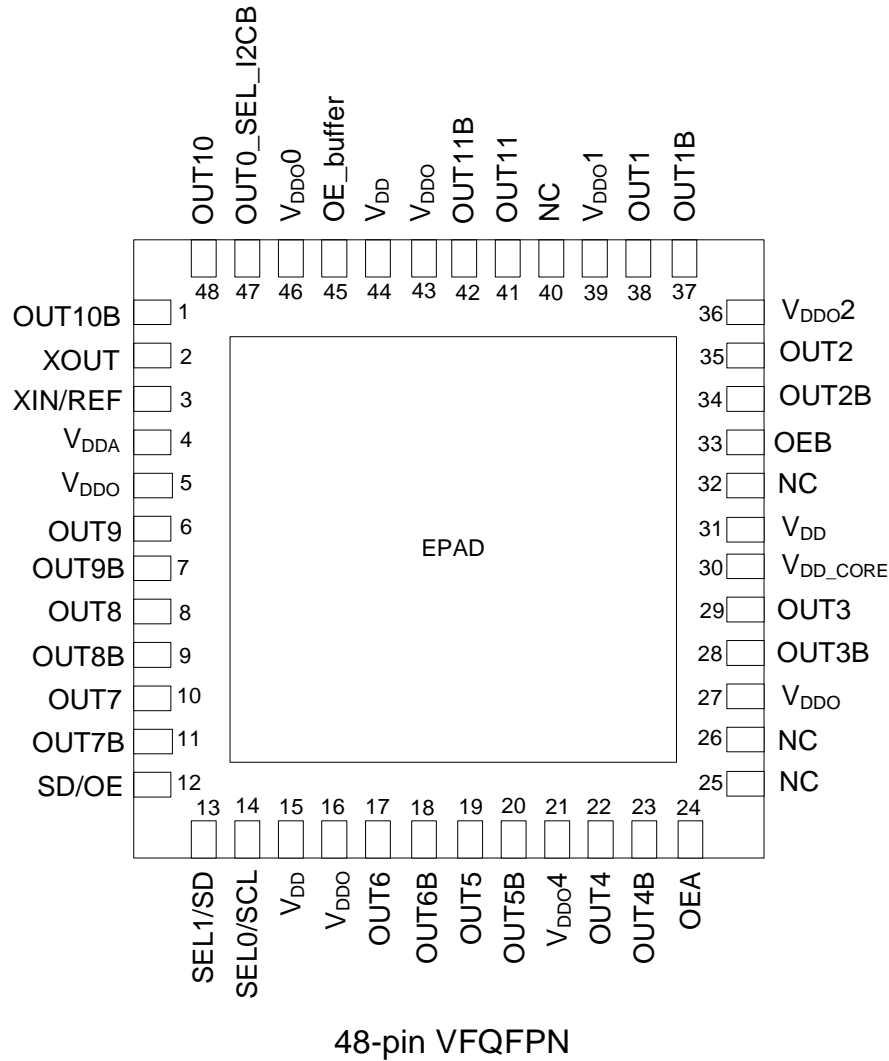


Contents

1.	Pin Assignments.....	3
2.	Pin Descriptions.....	3
3.	Absolute Maximum Ratings.....	6
4.	Thermal Characteristics.....	6
5.	Recommended Operating Conditions	6
6.	Electrical Characteristics	7
7.	Test Loads.....	14
8.	Jitter Performance Characteristics	15
9.	PCI Express Jitter Performance and Specification.....	16
10.	Features and Functional Blocks	17
10.1	Device Startup and Power-on-Reset.....	17
10.2	Reference Clock and Selection.....	18
10.3	Manual Switchover.....	18
10.4	Internal Crystal Oscillator (XIN/REF)	19
10.4.1	Choosing Crystals.....	19
10.4.2	Tuning the Crystal Load Capacitor.....	19
10.5	Programmable Loop Filter.....	20
10.6	Fractional Output Dividers (FOD).....	20
10.6.1	Individual Spread Spectrum Modulation	20
10.6.2	Bypass Mode	21
10.6.3	Cascaded Mode.....	21
10.6.4	Dividers Alignment	21
10.6.5	Programmable Skew.....	21
10.7	Output Drivers.....	21
10.8	SD/OE Pin Function.....	22
10.9	I ² C Operation	22
11.	Typical Application Circuit	23
11.1	Input – Driving the XIN/REF or CLKIN.....	24
11.1.1	Driving XIN/REF with a CMOS Driver	24
11.1.2	Driving XIN with a LVPECL Driver	25
11.1.3	Wiring the CLKIN pin to Accept Single-Ended Inputs	25
11.1.4	Driving CLKIN with Differential Clock.....	26
11.2	Output – Single-ended or Differential Clock Terminations	27
11.2.1	LVDS Termination.....	27
11.2.2	LVPECL Termination	28
11.2.3	HCSL Termination.....	29
11.2.4	LVC MOS Termination.....	29
12.	Package Outline Drawings	29
13.	Marking Diagram.....	30
14.	Ordering Information	30
15.	Revision History.....	30

1. Pin Assignments

Figure 1. Pin Assignments for 6 × 6 mm 48-VFQFPN Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Type	Description
1	OUT10B	Output	Complementary output clock 10. Low-power HCSL (LP-HCSL) output.
2	XOUT	Output	Crystal oscillator interface output.
3	XIN/REF	Input	Crystal oscillator interface input, or single-ended LVCMOS clock input. Input voltage is 1.2V max.
4	VDDA	Power	Analog functions power supply pin. Connect to 1.8V.
5	VDDO	Power	Connect to 1.8V. Power pin for outputs 3, and 5–11

Pin	Name	Type		Description
6	OUT9	Output		Output clock 9. Low-power HCSL (LP-HCSL) output.
7	OUT9B	Output		Complementary output clock 9. Low-power HCSL (LP-HCSL) output.
8	OUT8	Output		Output clock 8. Low-power HCSL (LP-HCSL) output.
9	OUT8B	Output		Complementary output clock 8. Low-power HCSL (LP-HCSL) output.
10	OUT7	Output		Output clock 7. Low-power HCSL (LP-HCSL) output.
11	OUT7B	Output		Complementary output clock 7. Low-power HCSL (LP-HCSL) output.
12	SD/OE	Input	Internal Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when the pin is configured as OE (Default is active LOW.) It has a weak internal pull-down resistor. When configured as SD, the device is shut down, differential outputs are driven high/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low depending on the programming bits as discussed in "SD/OE Pin Function".
13	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I ² C SDA input as selected by OUT0_SEL_I2CB. It has a weak internal pull-down resistor.
14	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I ² C SCL input as selected by OUT0_SEL_I2CB. It has a weak internal pull-down resistor.
15	VDD	Power		Connect to 1.8V.
16	VDDO	Power		Connect to 1.8V. Power pin for outputs 3, and 5–11.
17	OUT6	Output		Output clock 6. Low-power HCSL (LP-HCSL) output.
18	OUT6B	Output		Complementary output clock 6. Low-power HCSL (LP-HCSL) output.
19	OUT5	Output		Output clock 5. Low-power HCSL (LP-HCSL) output.
20	OUT5B	Output		Complementary output clock 5. Low-power HCSL (LP-HCSL) output.
21	VDDO4	Power		Connect to 1.8V to 3.3V. VDD supply for OUT4.
22	OUT4	Output		Output clock 4. For more information, see "Output Drivers."
23	OUT4B	Output		Complementary output clock 4. For more information, see "Output Drivers."
24	OEA	Input	Internal Pull-down	Active low output enable pin for outputs 3, 5, 6, and 11. 0 = Enable outputs, 1 = Disable outputs. This pin has an internal pull-down.
25	NC	—		Do not connect.
26	NC	—		Do not connect.
27	VDDO	Power		Connect to 1.8V. This is a power pin for outputs 3, and 5–11.
28	OUT3B	Output		Complementary output clock 3. Low-power HCSL (LP-HCSL) output.
29	OUT3	Output		Output clock 3. Low-power HCSL (LP-HCSL) output.
30	VDD_Core	Power		Connect to 1.8V.
31	VDD	Power		Connect to 1.8V.

Pin	Name	Type		Description
32	NC	Input		Do not connect.
33	OEB7_10	Input	Internal Pull-down	Active low output enable pin for outputs 7–10. 0 = Enable outputs; 1 = Disable outputs. This pin has an internal pull-down.
34	OUT2B	Output		Complementary output clock 2. For more information, see “Output Drivers.”
35	OUT2	Output		Output clock 2. For more information, see “Output Drivers.”
36	VDDO2	Power		Connect to 1.8V to 3.3V. VDD supply for OUT2
37	OUT1B	Output		Complementary output clock 1. For more information, see “Output Drivers.”
38	OUT1	Output		Output clock 1. For more information, see “Output Drivers.”
39	VDDO1	Power		Connect to 1.8V to 3.3V. VDD supply for OUT1.
40	NC	—		Do not connect.
41	OUT11	Output		Output clock 11. Low-power HCSL (LP-HCSL) output.
42	OUT11B	Output		Complementary output clock 11. Low-power HCSL (LP-HCSL) output.
43	VDDO	Power		Connect to 1.8V. Power pin for outputs 3, and 5–11
44	VDD	Power		Connect to 1.8V.
45	OE_buffer	Input	Internal Pull-up	Active High Output enable for outputs 3, and 5–11. 0 = Disable outputs; 1 = Enable outputs. This pin has an internal pull-up.
46	VDDO0	Power		Power supply pin for OUT0_SEL_I2CB and crystal oscillation. Connect to 1.8 to 3.3V. It sets the output voltage levels for OUT0.
47	OUT0_SEL_I2CB	Output	Internal Pull-down	Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 13 and 14. If a weak pull-up (10Kohms) is placed on OUT0_SEL_I2CB, pins 13 and 14 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull-down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 13 and 14 will act as the SDA and SCL pins of an I ² C interface. After power up, the pin acts as a LVCMOS reference output.
48	OUT10	Output		Output clock 10. Low-power HCSL (LP-HCSL) output.
ePAD	GND	GND		Connect to ground pad

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DDA} , V_{DDD} , V_{DDO}	3.6V
XIN/REF Input	1.2V
CLKIN, CLKINB Input	V_{DDO0} , 1.2V voltage swing
I ² C Loading Current (SDA)	10mA
Storage Temperature, TSTG	-65°C to 150°C
ESD Human Body Model	2000V

4. Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Theta JA. Junction to air thermal impedance (0mps)	41.06	°C/W
θ_{JB}	Theta JB. Junction to board thermal impedance (0mps)	13.6	°C/W
θ_{JC}	Theta JC. Junction to case thermal impedance (0mps)	36.42	°C/W

5. Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DDOX}	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions.	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
T_A	Operating temperature, ambient.	-40		85	°C
C_L	Maximum load capacitance (3.3V LVCMOS only).			15	pF

6. Electrical Characteristics

Table 5. Current Consumption Characteristics

V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V \pm 5%, 2.5V \pm 5%, 1.8V \pm 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$I_{DDCORE}^{[a]}$	Core Supply Current	100MHz on all outputs, 25MHz REFCLK.		33	42	mA
I_{DDOX}	Output Buffer Supply Current	LVPECL, 350MHz, 3.3V $V_{DDOX}^{[b]}$		45	58	mA
		LVPECL, 350MHz, 2.5V $V_{DDOX}^{[b]}$		36	47	mA
		LVDS, 350MHz, 3.3V $V_{DDOX}^{[b]}$		26	32	mA
		LVDS, 350MHz, 2.5V $V_{DDOX}^{[b]}$		25	30	mA
		LVDS, 350MHz, 1.8V $V_{DDOX}^{[b]}$		22	27	mA
		HCSL, 250MHz, 3.3V $V_{DDOX}^{[b]}$		39	48	mA
		HCSL, 250MHz, 2.5V $V_{DDOX}^{[b]}$		37	46	mA
		LVC MOS, 50MHz, 3.3V, $V_{DDOX}^{[b],[c]}$		22	27	mA
		LVC MOS, 50MHz, 2.5V, $V_{DDOX}^{[b],[c]}$		20	24	mA
		LVC MOS, 50MHz, 1.8V, $V_{DDOX}^{[b],[c]}$		17	21	mA
		LVC MOS, 200MHz, 3.3V $V_{DDOX}^{[b],[c]}$		43	56	mA
		LVC MOS, 200MHz, 2.5V $V_{DDOX}^{[b],[c]}$		33	43	mA
		LVC MOS, 200MHz, 1.8V $V_{DDOX}^{[b],[c]}$		24	31	mA
I_{DDPD}	Power Down Current	SD asserted, I ² C programming.		10	12	mA

[a] $I_{DDCORE} = I_{DDA} + I_{DDD}$.

[b] Measured into a 5" 50Ω trace. See Test Loads section for more details.

[c] Single CMOS driver active.

Table 6. AC Timing Characteristics

 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
F_{IN} [a]	Input Frequency	Input frequency limit (Crystal)	8		40	MHz
		Input frequency limit (CLKIN, CLKINB)	1		350	
		Input frequency limit (Single-ended over XIN)	1		200	
F_{OUT} [b]	Output Frequency	Single-ended clock output limit (LVCMOS), individual FOD mode.	1		200	MHz
		Differential clock output (LVPECL/LVDS/HCSL), individual FOD mode.	1		350	
		Single-ended clock output limit (LVCMOS), cascaded FOD mode, output 2–4.	0.001		200	
		Differential clock output limit (LVPECL/LVDS/HCSL), cascaded FOD mode, output 2–4.	0.001		350	
f_{VCO}	VCO Operating Frequency Range		2500		2900	MHz
T_{DC} [c]	Output Duty Cycle	Measured at $V_{DD}/2$, all outputs except reference output, $V_{DDOX} = 2.5V$ or $3.3V$.	45	50	55	%
		Measured at $V_{DD}/2$, all outputs except reference output, $V_{DDOX} = 1.8V$	40	50	60	%
		Measured at $V_{DD}/2$, reference output OUT0 (5–150.1MHz) with 50% duty cycle input.	40	50	60	%
		Measured at $V_{DD}/2$, reference output OUT0 (150.1–200MHz) with 50% duty cycle input.	30	50	70	%
T_{SKEW}	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns.		75		ps
$T_{STARTUP}$ [d] [e]	Startup Time	Measured after all V_{DDs} have raised above 90% of their target value. [f]			30	ms
		PLL lock time from shutdown mode.		3	4	ms

[a] Practical lower frequency is determined by loop filter settings.

[b] A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.

[c] Duty cycle is only guaranteed at maximum slew rate settings.

[d] Actual PLL lock time depends on the loop configuration.

[e] Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.

[f] Power-up with temperature calibration enabled, please contact IDT if shorter lock-time is required in system.

Table 7. Input Characteristics

 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless stated otherwise.

Symbol	Parameter	Pins	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLKIN,CLKINB,CLKSEL,SD/OE,SEL1/SDA,SEL0/SCL		3	7	pF
R_{PD}	Pull-down Resistor	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL, CLKIN, CLKINB, OUT0_SEL_I2CB	100		300	k Ω
V_{IH}	Input High Voltage	CLKSEL, SD/OE	$0.7 \times V_{DDD}$		$V_{DDD} + 0.3$	V
V_{IL}	Input Low Voltage	CLKSEL, SD/OE	GND - 0.3		$0.3 \times V_{DDD}$	V
V_{IH}	Input High Voltage	OUT0_SEL_I2CB	$0.65 \times V_{DDO0}$		$V_{DDO0} + 0.3$	V
V_{IL}	Input Low Voltage	OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input High Voltage	XIN/REF	0.8		1.2	V
V_{IL}	Input Low Voltage	XIN/REF	GND - 0.3		0.4	V
T_R/T_F	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	ns

Table 8. CLKIN Electrical Characteristics

 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{SWING}	Input Amplitude – CLKIN, CLKINB	Peak to peak value, single-ended	200		1200	mV
dv/dt	Input Slew Rate – CLKIN, CLKINB	Measured differentially	0.4		8	V/ns
I_{IL}	Input Leakage Low Current	$V_{IN} = GND$	-5		5	μA
I_{IH}	Input Leakage High Current	$V_{IN} = 1.7V$			20	μA
DC_{IN}	Input Duty Cycle	Measurement from differential waveform	45		55	%

Table 9. Electrical Characteristics – CMOS Outputs

 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	$I_{OH} = -15mA(3.3V), -12mA(2.5V), -8mA(1.8V)$	$0.7 \times V_{DDO}$		V_{DDO}	V
V_{OL}	Output Low Voltage	$I_{OH} = 15mA(3.3V), 12mA(2.5V), 8mA(1.8V)$			0.4	V
R_{OUT}	Output Driver Impedance	CMOS Output Driver		17		Ω
T_{SR}	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (output load = 5pF) $V_{DDOX} = 3.3V$	1.0	2.2		V/ns
	Slew Rate, SLEW[1:0] = 01		1.2	2.3		
	Slew Rate, SLEW[1:0] = 10		1.3	2.4		
	Slew Rate, SLEW[1:0] = 11		1.7	2.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (output load = 5pF) $V_{DDOX} = 2.5V$	0.6	1.3		
	Slew Rate, SLEW[1:0] = 01		0.7	1.4		
	Slew Rate, SLEW[1:0] = 10		0.6	1.4		
	Slew Rate, SLEW[1:0] = 11		1.0	1.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (output load = 5pF) $V_{DD} = 1.8V$.	0.3	0.7		
	Slew Rate, SLEW[1:0] = 01		0.4	0.8		
	Slew Rate, SLEW[1:0] = 10		0.4	0.9		
	Slew Rate, SLEW[1:0] = 11		0.7	1.2		
I_{OZDD}	Output Leakage Current (OUT1–4)	Tri-state outputs			5	μA
	Output Leakage Current (OUT0)	Tri-state outputs			30	μA

Table 10. Electrical Characteristics – LVDS Outputs

 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_{OT} (+)$	Differential Output Voltage for the TRUE Binary State	247		454	mV
$V_{OT} (-)$	Differential Output Voltage for the FALSE Binary State	-454		-247	mV
ΔV_{OT}	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage) at $3.3V \pm 5\%$, $2.5V \pm 5\%$	1.125	1.25	1.375	V
	Output Common Mode Voltage (Offset Voltage) at $1.8V \pm 5\%$	0.8	0.875	0.96	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT+} or $V_{OUT-} = 0V$ or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, $V_{OUT+} = V_{OUT-}$		6	12	mA
T_R	LVDS rise time 20%-80%		300		ps
T_F	LVDS fall time 80%-20%		300		ps

Table 11. Electrical Characteristics – LVPECL Outputs

 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OH}	Output Voltage High, terminated through 50Ω tied to $V_{DD} - 2V$	$V_{DDO} - 1.19$		$V_{DDO} - 0.69$	V
V_{OL}	Output Voltage Low, terminated through 50Ω tied to $V_{DD} - 2V$	$V_{DDO} - 1.94$		$V_{DDO} - 1.4$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	0.55		0.993	V
T_R	LVPECL rise time 20%-80%		400		ns
T_F	LVPECL fall time 80%-20%		400		ns

Table 12. Electrical Characteristics – HCSL Outputs^[a]
 $V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, T_A = -40^\circ C \text{ to } +85^\circ C$, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
dV/dt	Slew Rate	Scope averaging on ^[b] ^[c]	1		4	V/ns
$\Delta dV/dt$	Slew Rate Matching	Scope averaging on ^[b] ^[c]			20	%
V_{MAX}	Maximum Voltage	Measurement on single-ended signal using absolute value (scope averaging off)			1150	mV
V_{MIN}	Minimum Voltage		-300			mV
V_{SWING}	Voltage Swing	Scope averaging off ^[b] ^[f]	300			mV
V_{CROSS}	Crossing Voltage Value	Scope averaging off ^[d] ^[f]	250		550	mV
ΔV_{CROSS}	Crossing Voltage Variation	Scope averaging off ^[e]			140	mV

[a] Guaranteed by design and characterization. Not 100% tested in production.

[b] Measured from differential waveform.

[c] Slew rate is measured through the V_{SWING} voltage range centered on differential 0V. This results in a $\pm 150mV$ window around differential 0V.

[d] V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e., Clock rising and Clock# falling).

[e] The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.

[f] Measured from single-ended waveform.

Table 13. Spread-Spectrum Generation Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{SSOUT}	Spread Frequency	Output frequency range for spread spectrum	5		300	MHz
f_{MOD}	Mod Frequency	Modulation frequency.	30 to 63			kHz
f_{SPREAD}	Spread Value	Amount of spread value (programmable)–center spread.	$\pm 0.25\%$ to $\pm 2.5\%$			% f_{OUT}
		Amount of spread value (programmable)–down spread.	-0.5% to -5%			

Table 14. I²C Bus (SCL/SDA) DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V _{IH}	Input High Level	For SEL1/SDA pin and SEL0/SCL pin.	0.7 x V _{DDD}			V
V _{IL}	Input Low Level	For SEL1/SDA pin and SEL0/SCL pin.			0.3 x V _{DDD}	V
V _{HYS}	Hysteresis of Inputs		0.05 x V _{DDD}			V
I _{IN}	Input Leakage Current		-1		30	μA
V _{OL}	Output Low Voltage	I _{OL} = 3mA			0.4	V

 Table 15. I²C Bus (SCL/SDA) AC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
F _{SCLK}	Serial Clock Frequency (SCL)	10		400	kHz
t _{BUF}	Bus Free Time between Stop and Start	1.3			μs
t _{SU:START}	Setup Time, Start	0.6			μs
t _{HD:START}	Hold Time, Start	0.6			μs
t _{SU:DATA}	Setup Time, Data Input (SDA)	0.1			μs
t _{HD:DATA}	Hold Time, Data Input (SDA) ¹	0			μs
t _{OVD}	Output Data Valid from Clock			0.9	μs
C _B	Capacitive Load for Each Bus Line			400	pF
t _R	Rise Time, Data and Clock (SDA, SCL)	20 + 0.1 x C _B		300	ns
t _F	Fall Time, Data and Clock (SDA, SCL)	20 + 0.1 x C _B		300	ns
t _{HIGH}	High Time, Clock (SCL)	0.6			μs
t _{LOW}	Low Time, Clock (SCL)	1.3			μs
t _{SU:STOP}	Setup Time, Stop	0.6			μs

[a] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH(MIN)} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[b] I²C inputs are 5V tolerant.

7. Test Loads

Figure 2. LVCMOS Test Load

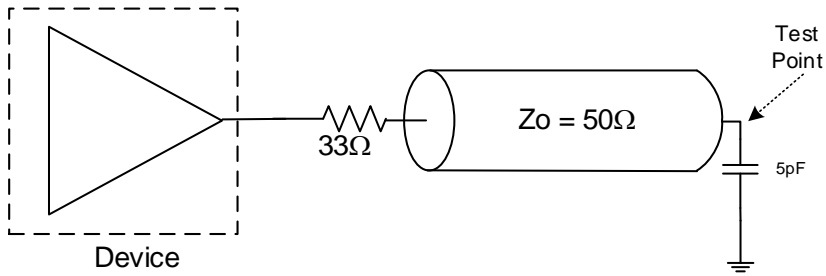


Figure 3. HCSL Test Load

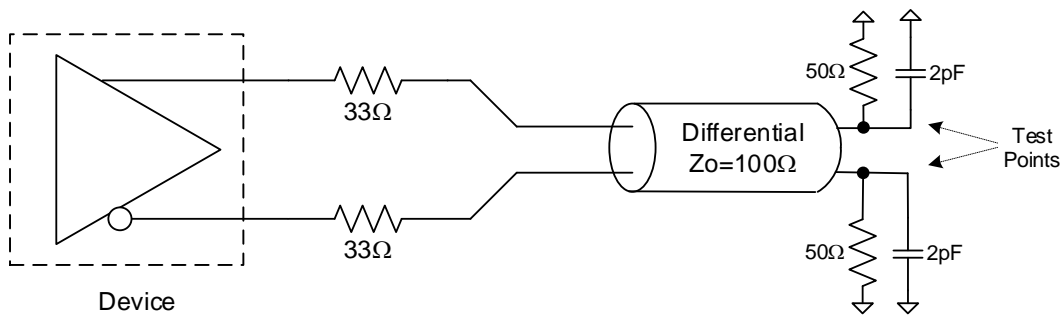


Figure 4. LVDS Test Load

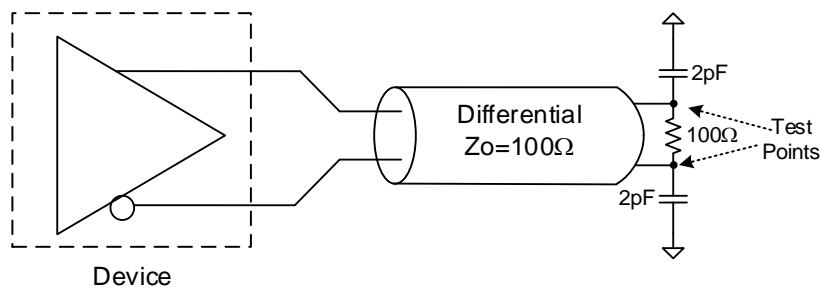
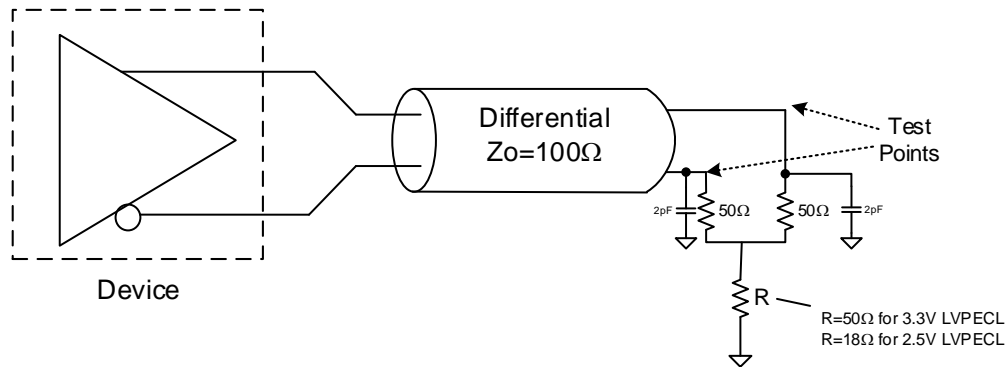
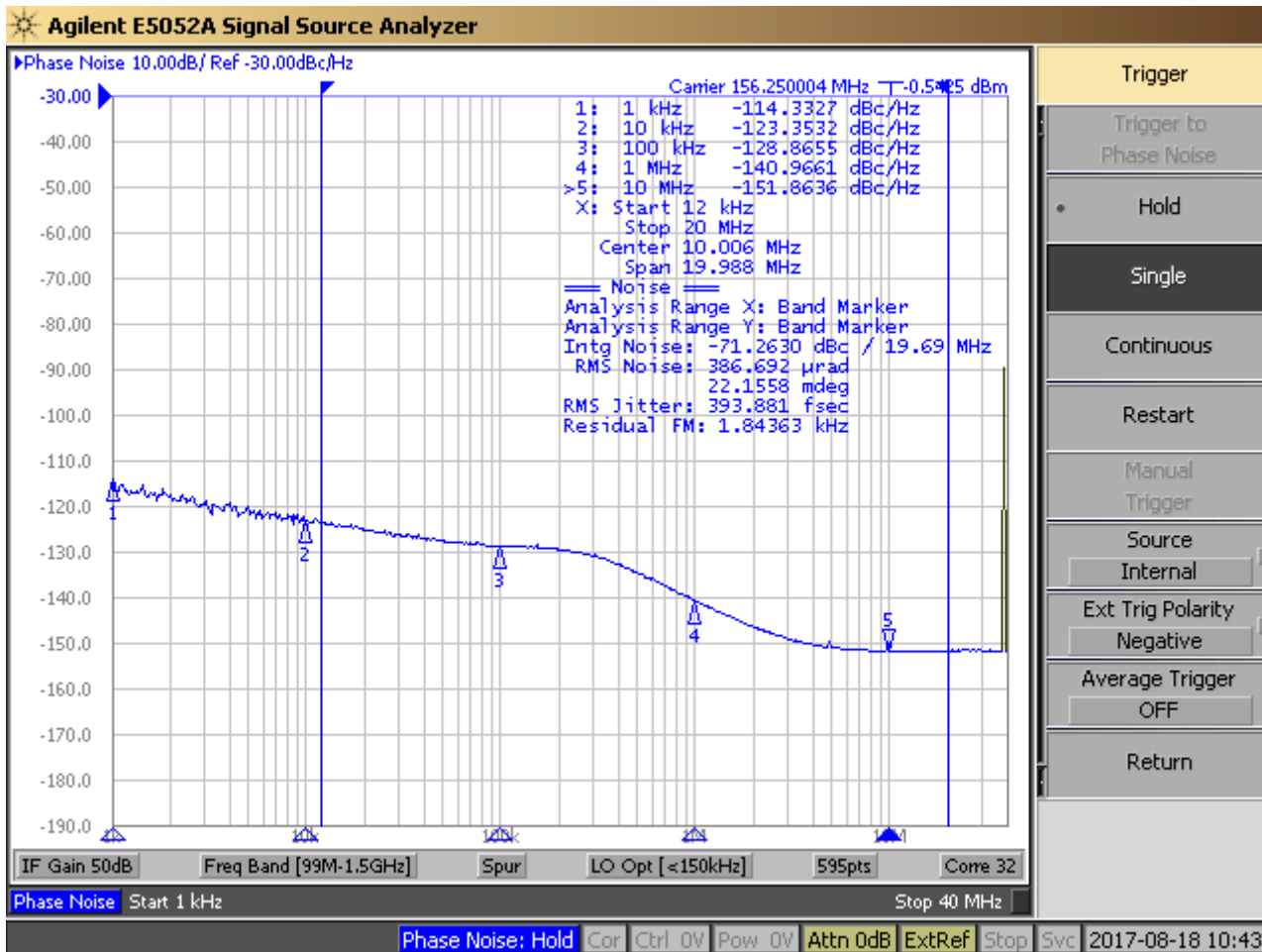


Figure 5. LVPECL Test Load



8. Jitter Performance Characteristics

Figure 6. Typical Phase Jitter Plot at 156.25MHz



Note: Measured with OUT2=156.25MHz on, 39.625MHz input.

Table 16. Jitter Performance^{[a] [b]}

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
J _{CY-CY}	Cycle to Cycle Jitter	LVC MOS 3.3V ±5%, -40°C to 90°C		5	30	ps
		All differential outputs 3.3V ±5%, -40°C to 90°C		25	35	ps
J _{pk-pk}	Period Jitter	LVC MOS 3.3V ±5%, -40°C-90°C		28	40	ps
		All differential outputs 3.3V ±5%, -40°C to 90°C		4	30	ps
J _{RMS}	RMS Phase Jitter (12kHz-20MHz)	LVC MOS 3.3V ±5%, -40°C to 90°C		0.3		ps
		All differential outputs 3.3V ±5%, -40°C to 90°C		0.5		ps

[a] Measured with 25MHz crystal input

[b] Configured with OUT0 = 25MHz-LVC MOS OUT1 = 100MHz HCSL OUT2 = 125MHz LVDS OUT3 = 156.25MHz-LVPECL

9. PCI Express Jitter Performance and Specification

 Table 17. PCI Express Jitter Performance ^{[a] [b]}

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limit	Units
PCIe Jitter (Common Clock-CC)	$t_{jphPCIeG1-CC}$	PCIe Gen 1 ^[c]		28.7		86	ps (p-p)
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		0.27		3	ps (rms)
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		2.56		3.1	ps (rms)
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.8		1	ps (rms)
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (SSC OFF) (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.26		0.5	ps (rms)
PCIe Jitter (IR) ^{[d] [e]}	$t_{jphPCIeG2-SRNS}$	PCIe Gen 2 (SSC OFF) (PLL BW of 16MHz, CDR = 5MHz)		0.93		2	ps (rms)
	$t_{jphPCIeG3-SRNS}$	PCIe Gen 3(SSC OFF) (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.32		0.7	ps (rms)

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] Based on PCIe Base Specification Rev4.0 version 0.7draft. For the latest specifications, see www.pcisig.com.

[c] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 10^{-12} .

[d] According to the PCIe Base Specification Rev4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

[e] IR(Independent Reference) is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures.

10. Features and Functional Blocks

10.1 Device Startup and Power-on-Reset

The 5P49V6975A has an internal power-up reset (POR) circuit. All VDDs must be connected to the desired supply voltage to trigger a POR.

The user can define specific default configurations through internal One-Time-Programmable (OTP) memory -- either the user or factory can program the default configuration. Contact IDT if a specific factory-programmed default configuration is required, or refer to the *VersaClock 6E Programming Guide*.

The device will identify which of the two modes to operate in by the state of the OUT0_SEL_I2CB pin at POR. Both modes' default configurations can be programmed as follows:

1. **Software Mode (I²C):** OUT0_SEL_I2CB is low at POR.

The I²C interface will be open to users for in-system programming, overriding device default configurations at any time.

2. **Hardware Select Mode:** OUT0_SEL_I2CB is high at POR.

The device has been programmed to load OTP at power-up (REG0[7] = 1). The device will load internal registers according to Table 18.

Internal OTP memory can support up to four configurations, which selectable by the SEL0/SEL1 pins.

At POR, logic levels at SEL0 and SEL1 pins must be settled, which results in the selected configuration to be loaded at power up.

After the first 10ms of operation, the levels of the SELx pins can be changed, either to low or to the same level as VDDD/VDDA. The SELx pins must be driven with a digital signal of < 300ns rise/fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

Table 18. Power-Up Behavior

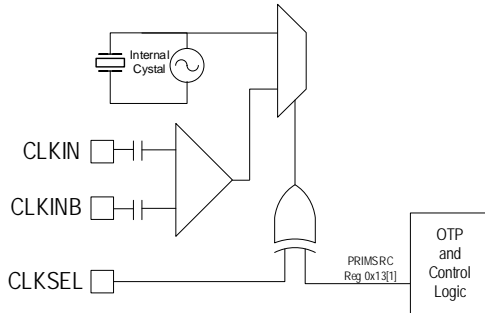
OUT0_SEL_I2CB at POR	SEL1	SEL0	I ² C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I ² C defaults
0	X	X	Yes	0	0

10.2 Reference Clock and Selection

The 5P49V6975A supports up to two clock inputs:

- Internal crystal input: This can be driven by a single ended clock.
- Clock input (CLKIN, CLKINB): This is a fully differential input that only accepts a reference clock. A single-ended clock can also drive it on CLKIN.

Figure 7. Clock Input Diagram Internal Logic



10.3 Manual Switchover

The CLKSEL pin selects the input clock between either XTAL/REF or (CLKIN, CLKINB). CLKSEL polarity can be changed by I²C programming (Byte 0x13[1]) as shown in the following table.

- 0 = XIN/REF, XOUT (default)
- 1 = CLKIN, CLKINB

Table 19. Input Clock Select

PRIMSRC	CLKSEL	Source
0	0	XIN/REF
0	1	CLKIN, CLKINB
1	0	CLKIN, CLKINB
1	1	XIN/REF

When SM[1:0] is 0x, the redundant inputs are in manual switchover mode. In this mode, CLKSEL pin is used to switch between the primary and secondary clock sources. The PRIMSRC bit determines the primary and secondary clock source setting. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift depending on the exact phase and frequency relationship between the primary and secondary clocks.

10.4 Internal Crystal Oscillator (XIN/REF)

10.4.1 Choosing Crystals

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa. Therefore, for an accurate oscillation frequency you must match the oscillator load capacitance with the crystal load capacitance.

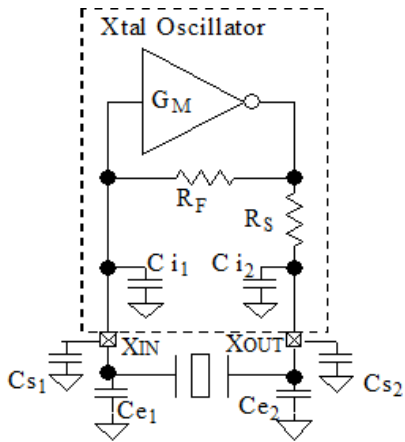
10.4.2 Tuning the Crystal Load Capacitor

Cs1 and Cs2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF (see Figure 8).

Ce1 and Ce2 are additional external capacitors. Increasing the load capacitance reduces the oscillator gain, so it is recommended to consult the manufacturer when adding Ce1 and/or Ce2 to avoid crystal startup issues.

Ci1 and Ci2 are integrated programmable load capacitors, one at XIN and one at XOUT.

Figure 8. Tuning the Crystal Load Capacitor



The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Ci1 and Ci2 are commonly programmed to be the same value. Adjustment of the crystal tuning capacitors allows maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table. Ci1/Ci2 starts at 9pF with the setting 000000b, and can be increased up to 25pF with the setting 111111b. The step per bit is 0.5pF.

Table 20. XTAL[5:0] Tuning Capacitor

Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.5	9	25

You can write the following equation for this capacitance:

$$C_i = 9\text{pF} + 0.5\text{pF} \times \text{XTAL}[5:0]$$

$$C_{XIN} = C_{i1} + C_{s1} + C_{e1}$$

$$C_{XOUT} = C_{i2} + C_{s2} + C_{e2}$$

The final load capacitance of the crystal:

$$C_L = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$$

It is recommended to set the same value at each crystal pin meaning:

$$C_{XIN} = C_{XOUT}$$

Example 1: The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is $C_s = 1.5\text{pF}$. Assuming an equal capacitance value at XIN and XOUT, the equation is as follows:

$$8\text{pF} = (9\text{pF} + 0.5\text{pF} \times \text{XTAL}[5:0] + 1.5\text{pF}) / 2$$

So, XTAL[5:0] = 11 (decimal)

Example 2: The crystal load capacitance is specified as 12pF and the stray capacitance C_s is unknown. Footprints for external capacitors C_e are added and a worst case C_s of 5pF is used. This example uses $C_s + C_e = 5\text{pF}$; the correct value for C_e can be determined later to make 5pF together with C_s .

$$12\text{pF} = (9\text{pF} + 0.5\text{pF} \times \text{XTAL}[5:0] + 5\text{pF}) / 2$$

So, XTAL[5:0] = 20 (decimal)

Table 21. Recommended Crystal Characteristics

Parameter	Minimum	Typical	Maximum	Units
Mode of Oscillation	Fundamental			
Frequency	8	25	40	MHz
Equivalent Series Resistance (ESR)		10	100	Ω
Shunt Capacitance			7	pF
Load Capacitance (C_L) at $\leq 25\text{MHz}$	6	8	12	pF
Load Capacitance (C_L) $> 25\text{MHz}$ to 40MHz	6		8	pF
Maximum Crystal Drive Level			100	μW

10.5 Programmable Loop Filter

The device PLL loop bandwidth operating range depends on the input reference frequency (F_{ref}).

Table 22. Loop Filter Settings

Input Reference Frequency (MHz)	Loop Bandwidth Minimum (kHz)	Loop Bandwidth Maximum (kHz)
1	40	126
350	300	1000

10.6 Fractional Output Dividers (FOD)

The 5P49V6975A has four fractional output dividers (FOD). Each FOD is comprised of a 12-bit integer counter and a 24-bit fractional counter. The output divider can operate in integer divide only mode for improved performance, or use the fractional counters to generate a clock frequency accurate to 50ppb.

FODs support the following features.

10.6.1 Individual Spread Spectrum Modulation

The output clock frequencies can be modulated to spread energy across a broader range of frequencies, thereby lowering system EMI. Each divider has individual spread ability. Spread modulation independent of output frequency, a triangle wave modulation between 30 and 63kHz.

Spread spectrum can be applied to any output clock, clock frequency, or spread amount from $\pm 0.25\%$ to $\pm 2.5\%$ center-spread and -0.5% to -5% down-spread.

10.6.2 Bypass Mode

Bypass mode (divide by 1) allows the output to behave as a buffered copy from the input or another FOD.

10.6.3 Cascaded Mode

As shown in the block diagram on page 1, FODs can be cascaded for lower output frequency.

For example, if OUT1 is configured to run at 12.288MHz and needs another 48kHz output, the user can cascade FOD2 by taking input from OUT1, with a divide ratio of 256. As a result, OUT 2 runs at 48kHz while in alignment with 12.288MHz on OUT1.

10.6.4 Dividers Alignment

Each output divider block has a synchronizing pulse to provide startup alignment between outputs dividers. This allows alignment of outputs for low skew performance.

When the 5P49V6975A is in hardware select mode, outputs are automatically aligned at POR. The same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration.

When the 5P49V6975A is using software mode, I²C is used to reprogram an output divider during operation, and therefore, alignment can be lost. Alignment can be restored by manually triggering a reset through I²C.

The outputs are aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by using the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.

10.6.5 Programmable Skew

The 5P49V6975A can skew outputs by quadrature values. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. As a result, for 100MHz output and a 2800MHz VCO, the user can select how many 11.161ps units to be added to the skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

10.7 Output Drivers

Device output drivers can individually support the following features:

- 2.5V or 3.3V voltage level for HCSL/LVPECL operation
- 1.8V, 2.5V, or 3.3V voltage levels for CMOS/LVDS operation
- CMOS supports four operating modes:
 - CMOSD: OUTx and OUTxB 180 degrees out of phase
 - CMOSX2: OUTx and OUTxB phase-aligned
 - CMOS1: only OUTx pin is on
 - CMOS2: only OUTxB pin is on

When a given output is configured to CMOSD or CMOSX2, then all previously described configuration and control apply equally to both pins.

- Independent output enable/disabled by register bits. When disabled, an output can be either in a logic 1 state or Hi-Z.

The following options are used to disable outputs:

- Output turned off by I²C
- Output turned off by SD/OE pin
- Output unused, which means it is turned off regardless of OE pin status

10.8 SD/OE Pin Function

The SD/OE pin can be programmed as follows:

- OE output enable (low active)
- OE output enable (high active)
- Global shutdown (low active)
- Global shutdown (high active)

Output behavior when disabled is also programmable. The user can select the output driver behavior when it is off as follows:

- OUTx pin high, OUTxB pin low (controlled by SD/OE pin)
- OUTx/OUTxB Hi-Z (controlled by SD/OE pin)
- OUTx pin high, OUTxB pin low (configured through I²C)
- OUTx/OUTxB Hi-Z (configured by I²C)

The user can disable the output with either I²C or SD/OE pin. For more information, see the *VersaClock 6E Programming Guide*.

10.9 I²C Operation

The 5P49V6975A acts as a slave device on the I²C bus using one of the two I²C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations.

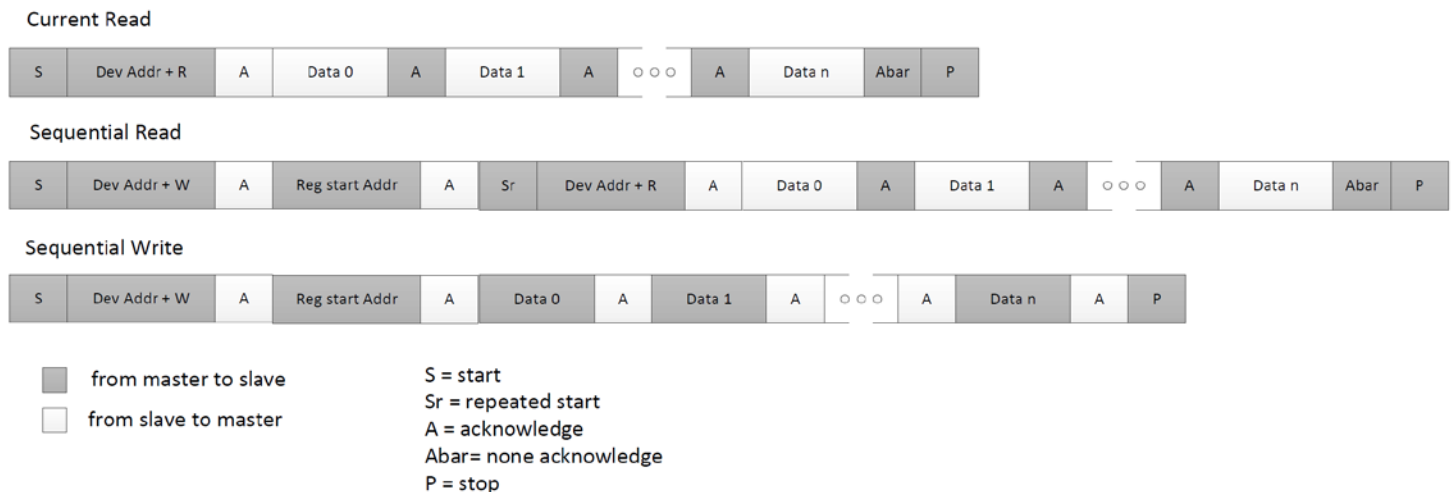
Address bytes (2 bytes) specify the register address of the byte position of the first register to write or read.

Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first).

Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

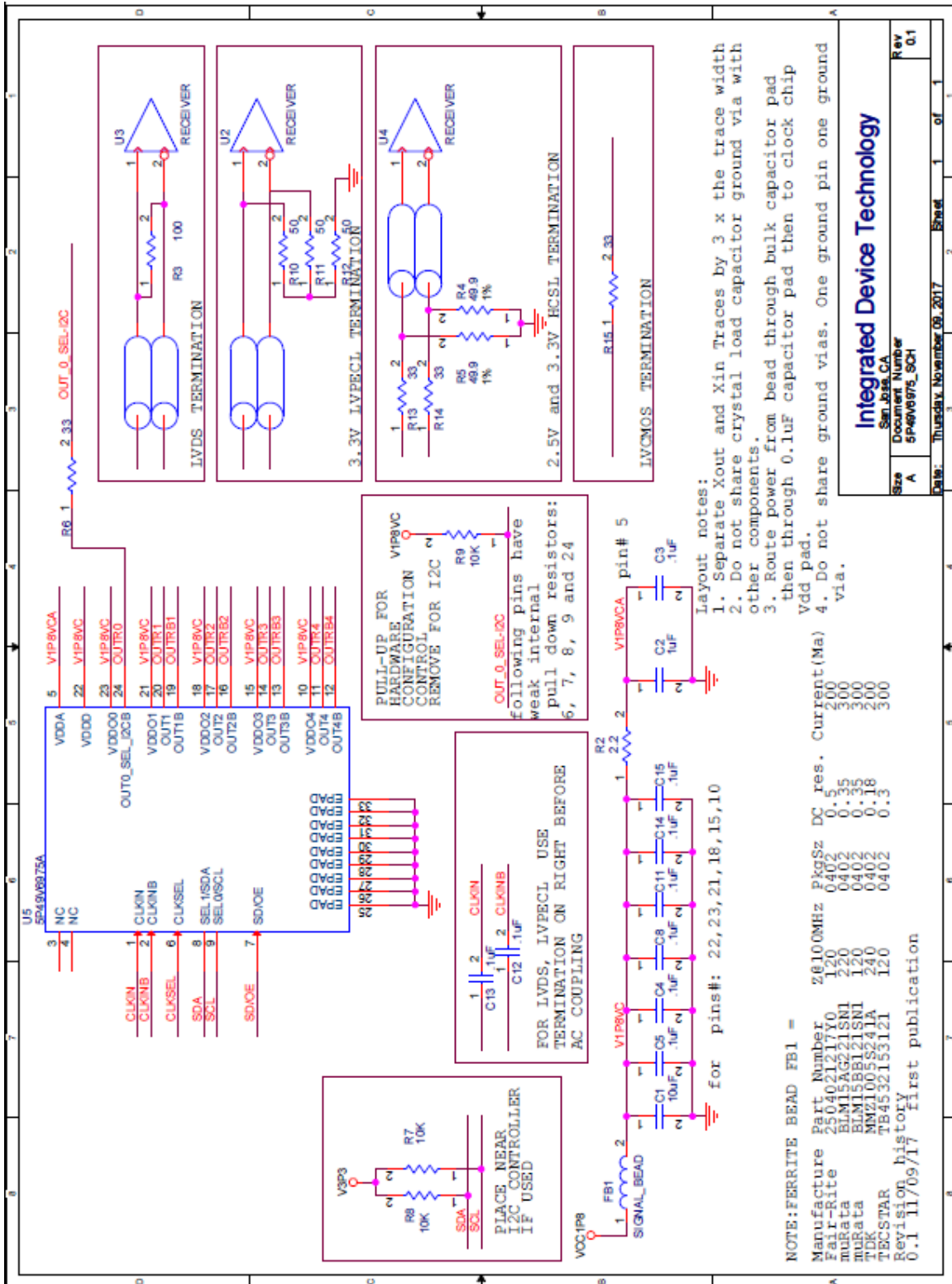
For full electrical I²C compliance, use external pull-up resistors for SDATA and SCLK.

Figure 9. I²C R/W Sequence



11. Typical Application Circuit

Figure 10. Typical Application Circuit



11.1 Input – Driving the XIN/REF or CLKIN

11.1.1 Driving XIN/REF with a CMOS Driver

In some instances, it is preferable to have XIN/REF driven by a clock input -- for reasons such as better SNR, multiple input select with device CLKIN, etc. The XIN/REF pin can take an input when its amplitude is between 500mV and 1.2V, and the slew rate less than 0.2V/ns. The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating.

Figure 11. Overdriving XIN with a CMOS Driver

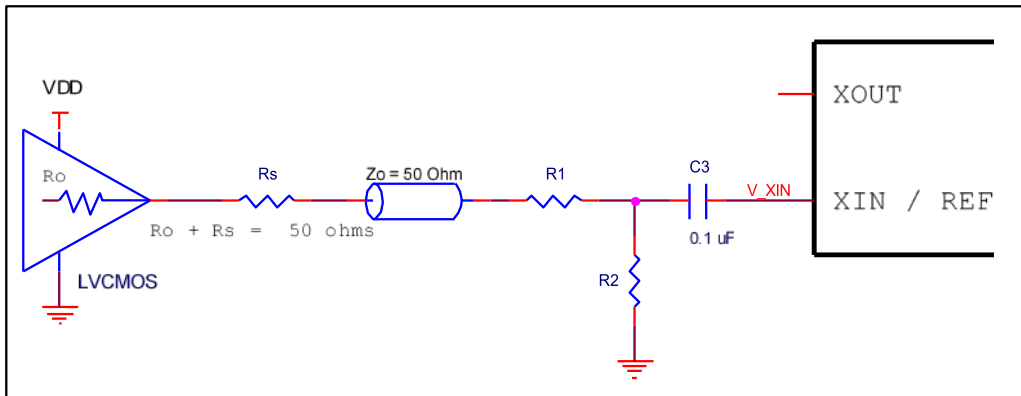


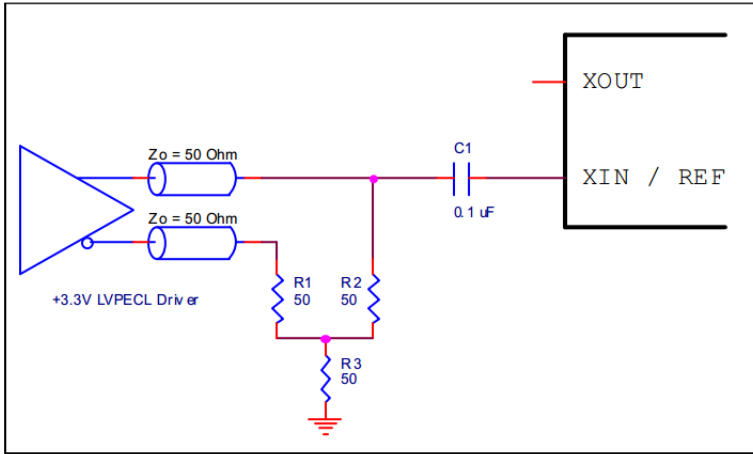
Table 23. Nominal Voltage Divider Values for Overdriving CLKIN with Single-ended Driver

LVC MOS Diver V_{DD}	$R_o + R_s$	R_1	R_2	V_{XIN} (peak)	$R_o+R_s+R_1+R_2$
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

11.1.2 Driving XIN with a LVPECL Driver

Figure 11 shows an example of the interface diagram for a 3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematic be placed in the layout; though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and guaranteed using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only required change is to use the appropriate R3 value.

Figure 12. Overdriving XIN with a LVPECL Driver



11.1.3 Wiring the CLKIN pin to Accept Single-Ended Inputs

CLKIN cannot take a signal larger than 1.2V pk-pk due to the 1.2V regulated input inside. However, since it is internally AC coupled it can accept both LVDS and LVPECL input signals.

Occasionally it is desired to have CLKIN to take CMOS levels. Figure 12 shows an example of how this can be achieved. This configuration has three properties:

- Total output impedance of R_o and R_s matches the 50Ω transmission line impedance
- V_{rx} voltage is generated at the CLKIN, which maintains the LVCMOS driver voltage level across the transmission line for best S/N
- R_1 - R_2 voltage divider values ensure that V_{rx} p-p at CLKIN is less than the maximum value of 1.2V

Figure 13. Recommended Schematic for Driving CLKIN with LVCMOS Driver

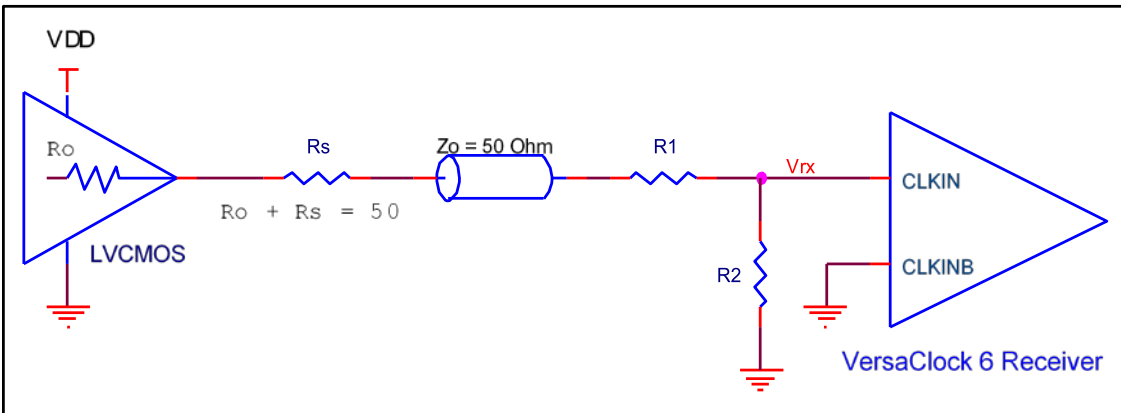


Table 21 shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver V_{DD} , V_{DD00} , and 5% resistor tolerances. The resistor values can be adjusted to reduce the loading for a slower and weaker LVCMOS driver by increasing the impedance of the R1–R2 divider. To better assist with this assessment, the total load ($R_0+R_s+R_1+R_2$) on the driver is included in the table.

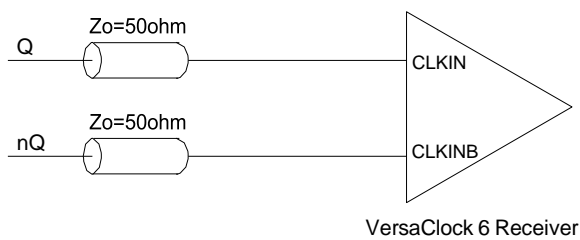
Table 24. Nominal Voltage Divider Values for Overdriving CLKIN with Single-ended Driver

LVCMOS Diver V_{DD}	$R_0 + R_s$	R1	R2	V_{rx} (peak)	$R_0+R_s+R_1+R_2$
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

11.1.4 Driving CLKIN with Differential Clock

CLKIN/CLKINB will accept DC coupled HCSL/LVPECL/LVDS signals.

Figure 14. CLKIN, CLKINB Input Driven by an HCSL Driver



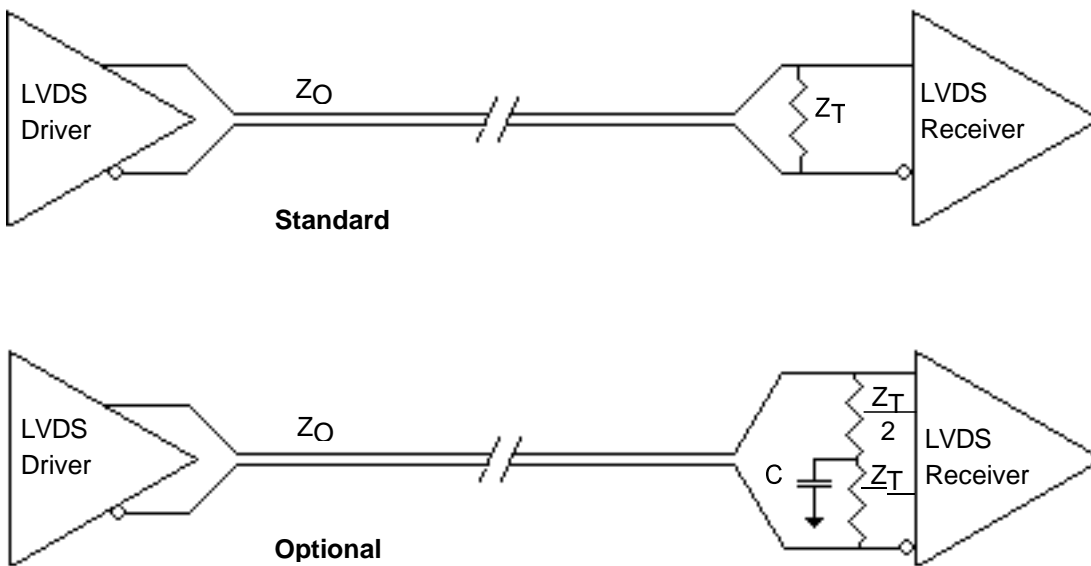
11.2 Output – Single-ended or Differential Clock Terminations

11.2.1 LVDS Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω Differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the IDT LVDS output.

If using a non-standard termination, it is recommended to contact IDT and confirm that the termination will function as intended. For example, the LVDS outputs cannot be AC coupled by placing capacitors between the LVDS outputs and the 100Ω shunt load. If AC coupling is required, the coupling caps must be placed between the 100Ω shunt termination and the receiver. In this manner the termination of the LVDS output remains DC coupled.

Figure 15. Standard and Optional Terminations



11.2.2 LVPECL Termination

The clock layout topology shown below are typical terminations for LVPECL outputs. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. For $V_{DDO} = 2.5V$, the $V_{DDO} - 2V$ is very close to ground level. The R_3 in 2.5V LVPECL Output Termination can be eliminated and the termination is shown in 2.5V LVPECL Output Termination (2).

Figure 16. 3.3V LVPECL Output Termination

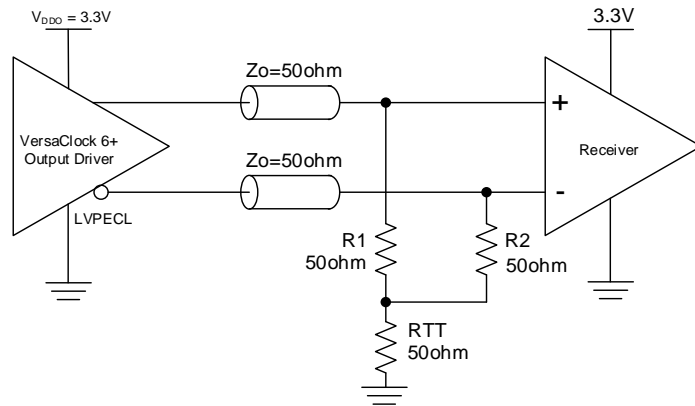


Figure 18. 2.5V LVPECL Output Termination

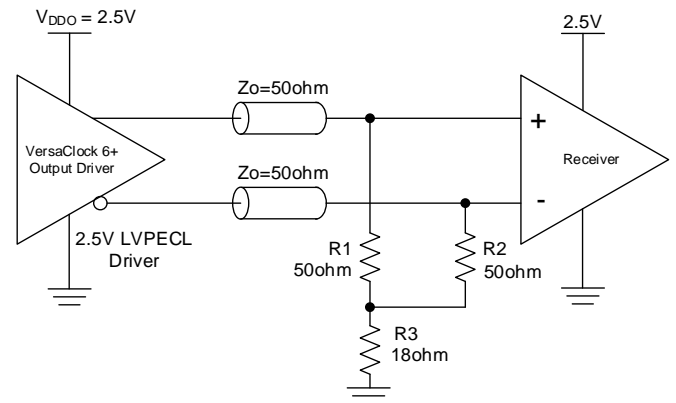


Figure 17. 3.3V LVPECL Output Termination (2)

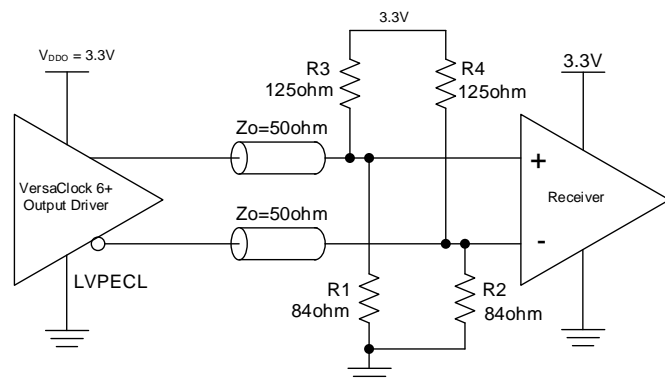


Figure 19. 2.5V LVPECL Output Termination (2)

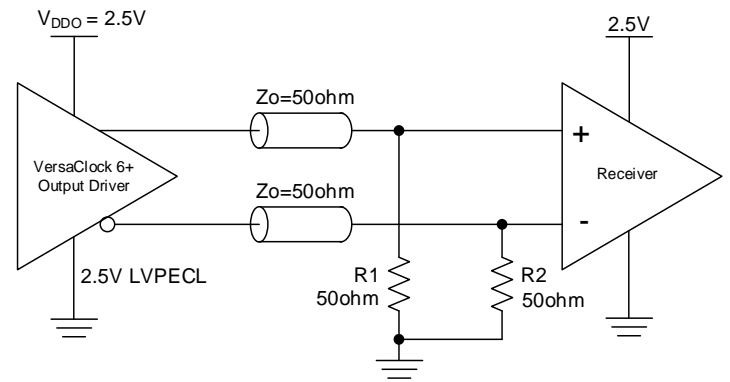
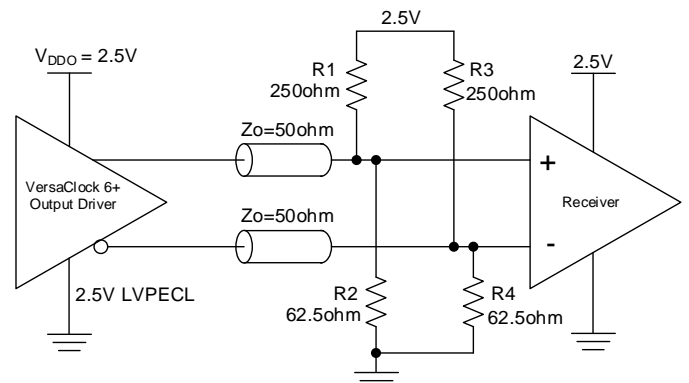


Figure 20. 2.5V LVPECL Output Termination (3)



11.2.3 HCSL Termination

HCSL termination scheme applies to both 3.3V and 2.5V VDDO.

Figure 21. HCSL Receiver Terminated

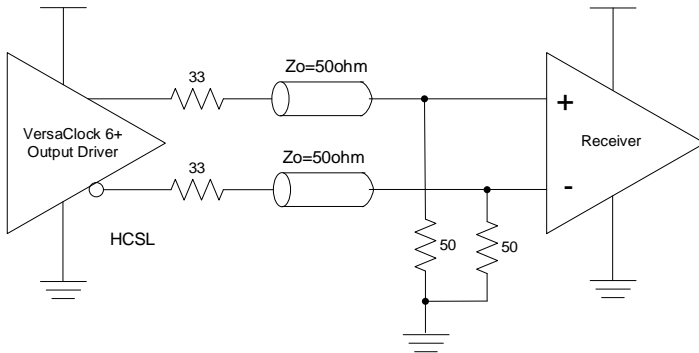
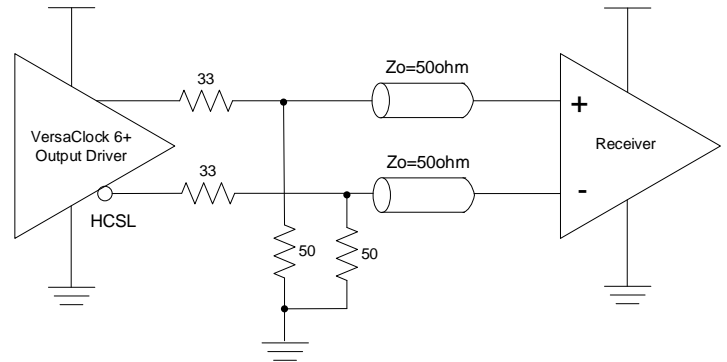


Figure 22. HCSL Source Terminated

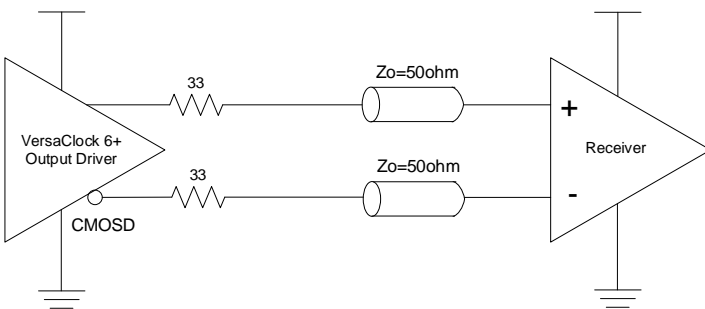


11.2.4 LVCMOS Termination

Each output pair can be configured as a standalone CMOS or dual-CMOS output driver. An example of CMOSD driver termination is shown in the following figure:

- CMOS1 – Single CMOS active on OUTx pin
- CMOS2 – Single CMOS active on OUTxB pin
- CMOSD – Dual CMOS outputs active on both OUTx and OUTxB pins, 180 degrees out of phase
- CMOSX2 – Dual CMOS outputs active on both OUTx and OUTxB pins, in-phase

Figure 23. LVCMOS Termination



12. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/ndndg-48-package-outline-60-x-60-mm-body-040-mm-pitch-qfn-epad-size-420-x-420-mm

13. Marking Diagram



1. Lines 1 and 2 indicate the part number.
2. Line 3:
 - "YYWW" is the last digit of the year and week that the part was assembled.
 - # denotes the sequential lot number.
 - "\$" denotes the mark code.

14. Ordering Information

Orderable Part Number [a][b]	Package	Carrier Type	Temperature
5P49V6968AdddNDGI	6 × 6 mm 48-VFQFPN	Tray	-40° to +85°C
5P49V6968AdddNDGI8	6 × 6 mm 48-VFQFPN	Tape and Reel	-40° to +85°C
5P49V6968A000NDGI	6 × 6 mm 48-VFQFPN	Tray	-40° to +85°C
5P49V6968A000NDGI8	6 × 6 mm 48-VFQFPN	Tape and Reel	-40° to +85°C

[a] "ddd" denotes factory programmed configurations based on required settings. Please contact factory for factory programming.

[b] "000" denotes un-programmed parts for user customization.

15. Revision History

Revision Date	Description of Change
March 16, 2018	Updated Current Consumption, AC Timing, LVDS, and CMOS electrical tables.
December 12, 2017	Initial release.



Corporate Headquarters
 6024 Silver Creek Valley Road
 San Jose, CA 95138
www.IDT.com

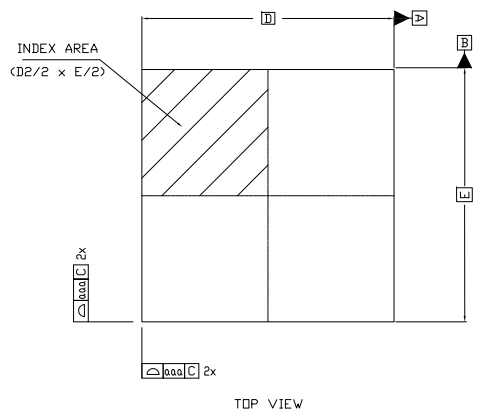
Sales
 1-800-345-7015 or 408-284-8200
 Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

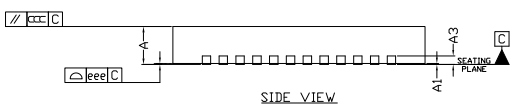
DISCLAIMER Integrated Device Technology, Inc. (IDT) and its affiliated companies (herein referred to as "IDT") reserve the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

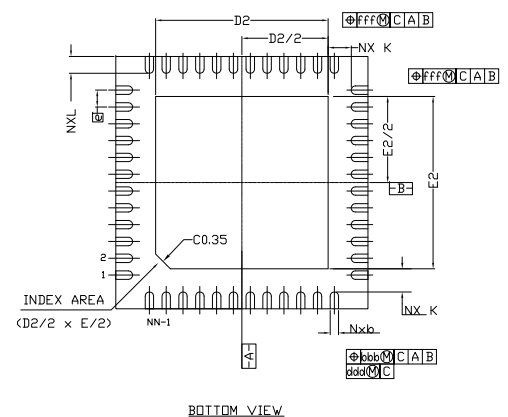
Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit www.idt.com/go/glossary. All contents of this document are copyright of Integrated Device Technology, Inc. All rights reserved.



TOP VIEW



SIDE VIEW




BOTTOM VIEW

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/06/16	JH
01	ADD CHAMFER	09/14/16	JH

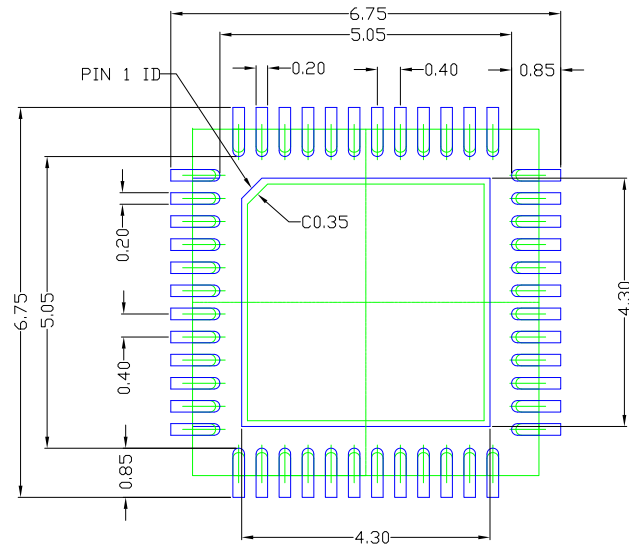
SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	4.10	4.20	4.30
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
K	0.50 REF.		
D	6.00 BSC.		
E	6.00 BSC.		
e	0.40 BSC.		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 REF	---
N	48		
ND	12		
NE	12		
b	0.15	0.20	0.25
TOLERANCE of FORM & POSITION			
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

TOLERANCES UNLESS SPECIFIED		 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com
DECIMAL	ANGULAR	
X±	±1°	TITLE ND/NDG 48 PACKAGE OUTLINE 6.0 x 6.0 mm BODY 0.40 mm PITCH QFN
XX±		
XXX±		
APPROVALS	DATE	SIZE C DRAWING No. PSC-4212-02 REV 01
DRAWN <i>oac</i>	01/06/16	
CHECKED		DO NOT SCALE DRAWING
		SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/06/16	JH
01	ADD CHAMFER	09/14/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±



6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

APPROVALS DATE
DRAWN *QAC* 01/06/16
CHECKED

TITLE ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY
0.40 mm PITCH QFN

SIZE C

DRAWING No. PSC-4212-02 REV 01

DO NOT SCALE DRAWING SHEET 2 OF 2