ULN2803A Darlington Transistor Arrays

1 Features

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications
- Compatible with ULN2800A Series

2 Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The ULN2803A device is a high-voltage, high-current Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

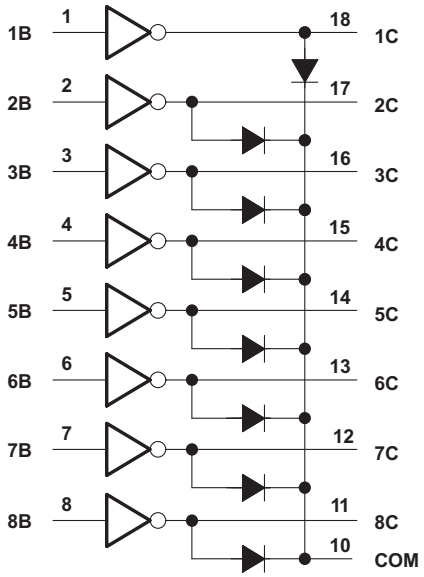
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A device has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
ULN2803	SOIC (18)	11.50 mm × 7.50 mm
	PDIP (18)	22.48 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematics



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5 Revision History

Changes from Revision F (January 2014) to Revision G **Page**

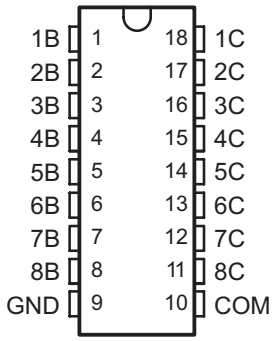
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision E (July 2006) to Revision F **Page**

- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1

6 Pin Configuration and Functions

DW OR N PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
<1:8>B	1 - 8	I	Channel 1 through 7 darlington base input
<1:8>C	18 - 11	O	Channel 1 through 7 darlington collector output
GND	7	—	Common Emmitter shared by all channels (typically tied to ground)
COM	8	I/O	Common cathode node for flyback diodes (required for inductive loads)

7 Specifications

7.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Collector-emitter voltage		50	V
	Input voltage(2)		30	V
	Peak collector current		500	mA
	Output clamp current		500	mA
	Total substrate-terminal current		–2.5	A
T_J	Operating virtual junction temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I		0	5	V
V_{CC}		0	50	V
T_J	Junction Temperature	-40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		ULN2803A		UNIT
		D	DW	
		18 PINS	18 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	29.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.9	33.0	
ψ_{JT}	Junction-to-top characterization parameter	10.9	6.0	
ψ_{JB}	Junction-to-board characterization parameter	38.7	32.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at T_A = 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		ULN2803A			UNIT
				MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, see Figure 4	I_I = 0			50	µA
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA, see Figure 5	50	65		µA
$I_{I(on)}$	Input current	V_I = 3.85 V,	See Figure 6		0.93	1.35	mA
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see Figure 7	I_C = 200 mA			2.4	V
			I_C = 250 mA			2.7	
			I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, see Figure 8	I_C = 100 mA		0.9	1.1	V
		I_I = 350 µA, see Figure 8	I_C = 200 mA		1	1.3	
		I_I = 500 µA, see Figure 8	I_C = 350 mA		1.3	1.6	
I_R	Clamp diode reverse current	V_R = 50 V,	see Figure 9			50	µA
V_F	Clamp diode forward voltage	I_F = 350 mA	see Figure 10		1.7	2	V
C_i	Input capacitance	V_I = 0,	f = 1 MHz		15	25	pF

7.6 Switching Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω, See Figure 11		130		ns
t_{PHL}	Propagation delay time, high- to low-level output			20		
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 12	V_S – 20			mV

7.7 Typical Characteristics

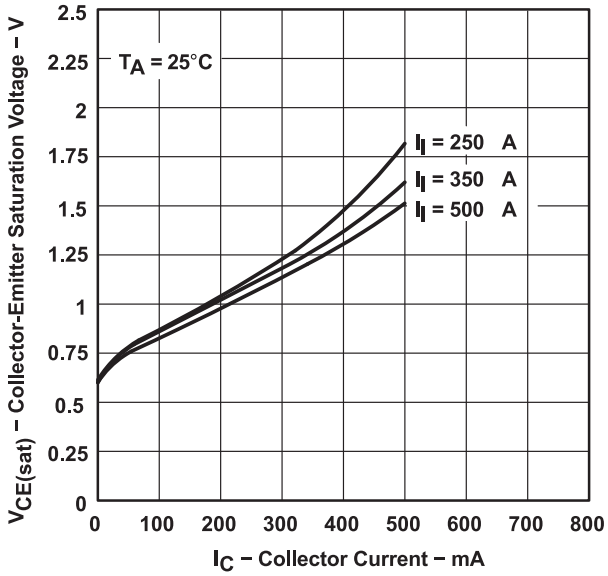


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

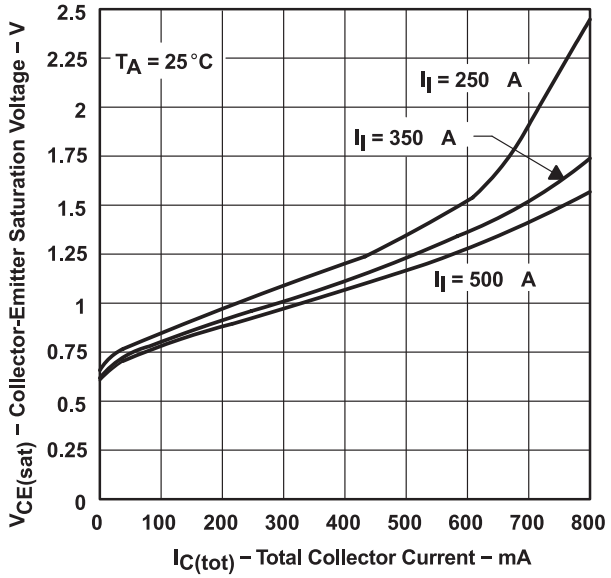


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

Typical Characteristics (continued)

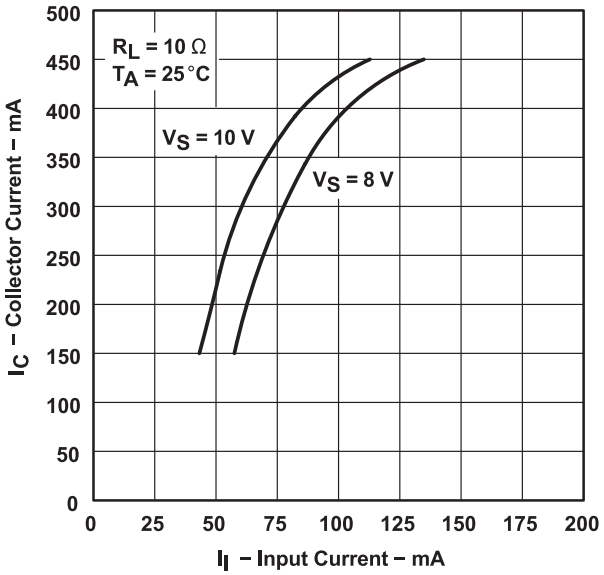


Figure 3. Output Current vs Input Current

8 Parameter Measurement Information

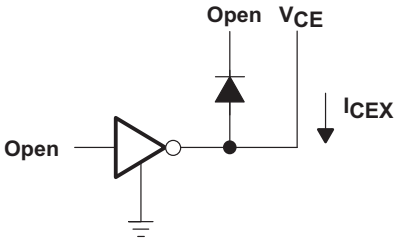


Figure 4. I_{CEX} Test Circuit

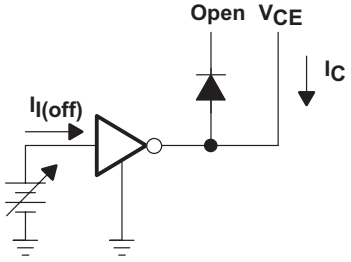


Figure 5. $I_{I(off)}$ Test Circuit

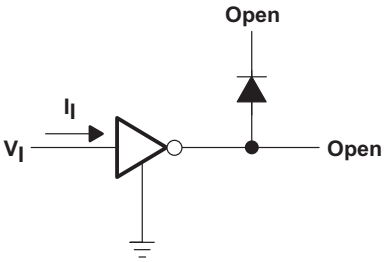


Figure 6. $I_{I(on)}$ Test Circuit

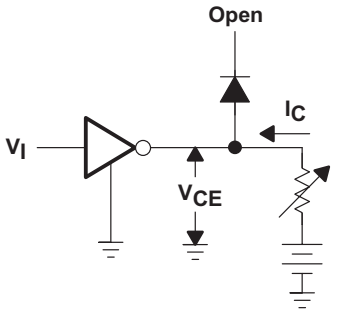


Figure 7. $V_{I(on)}$ Test Circuit

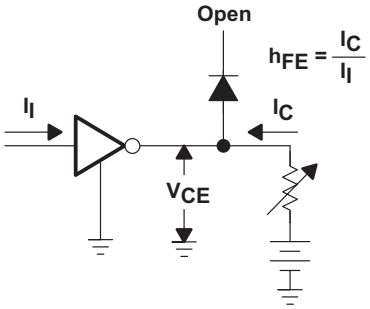


Figure 8. h_{FE}, $V_{CE(sat)}$ Test Circuit

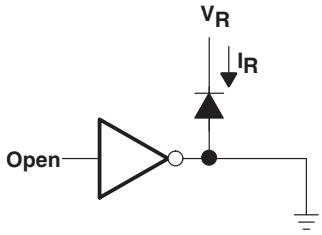


Figure 9. I_R Test Circuit

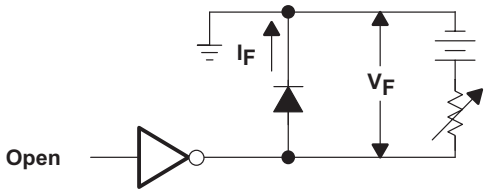
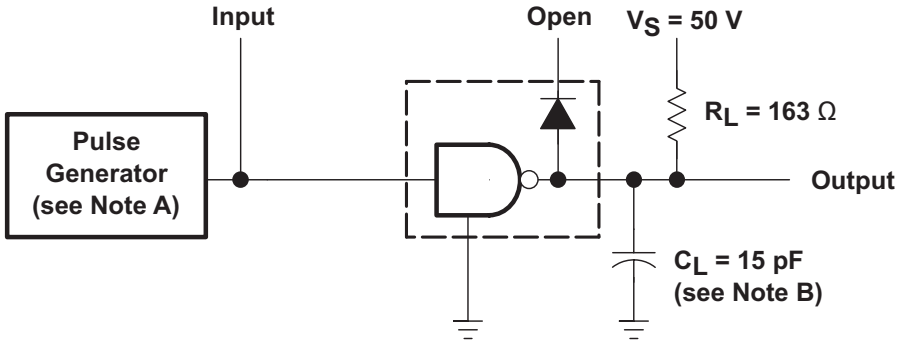
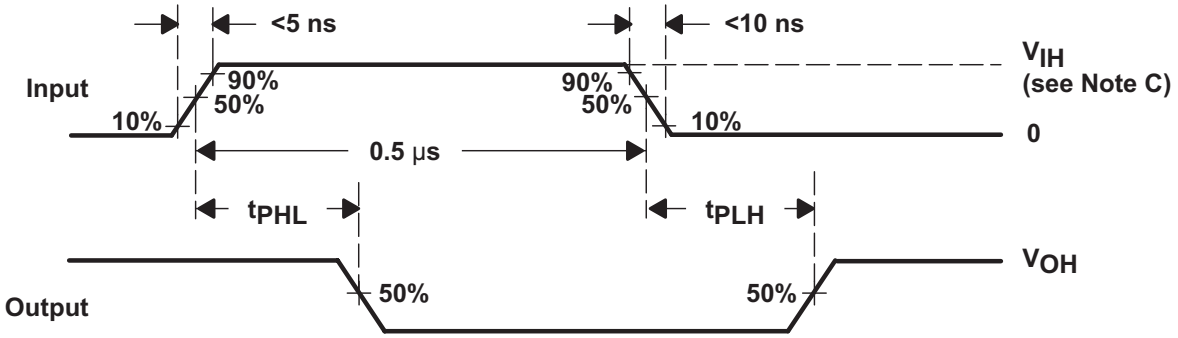


Figure 10. V_F Test Circuit

Parameter Measurement Information (continued)



Test Circuit



Voltage Waveforms

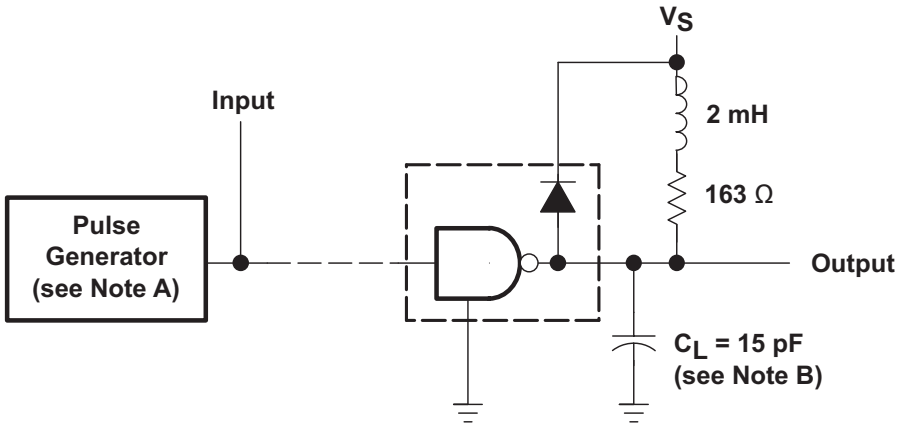
A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

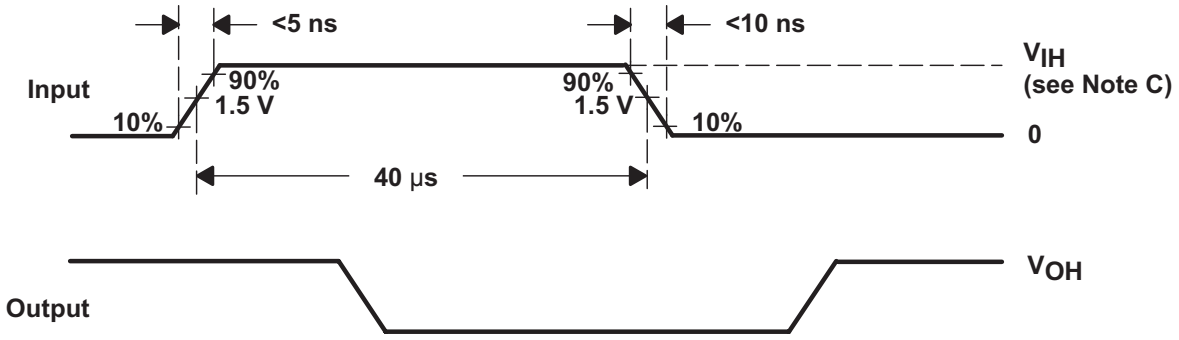
C. V_{IH} = 3 V

Figure 11. Propagation Delay-Times

Parameter Measurement Information (continued)



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. V_{IH} = 3 V

Figure 12. Latch-Up Test

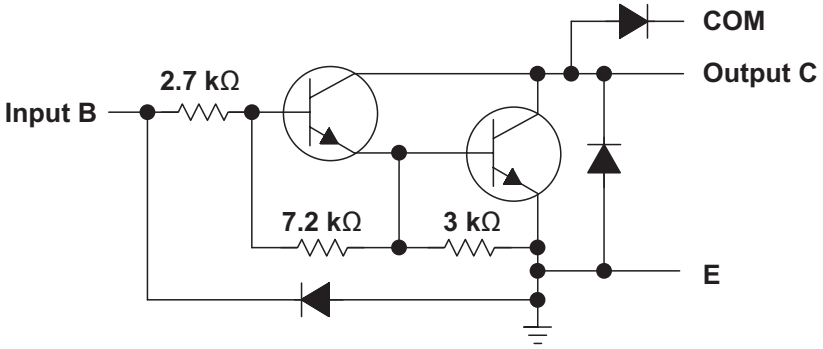
9 Detailed Description

9.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 8 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803A comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803A has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V or 3.3 V. The ULN2803A offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

9.2 Functional Block Diagram



9.3 Feature Description

Each channel of ULN2803A consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current via the 2.7 kΩ resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2 kΩ & 3.0 kΩ resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply via the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

9.4 Device Functional Modes

9.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2803A is able to drive inductive loads and supress the kick-back voltage via the internal free wheeling diodes.

9.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for ULN2803A to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

ULN2803A will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803A, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in Figure 13.

10.2 Typical Application

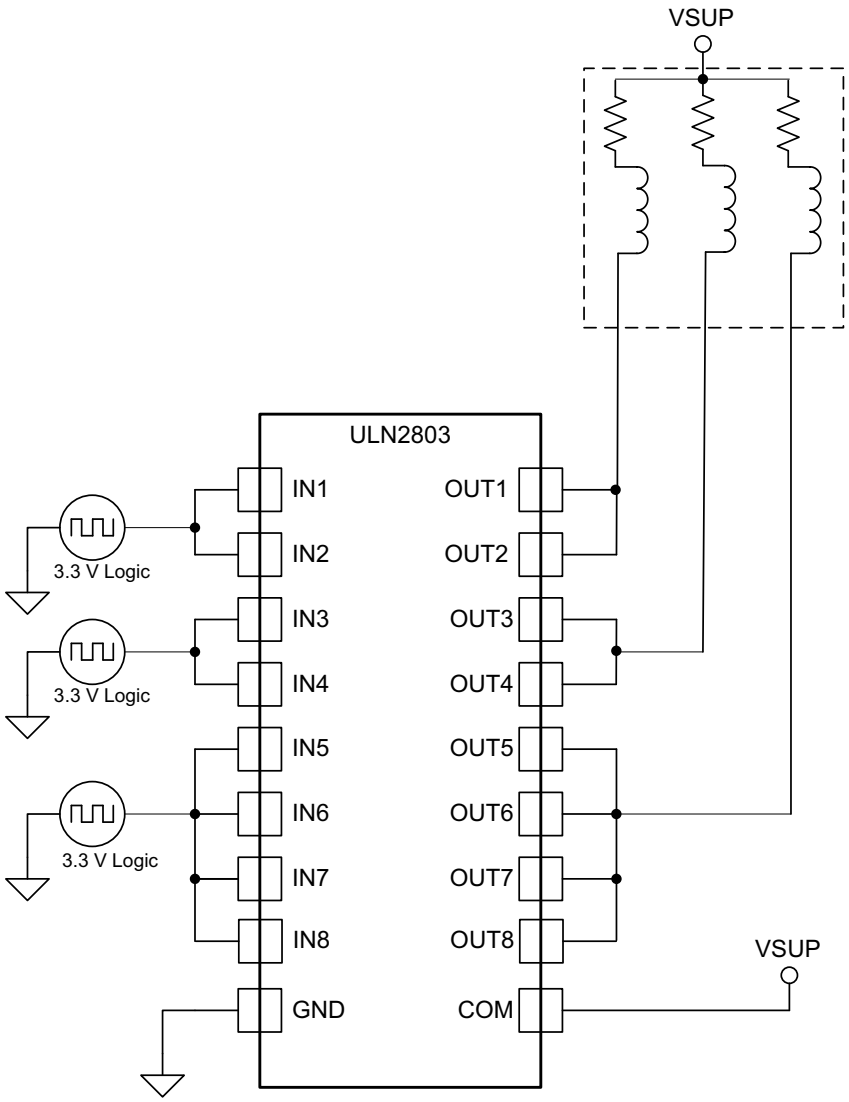


Figure 13. ULN2803A as Inductive Load Driver

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO Voltage	3.3 V or 5.0 V
Coil Supply Voltage	12 V to 100 V
Number of Channels	8
Output Current (R_{COIL})	20 mA to 300 mA per channel
Duty Cycle	100%

10.2.2 Detailed Design Procedure

When using ULN2803A in a coil driving application, determine the following:

- Input Voltage Range
- Temperature Range
- Output & Drive Current
- Power Dissipation

10.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance & output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

10.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by, Figure 1, Figure 2, or *Electrical Characteristics*.

10.2.2.3 Power Dissipation & Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use the below equation to calculate ULN2803A on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (2)

In order to guarantee reliability of ULN2803A and the system the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by below equation Equation 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA}$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance. (3)

It is recommended to limit ULN2803A IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

10.2.3 Application Curves

The following curves were generated with ULN2803A driving an OMRON G5NB relay – V_{in} = 5.0V; V_{sup}= 12 V & R_{COIL}= 2.8 kΩ

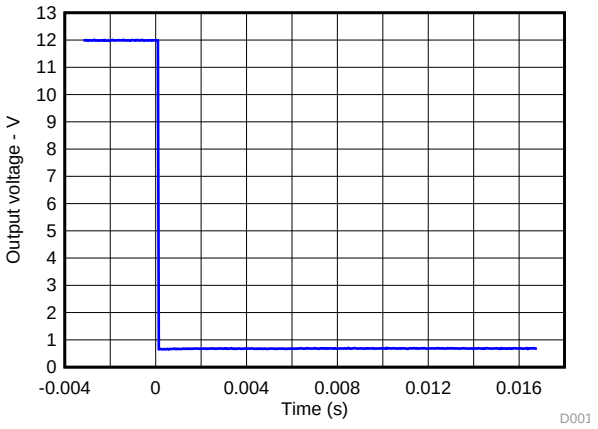


Figure 14. Output Response with Activation of Coil (Turn On)

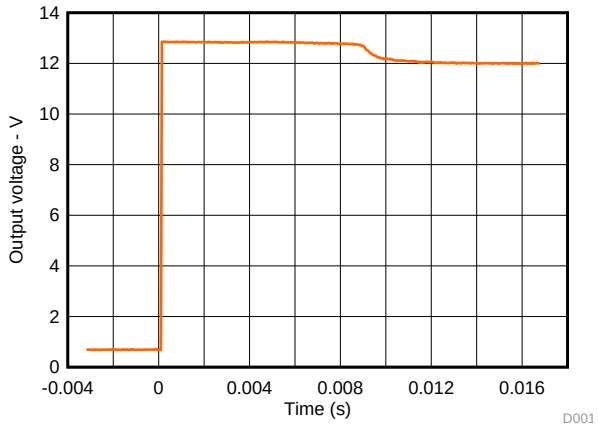


Figure 15. Output Response with De-activation of Coil (Turn Off)

11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803A. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

12.2 Layout Example

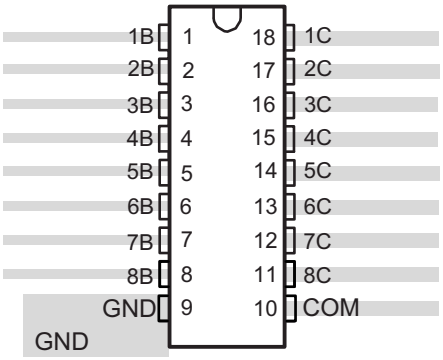


Figure 16. Package Layout

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2803ADW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803ADWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803ADWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803ADWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803AN	LIFEBUY	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	ULN2803AN	
ULN2803AN-P	LIFEBUY	PDIP	N	18		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	ULN2803AN	
ULN2803ANE4	LIFEBUY	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	ULN2803AN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

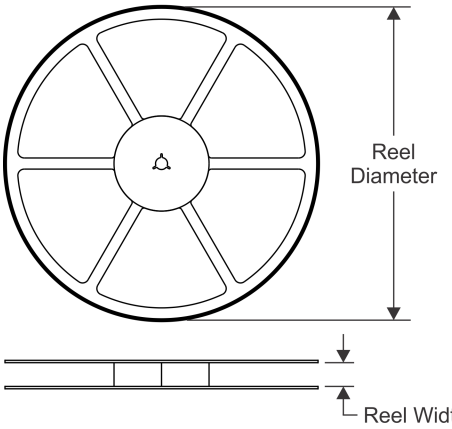
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

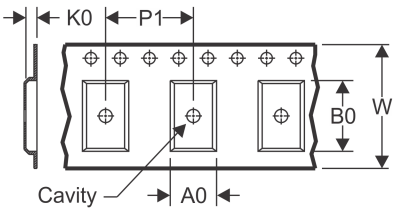
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

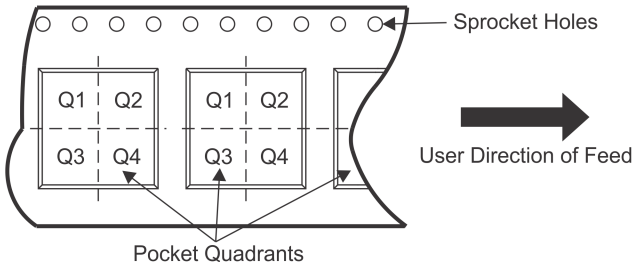


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

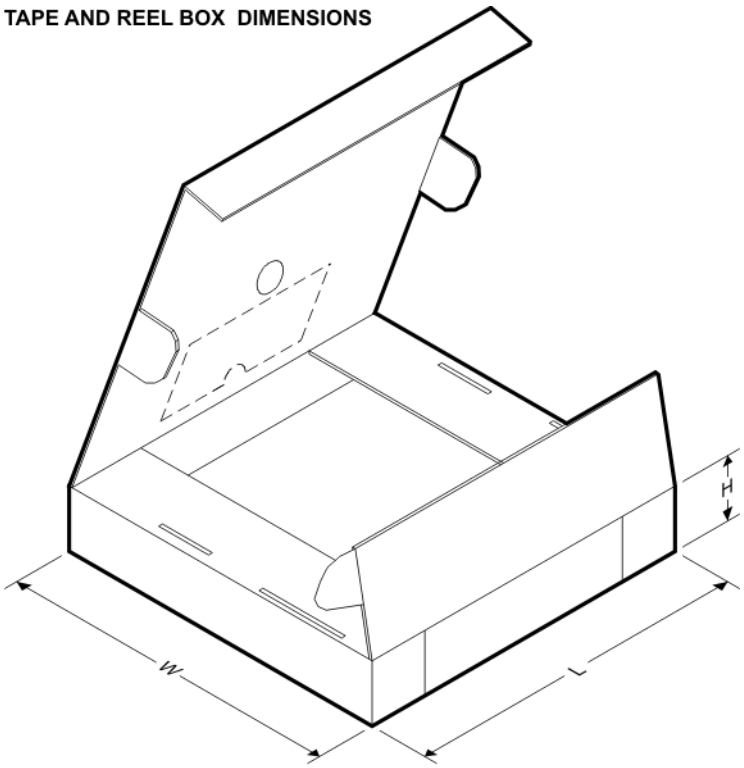
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2803ADWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

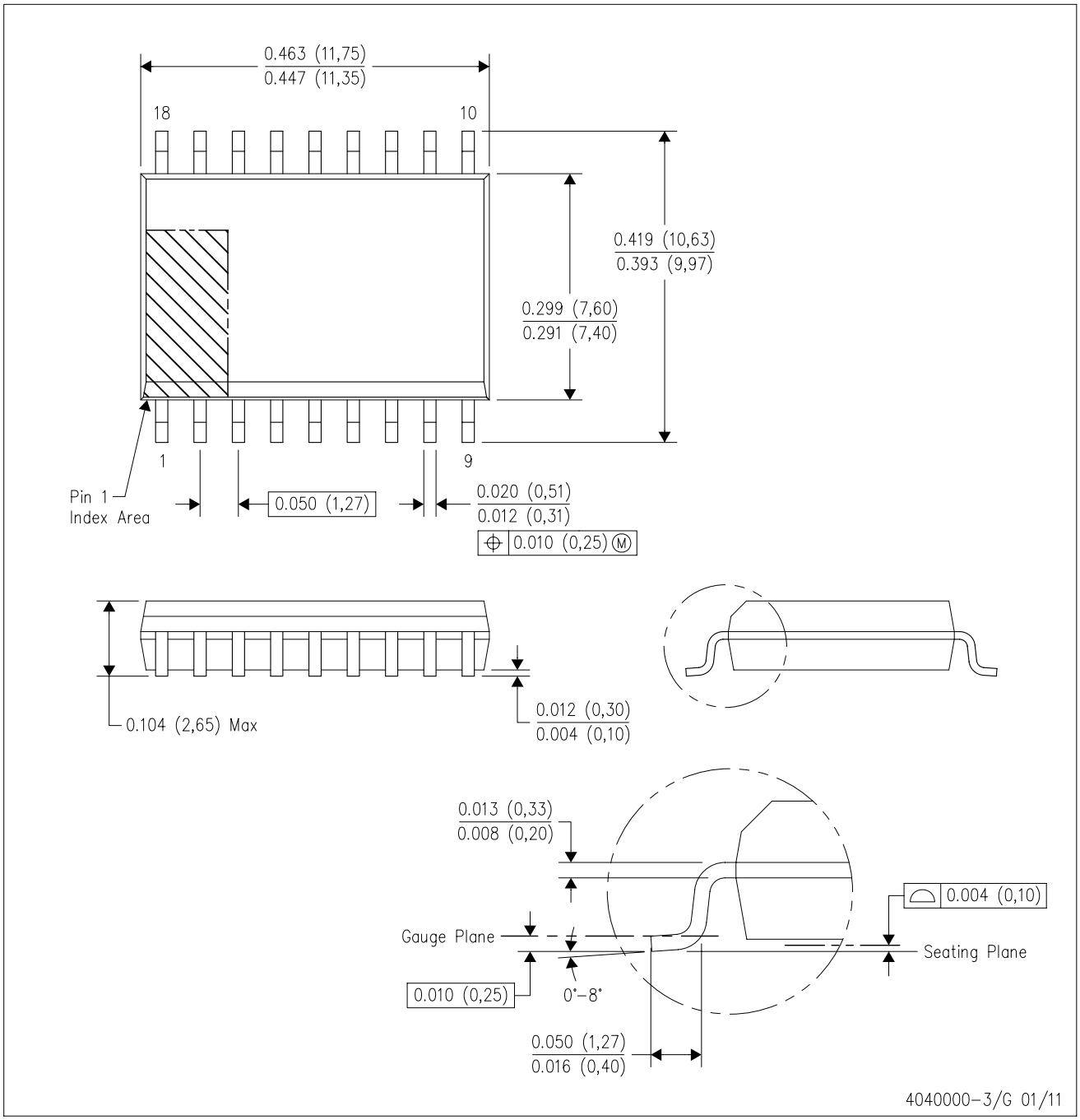
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

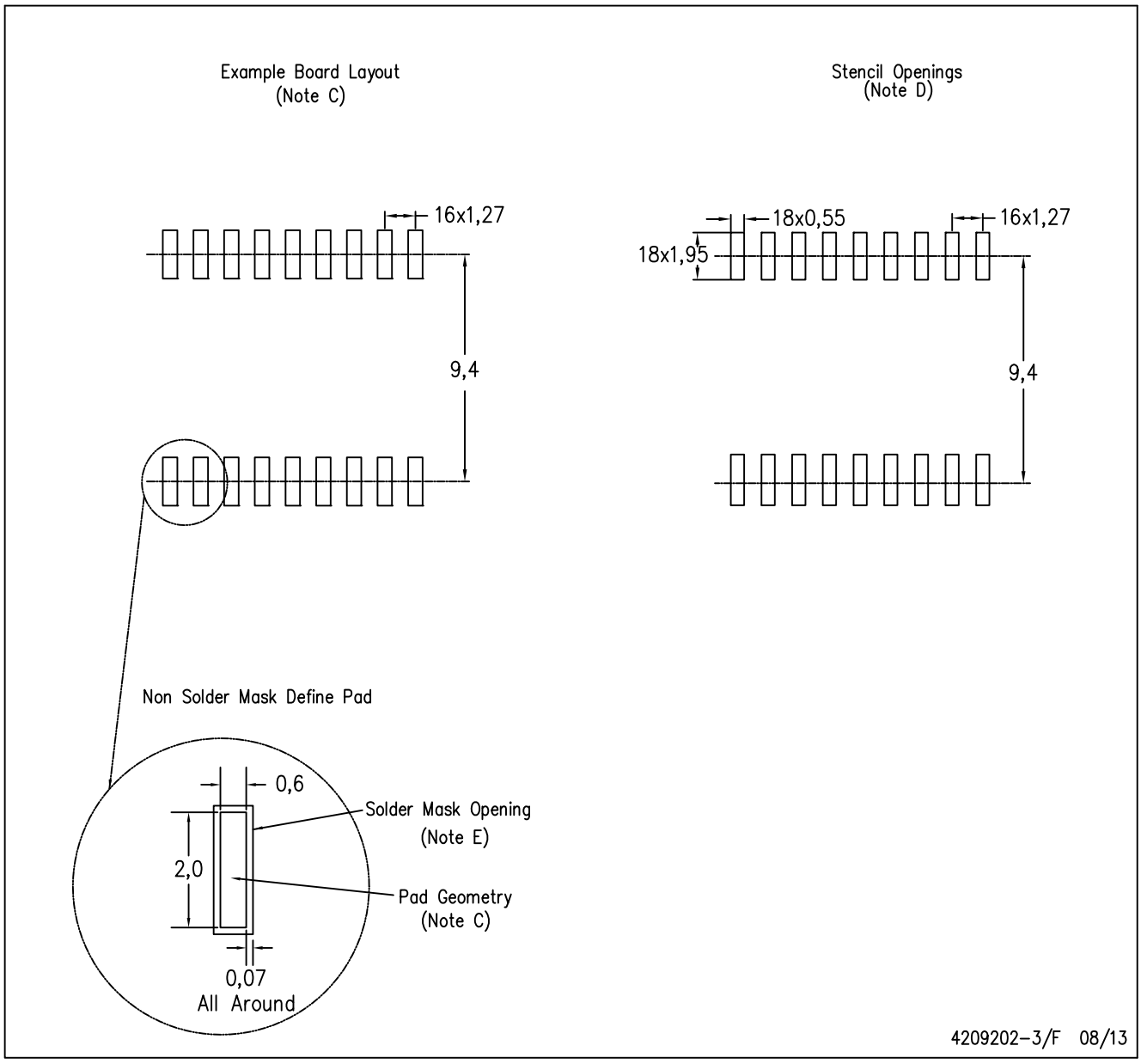
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2803ADWR	SOIC	DW	18	2000	370.0	355.0	55.0

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.