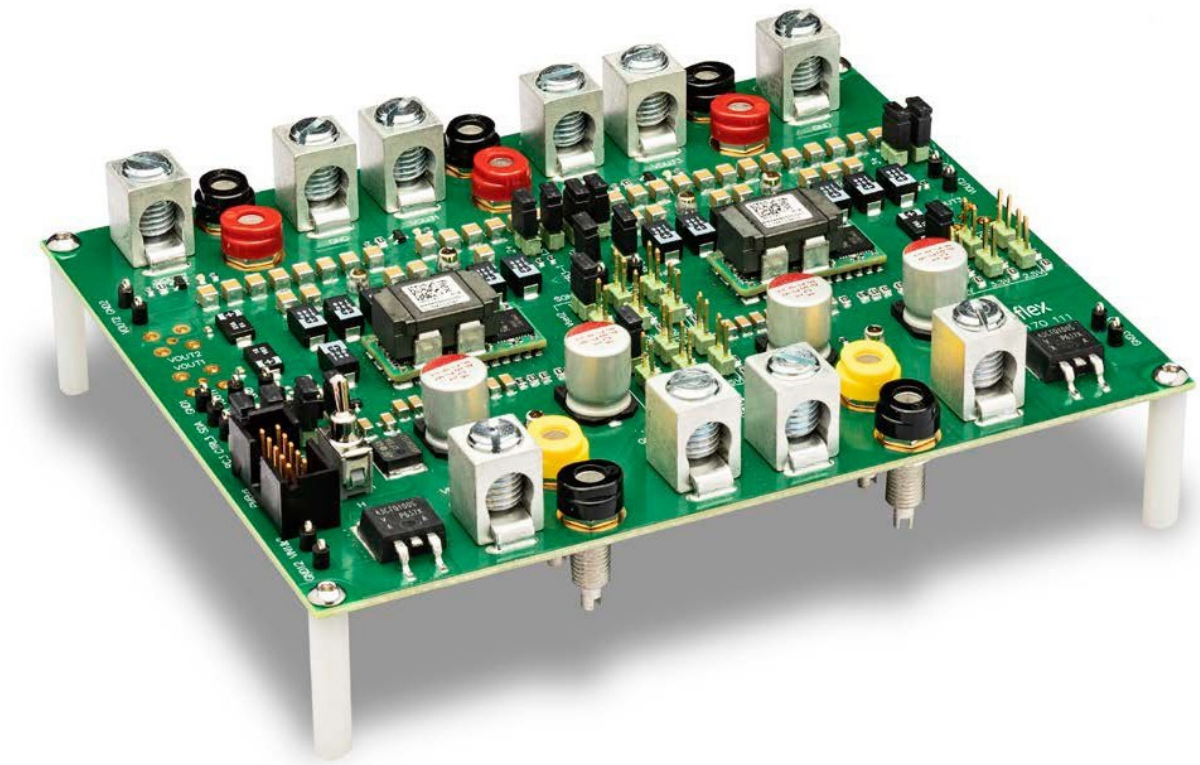
POL BMR469 Evaluation Board

ROA 170 111

User Guide



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1 Introduction

This User Guide provides a brief introduction and instruction on how to use the Reference Board ROA 170 111. This board facilitates evaluation of a BMR469 module configured either as a single output, or as a dual output device. It is also possible to use the board to evaluate both single output and dual output configured devices simultaneously.

The User Guide also provides a description of how the layout guidelines provided in the BMR 469 Technical Specification have been applied to the Reference Board layout.

Ordering information

Part Number	Product	General Information
ROA170111	BMR4690000/001 evaluation board	One module with dual output configuration and one module with single output configuration.
ROA170111/1	BMR4696001/001 evaluation board	

1.1 How to contact Flex

For general questions or interest in our products, please contact your local sales representative. Contact details are available from our website:
www.flex.com/powermodules

1.2 Prerequisites

In order to operate the ROA 170 111 board the following is needed:

- DC power supply 7.5-14 V.
- USB-PMBus adapter Flex KEP 910 17. It is only needed when the PMBus shall be used.
- The “Flex Power Designer” software package and a compatible Windows PC. Users must be familiar with the Windows® operating system.

2 Reference Board ROA 170 111

Power the board by connecting 7.5-14 V DC power to the “Vin” and “GND” connectors.

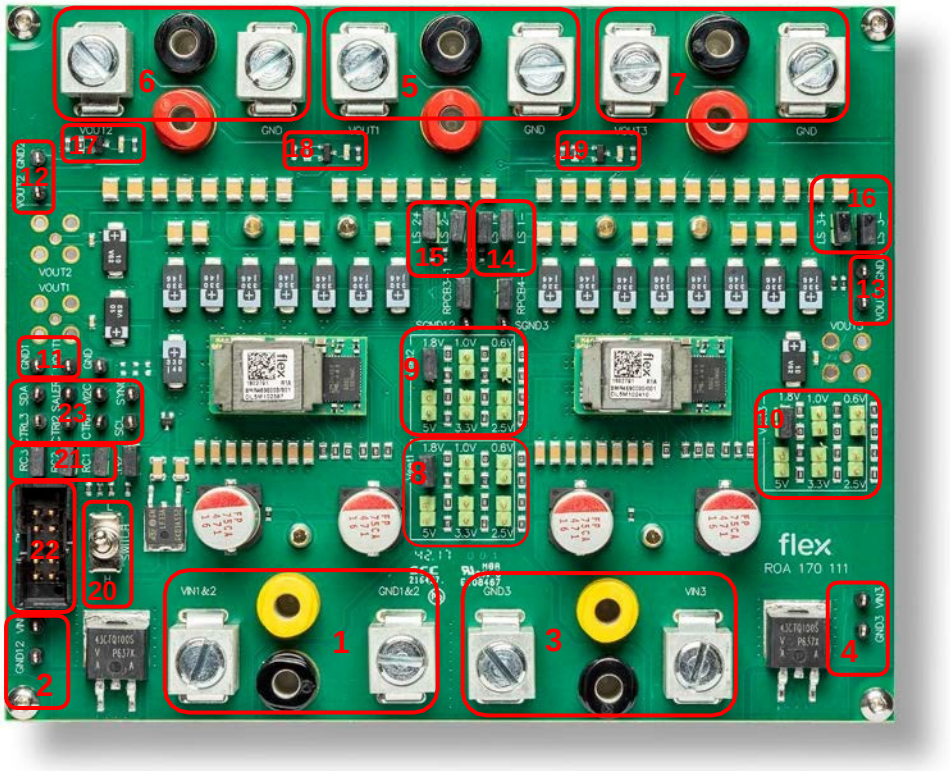

Figure 2.1 Top side of the reference board ROA 170 111.

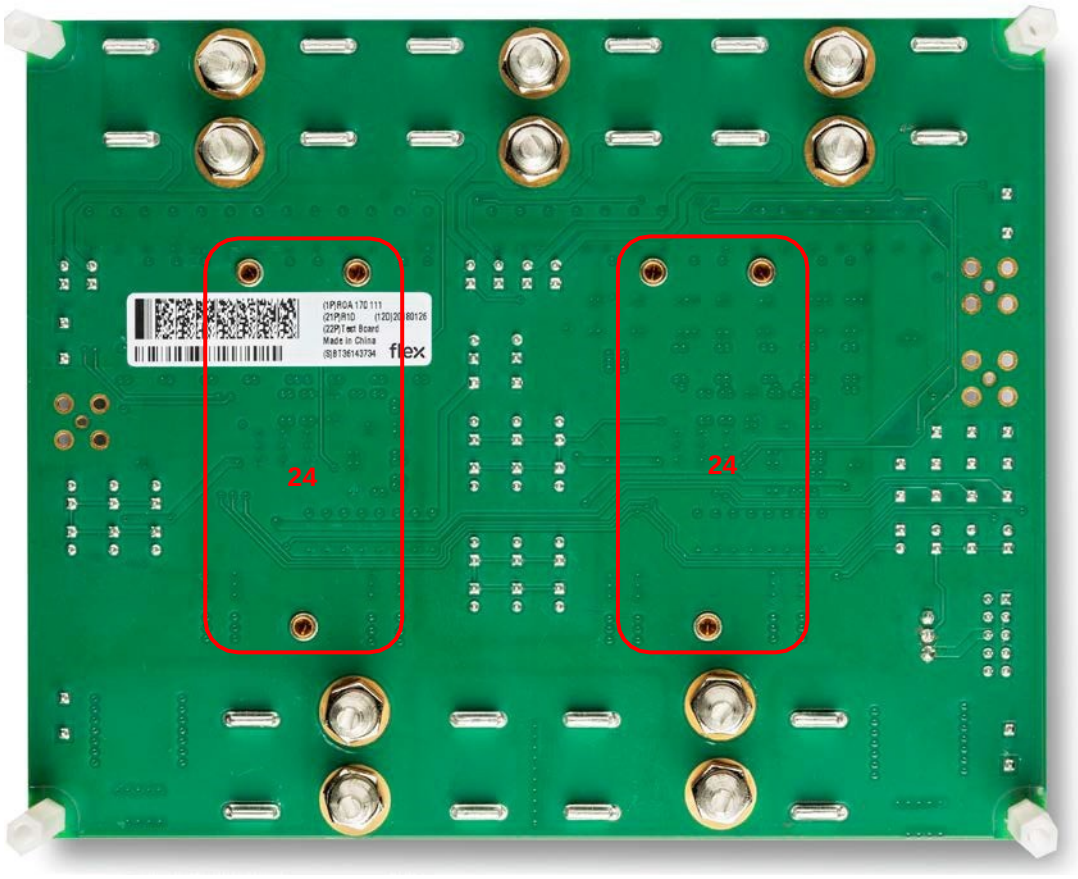

Figure 2.2 Bottom side of the reference board ROA 170 111.

Position Description

1 Input voltage connectors, VIN1&2/GND1&2

2 Input voltage sense points, VIN1&2/ GND12

3 Input voltage connectors, VIN3/GND3

4 Input voltage sense points, VIN3/GND3

5 Output 1 voltage connectors, VOUT1/GND

6 Output 2 voltage connectors, VOUT2/GND

7 Output 3 voltage connectors, VOUT3/GND

8 Output 1 voltage setting, Vset1

9 Output 2 voltage setting, Vset2

10 Output 3 voltage setting, Vset3

11 Output 1 efficiency test points, VOUT1/GND1

12 Output 2 efficiency test points, VOUT2/GND2

13 Output 3 efficiency test points, VOUT3/GND3

14 Output 1 voltage sense pins LS 1+/LS 1-

15 Output 2 voltage sense pins LS 2+/LS 2-

16 Output 3 voltage sense pins LS 3+/LS 3-

17 Power good 1 LEDs, PG1

18 Power good 2 LEDs, PG2

19 Power good 3 LEDs, PG3

20 CONTROL switch, SWITCH

21 Control jumpers, RC1 RC2 and RC3

22 Connector for the Flex KEP 910 17 USB-PMBus adapter, PMBus

23 Test points, SCL, SDA, SALERT, VI2C, GND and CTRL1-3.

24 Positions for populating Flex electronic load module (ROA 128 5552).

3 USB-PMBus adapter

The USB-PMBus adapter used with this board is the Flex KEP 910 17.

3.1 Connection of Flex KEP 910 17 USB-PMBus adapter

Connect the Flex KEP 910 17 USB-PMBus adapter to the PMBus header, see Figure 3.1.

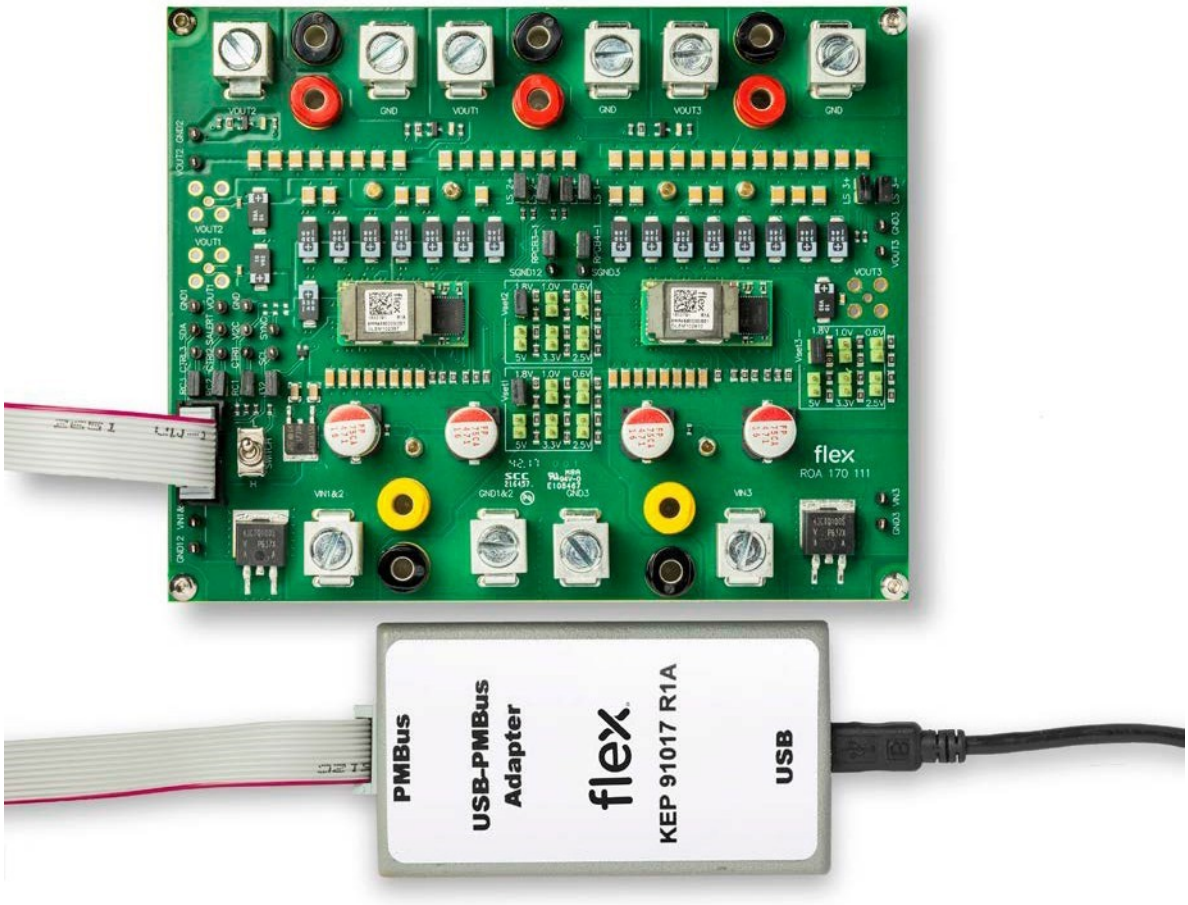

Figure 3.1 Connection of the Flex KEP 910 17 USB-PMBus adapter.

4 Power-up and Power-down Instructions

4.1 Power-up instruction

- The board is populated by default with two BMR 469 modules.

  - One module is configured as single output (Output 3)

  Place a jumper in the “Vset3” position for the desired output voltage

  - One module is configured as dual output (Output 1 and Output 2)

  Place a jumper in the “Vset1” position for the desired output voltage

  Place a jumper in the “Vset2” position for the desired output voltage

- Add the control jumpers to the RC1, RC2 and RC3. this will ensure that the 3 outputs will be enabled.
- Connect the PMBus Adapter/Cable to the board
- Connect the VIN1&2 and VIN3 connections to the DC power supply with a voltage setting in the range of 7.5 V to 14 V. Note that the module(s) can be started-up if enabled with input power even the PMBus adapter is not plugged-in.
- Turn the CONTROL switch in High position.
- Start the software program.
- The power good LEDs for each output should now give green light. The LEDs are controlled by PG output of each BMR469 module, but supplied from the USB-PMBus adapter. (For this reason, the LEDs will also give green light if the USB-PMBus adapter is connected).

Note: Make sure to populate a jumper to position J32. Otherwise the modules wound not start up.

4.2 Power-down instruction

- Turn the CONTROL switch in Low position or turn off the 7.5-14 V supply or disable with PMBus

4.3 RC instruction

ROA 170 111 supports both BMR 469 0000 and BMR 469 6001 module.
For BMR 469 0000, ROA170111, adding control jumpers to RC1, RC2 and RC3 enables corresponding output.
For BMR 469 6001, ROA170111/1, control of RC1 and RC2 is different.

- Put jumpers on RC1 and RC2, switch will control both Vo1 and Vo2 at the same time.
- To control Vo1 only, connect CTRL2 to GND2, add jumper to RC1 and leave RC2 open.
- To control Vo2 only, connect CTRL1 to GND1, add jumper to RC2 and leave RC1 open.

5 VSET and address resistors

5.1 Adjustment of VSET resistors

Place a jumper in each “Vset” position for the desired output voltage. The silk screen marking shows the voltage settings that can be achieved by populating jumpers. Note that the resistors in positions next to jumper pins can be replaced in order to change the predefined output voltages.

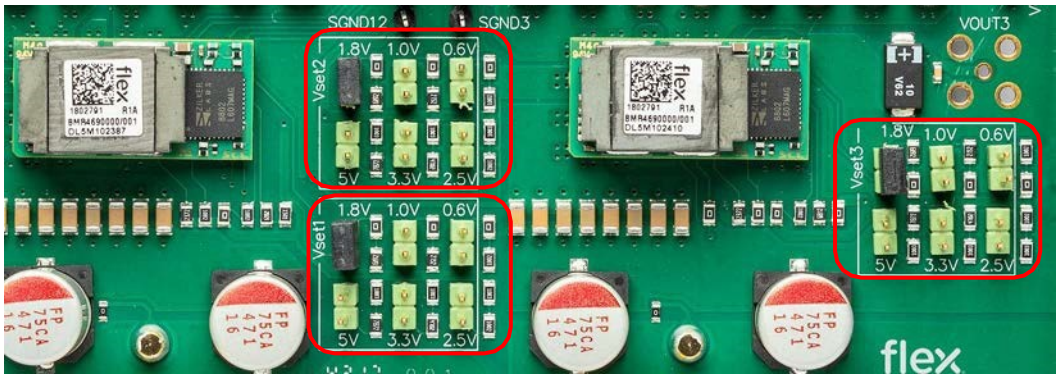

Figure 5.1 VSET1-3 resistors.

5.2 Adjustment of address resistors

To change the addresses, change the resistor values as shown in Figure 5.2.

Change resistors R_{SA12} and/or R_{SA3} to achieve the desired PMBus address for the modules. Refer to chapter “PMBus addressing” in the technical specification to select the values of R_{SA12} and R_{SA3}.

Note that each module must have its own unique address so a host can distinguish between the devices. Other pin-strap resistors setting, such as R_{CFG}, R_{SYNC} can refer to technical specification for more details.

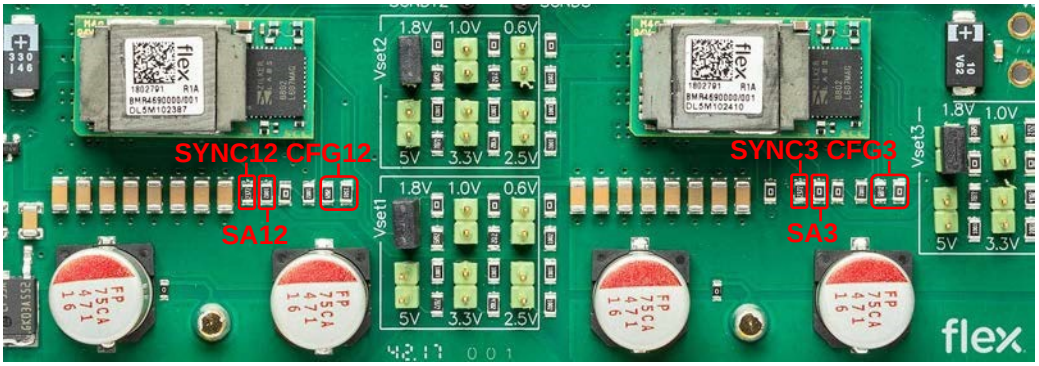

Figure 5.2 Pin-strap resistors.

6 Test Points

Input voltage should be measured at test points VIN1&2/GND12 and VIN3/GND3 which are connected directly to the VIN connectors of the board, see Fig. 6.1.

LS x+ and LS x- (load sampling point, x=1, 2 or 3) jumpers are connected to connectors VOUTx+ (x=1, 2 or 3) and GND respectively which are close to the load side. But the modules will use internal sense with reduced voltage accuracy if LS x+ and LS x- is not populated.

See the schematic of the board for more information.

Test points are provided for most signals according to printing on the test board.

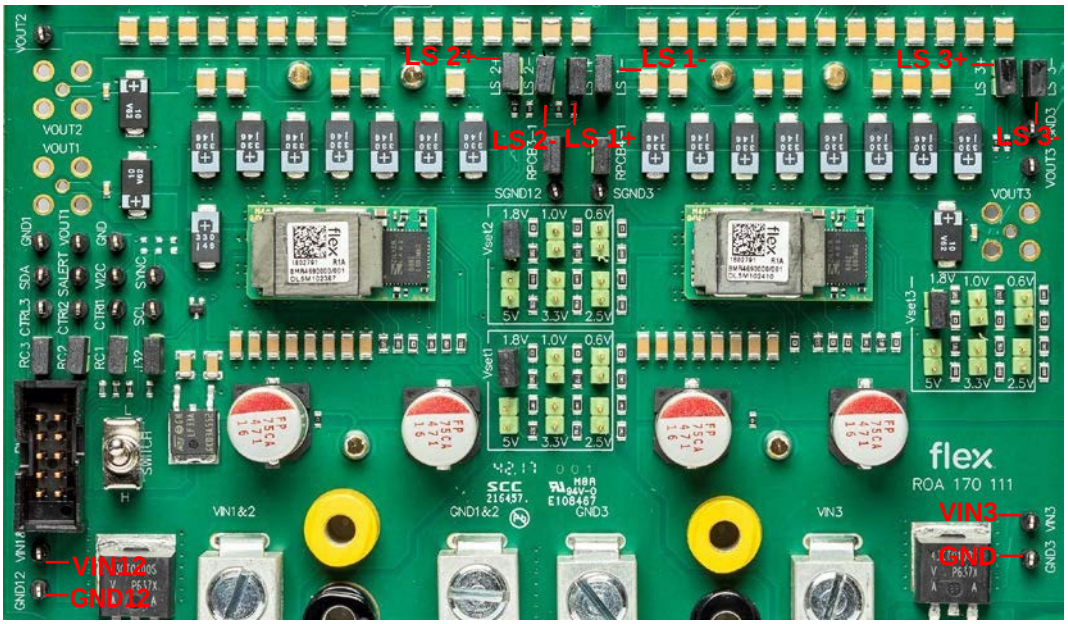

Figure 6.1 Sense points.

7 Layout Description

7.1 Layout description

The following sections describe how the layout guidelines provided in the BMR 469 Technical Specification have been applied to the Reference Board layout. The purpose is to give the reader a better understanding of the guidelines by examples. Please note that every system is different and that there may well be considerations to make which are not provided here, depending on the system requirements and limitations set in the end application.

7.2 PCB stack-up summary

Layer	Description	Thickness
Top layer	VIN12, VIN3, VOUT1-3, GND planes Component footprints, signal traces	105 µm / 3 oz
Layer 2	GND plane	105 µm / 3 oz
Layer 3	VIN12, VIN3, VOUT1-3 planes	105 µm / 3 oz
Layer 4	VIN12, VIN3, VOUT1-3 planes	105 µm / 3 oz
Layer 5	GND plane, sense traces	105 µm / 3 oz
Layer 6	VIN12, VIN3, VOUT1-3 planes	105 µm / 3 oz
Layer 7	GND plane	105 µm / 3 oz
Bottom layer	GND plane Component footprints, signal traces	105 µm / 3 oz

7.3 Power pins

Refer to Figure 7.1. The power pins (VIN, VOUT and GND) should connect with low impedance to internal power planes in order to:

- Provide effective heat spread from module to the application board.
- Provide low electrical impedance to input and output capacitors, minimizing the input and output ripple levels.
- Provide a low resistance path for input and output current of the module, lowering the resistive losses.

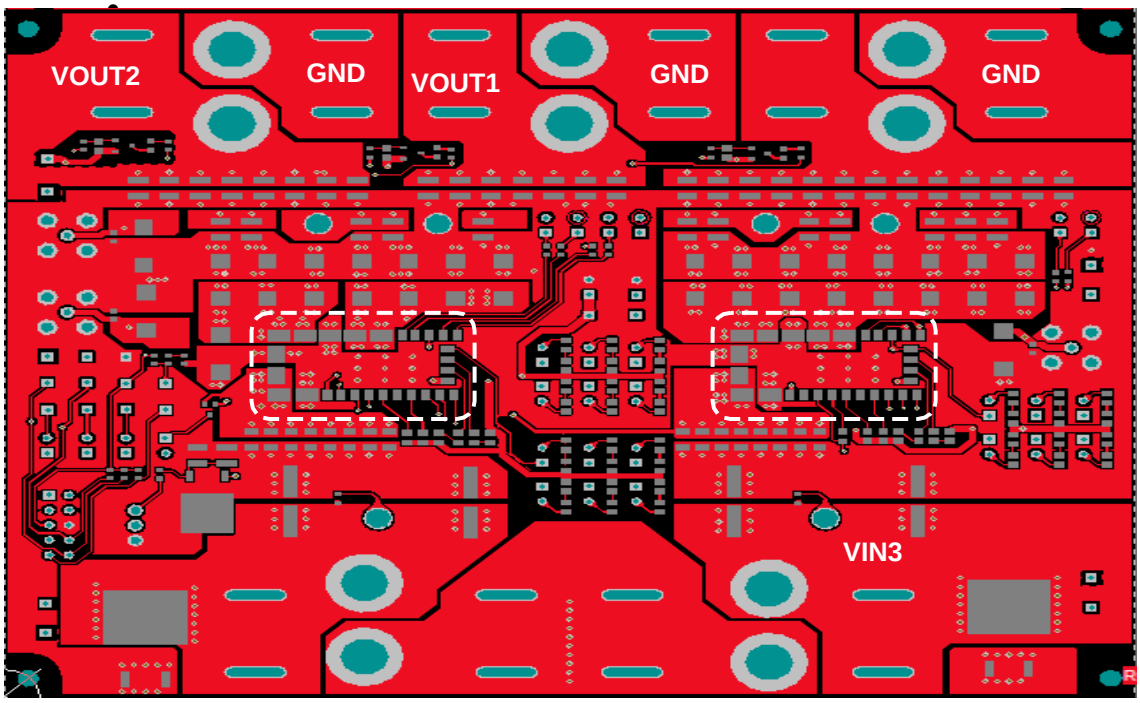

Figure 7.1. Top layer. Connection of power pins. BMR 469 in dashed areas.

This board is designed for box-pin modules which means the currents are quite effectively spread to the inner layers of the PCB. It is recommended to place multiple vias around the power pads on outer layers in order to provide good path for current and heat to the inner layers.

7.4 Input capacitance

Refer to Figure 7.2. The smaller ceramic input capacitors (used mainly to lower the input voltage ripple level) are placed close to the VIN/GND pins of the module in order to minimize the connection impedance. For the same reason multiple vias are placed close to the capacitors' terminals, utilizing also the inner layers to connect the capacitors to the input pins of the modules. An even better connection can be achieved by embedding the capacitor's terminals in the planes (no thermal clearance) and/or placing the vias directly in the terminal pads of the capacitors.

Note that ceramic input capacitors are also placed on the bottom side of the board, at the same locations as the ceramic capacitors shown in Figure 7.2.

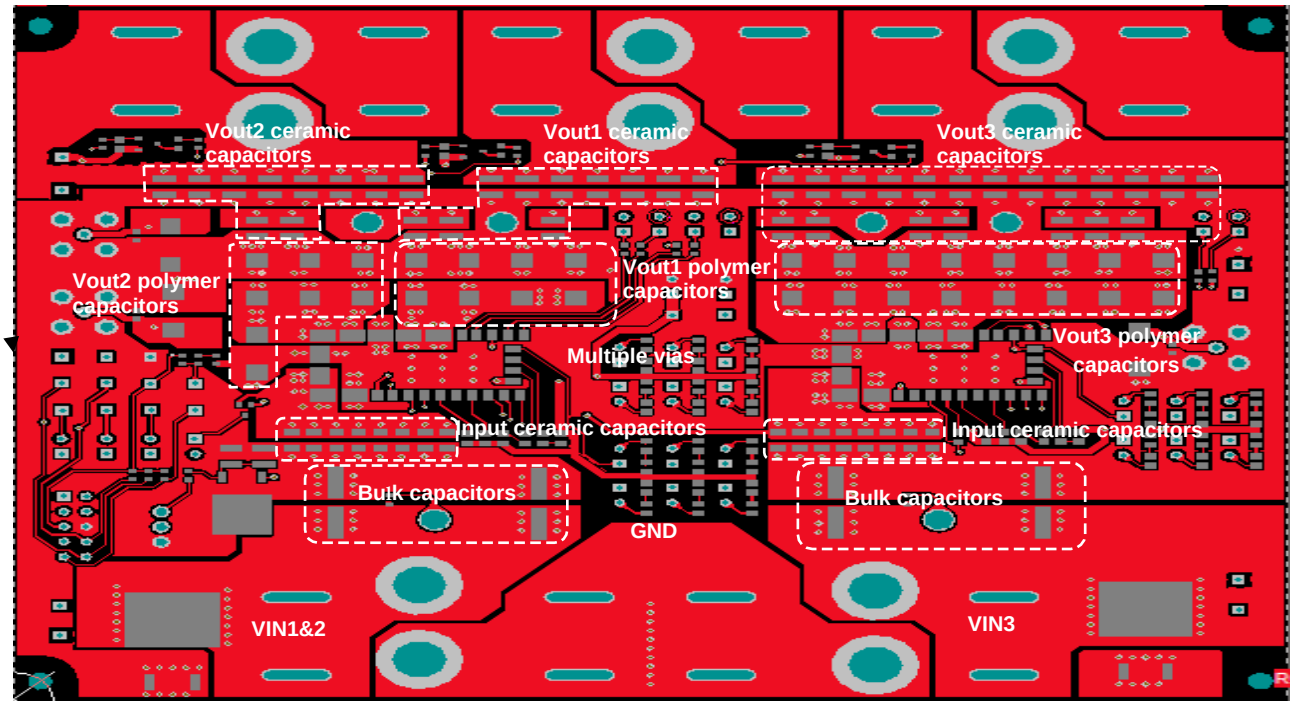

Figure 7.2. Top layer. Input and output capacitance in dashed areas.

Care should be taken when placing multiple vias regarding the fact that this could lead to large voids in the internal power planes, giving narrow passages for the large currents that may have to pass.

Placement and connections of the larger bulk input capacitor (used mainly to hold up the input voltage during large load transients or changes in input voltage) follows the rules of the ceramics described above. However, in this case low impedance is not as critical due to the slower action, so the capacitor can be placed “behind” the ceramic input capacitors at a larger distance from the module.

7.5 Output capacitance

Refer to Figure 7.2. Output capacitors are placed both close to module (to handle the module’s output ripple) and close to the load (to handle load transients), see application note AN321 for more details. In both cases it is important with low impedance connections (to module VOUT/GND pins or to the load’s VOUT/GND pins) and the guidelines described above for the input capacitors are applied.

Note that output capacitors are also placed on the bottom side of the board, at the same locations as the capacitors shown in Figure 7.2.

Further it is important to use planes to distribute the output current to the load in order to minimize losses and the effective output impedance, providing good conditions for the module’s control loop to compensate for load transient.

7.6 Sense traces

Refer to Figure 7.3 showing the sense traces routed on Top layer and Layer 2. The traces connect at VOUT/GND points close to the load in order to provide accurate regulation. Since regulation is sensitive to disturbances on the +S/-S inputs the wires are routed as a coupled pair all the way from load to the +S/-S pins. To further provide good signal integrity a solid ground follows the traces on an adjacent layer. In this layout the sense signals are routed through jumpers and resistors, in order to provide alternatives for sensing. This is only for testing purposes however and is normally not recommended in an end application.

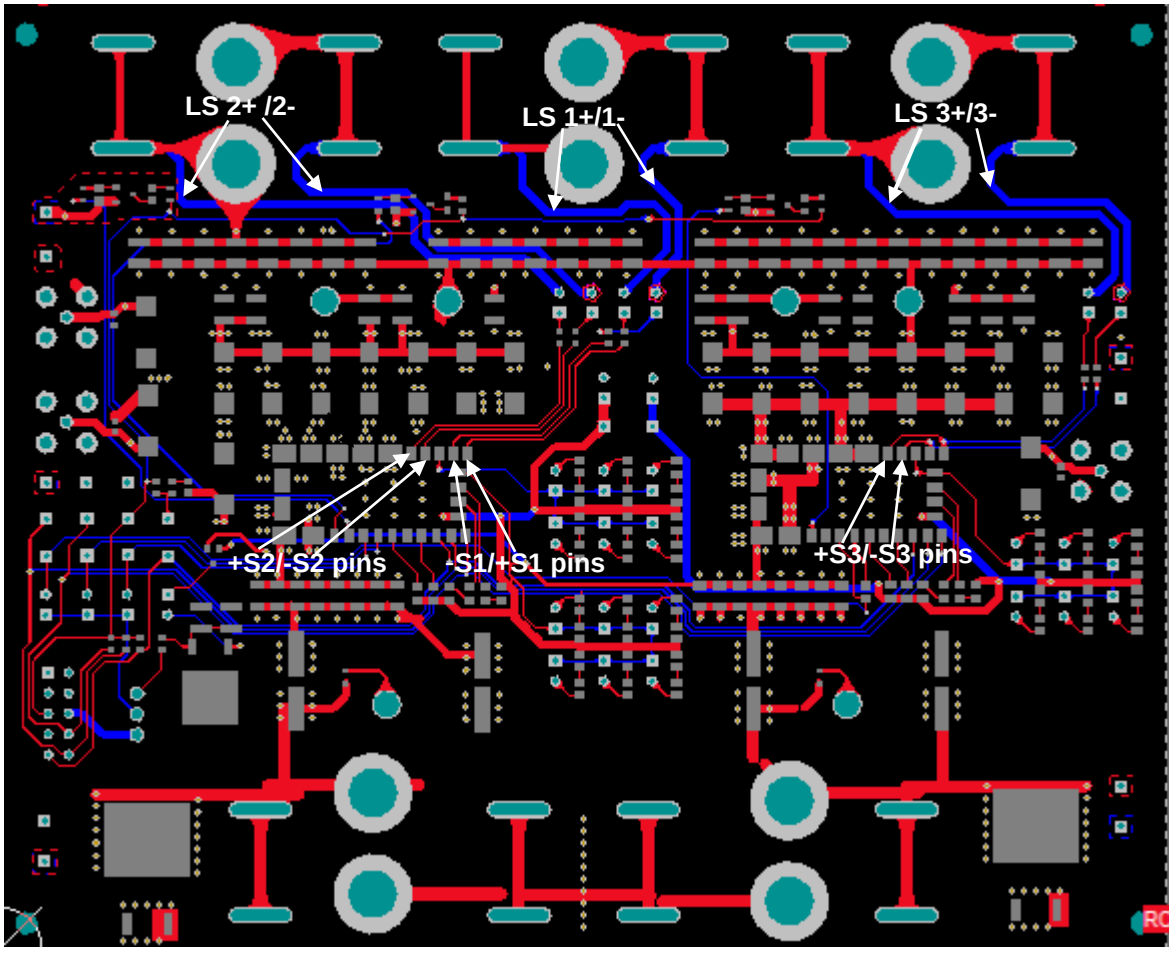

Figure 7.3. Top layer + Bot layer. Sense pair traces in dashed area.
(Red = Top layer, Blue = Bot layer)

7.7 Pin-strap resistors

Refer to Figure 7.4 showing the routing of the pin-strap resistors circuitry. To minimize capacitive load and provide good signal integrity, the resistors are placed with short traces close to the module and with a solid ground plane on an adjacent layer. Pin-strap reference PREF12 is signal ground for dual output and PREF 3 is signal ground for single output. Both can connect to GND via RPCB3-1 or RPCB4-1 on evaluation board. As GND and PREF are shorted together on BMR469 module inner PCB, it's not critical that how to connect PREF to GND on evaluation board.

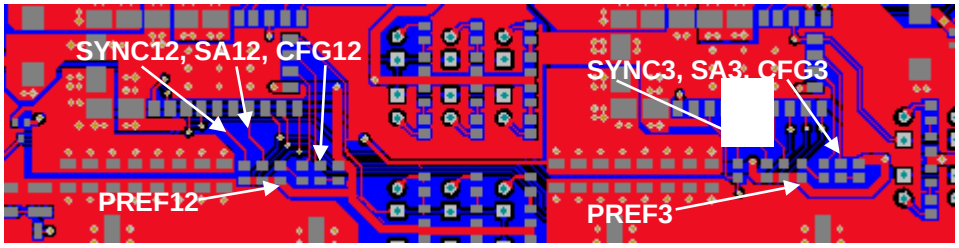

Figure 7.4. Top layer + Bot layer. Pin-strap resistors in dashed area.
(Red = Top layer, Blue= Bot layer)