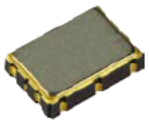
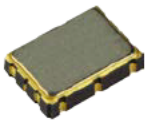
I²C-Bus Programmable Crystal Oscillator (SPXO)

Output: LV-PECL

SG-8506CA

Pb Free RoHS Compliant

Product Number
X1G005031xxxx00

- Frequency range : 50 MHz to 800 MHz
- Supply voltage : 2.5 V to 3.3 V
- External dimensions : 7.0 × 5.0 × 1.5 mm (8 pins)

Features
- User-specified one startup frequency, 7-bit I²C
- User Programming: I²C Interface
- High frequency fundamental tone crystal, Low jitter PLL technology
- Available field oscillator programmer "SG-Writer II"

Application
- OTN, BTS, Test Instrument

*The I2C-Bus is a trademark of NXP Semiconductors

Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	fo	50 MHz to 800 MHz	It can be changed by I²C
Supply voltage	V_{CC}	2.5 V - 0.125 V to 3.3 V + 0.33 V	-
Storage temperature	T_stg	-55 ºC to +125 ºC	Store as bare product after packing
Operating temperature	T_use	-40 ºC to +85 ºC	-
Frequency tolerance *1	f_tol	K : ±31.5 × 10^{-6}	Customized Product (Option)
		L : ±50 × 10^{-6}	
Current consumption	I_{CC}	90 mA Max.	OE Active, L_ECL=50 Ω
Disable current	I_dis	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode
		70 mA Max.	OE Inactive, Output Standby: Fix mode
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V_{OH}	Vcc - 1.025 V Min.	DC characteristics
	V_{OL}	Vcc - 1.62 V Max.	
Output load condition	L_ECL	50 Ω	Termination to Vcc - 2.0 V
Input voltage	V_{IH}	70% Vcc Min.	OE, SDA and SCL
	V_{IL}	30% Vcc Max.	
Rise time / Fall time	tr / tf	400 ps Max.	Between 20% and 80% of (V_{OH} - V_{OL})
Start-up time	t_str	10 ms Max.	Time at minimum supply voltage to be 0 s
Setting time for frequency change	t_{SET1}	1.5 ms Max.	From setting NEW_FREQ bit to output new frequency

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 ºC.

Product Name (Standard form): SG-8506 ① CA ② 156.2MHz ③ 0x37 ④ A ⑤ P ⑥ R ⑦ L ⑧ Z ⑨

① Model, ② Package type,
③ Power-on default output frequency (50 ~ 800 MHz), ④ I²C slave address, ⑤ Internal crystal frequency,
⑥ Output enable pin Polarity, ⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

⑤ Internal crystal frequency	
A	114.1444 MHz

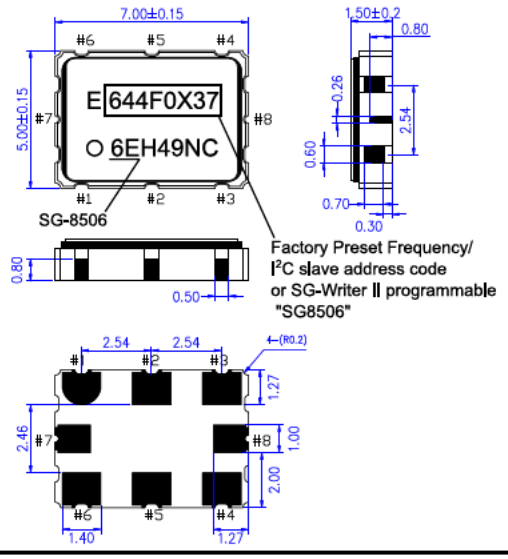
⑥ Output enable pin Polarity	
P	Active High
Q	Active Low

⑦ Supply voltage/ Output format	
R	2.5 V ~ 3.3 V/LVPECL

⑧ Frequency tolerance/ Operating temperature	
K	±31.5 × 10^{-6}/-40 to +85 °C
L	±50 × 10^{-6}/-40 to +85 °C

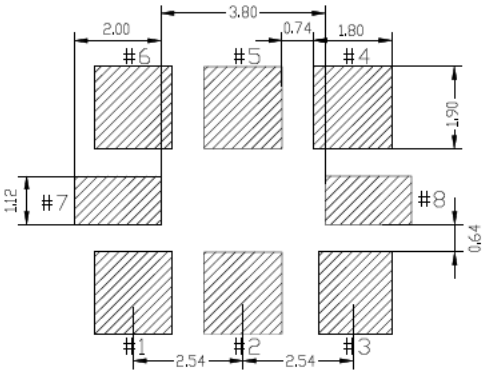
⑨ Output standby type	
F	Fix (OUT="L", OUTN="H")
Z	High-Z

External dimensions (Unit: mm)



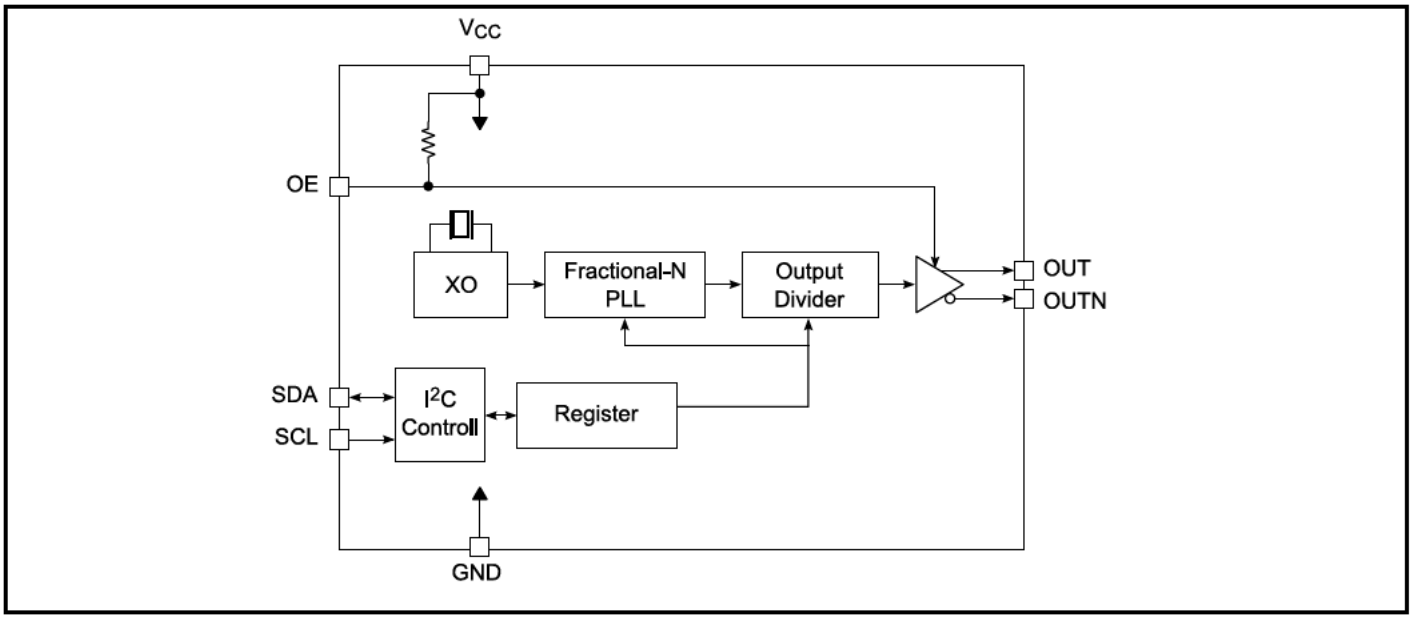
Pin	Connection
1	NC
2	OE
3	GND
4	OUT
5	OUTN
6	Vcc
7	SDA
8	SCL

Footprint (Recommended) (Unit: mm)

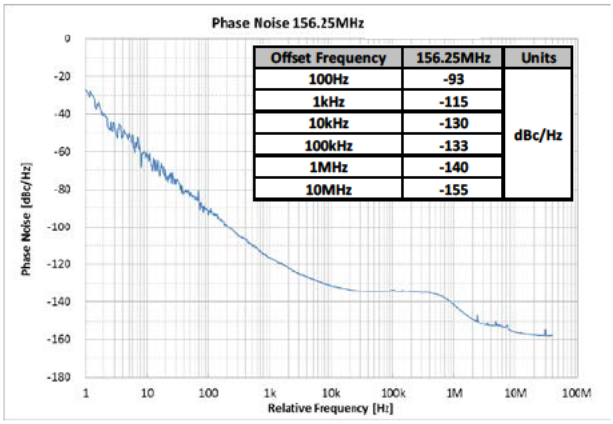


In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.

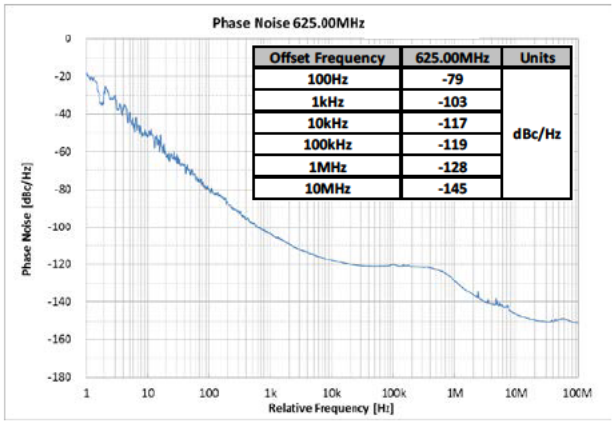
Block diagram



Phase Noise



Offset Frequency	156.25MHz	Units
100Hz	-93	dBc/Hz
1kHz	-115	
10kHz	-130	
100kHz	-133	
1MHz	-140	
10MHz	-155	



Offset Frequency	625.00MHz	Units
100Hz	-79	dBc/Hz
1kHz	-103	
10kHz	-117	
100kHz	-119	
1MHz	-128	
10MHz	-145	

Phase Jitter

	Offset Frequency	100.00 MHz	125.00 MHz	156.25 MHz	250.00 MHz	312.50 MHz	500.00 MHz	625.00 MHz
Phase jitter *2 Typ.	12 kHz to 20 MHz	0.31 ps	0.30 ps	0.26 ps	0.26 ps	0.29 ps	0.28 ps	0.29 ps

*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 µF + 10 µF) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.