# EPC2100 – Enhancement Mode GaN Power Transistor Half Bridge
# Preliminary Specification Sheet

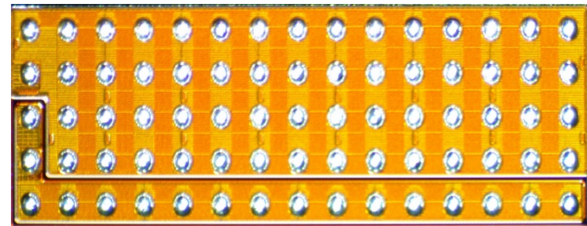
**Status: Engineering**

**Features:**

- 90% System Efficiency at 25 A
  - 12 $V_{IN}$ to 1.2$V_{OUT}$, 500 kHz
  - Includes output filter
- High Frequency Operation (Beyond 10 MHz)
- High Density Footprint
- Low Inductance Package
- Pb-Free (RoHS Compliant), Halogen Free

**Applications:**

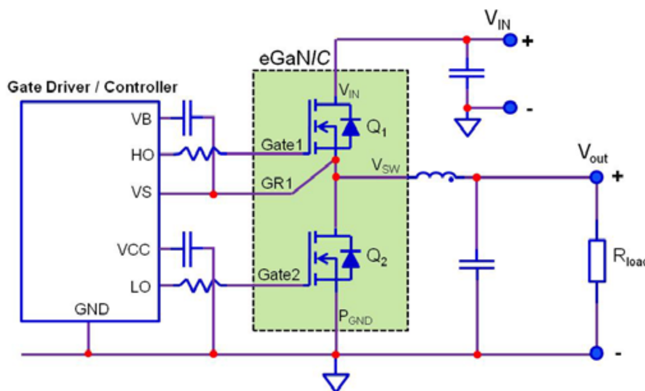
- High Frequency DC-DC Conversion
- Point-of-Load (POL) Converters



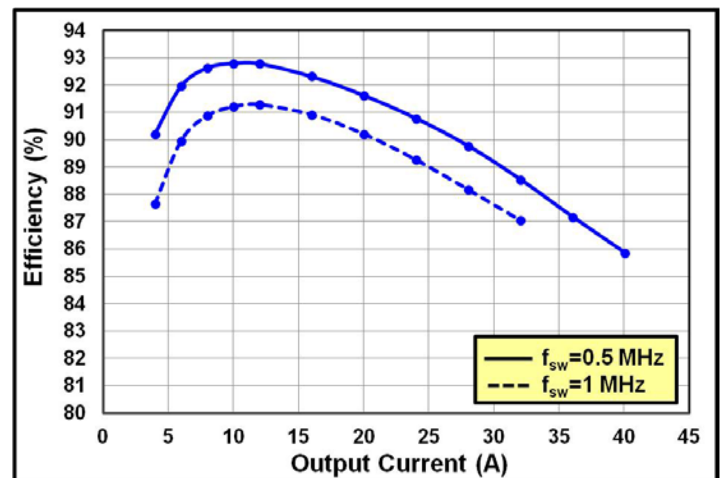
EPC2100 devices are supplied only in passivated die form with solder bars

Die Size: 6.05 mm x 2.3 mm

**Typical Circuit**




**Typical System Efficiency**




**MAXIMUM RATINGS**

| Parameter | | Value |
|---|---|---|
| Maximum Drain – Source Voltage ($V_{SW}$ to $P_{GND}$, $V_{IN}$ to $V_{SW}$) | | 30 V |
| Maximum Gate – Source Voltage Range (Gate 1 to $V_{SW}$, Gate 2 to $P_{GND}$) | | -4 V < $V_{GS}$ < 6 V |
| Continuous Drain Current, 25 °C | Q1 Control FET | 9.5 A |
| | Q2 Sync FET | 38 A |
| Maximum Pulsed Drain Current, 25 °C, $T_{pulse}$ = 300 µs | Q1 Control FET | 100 A |
| | Q2 Sync FET | 400 A |
| Optimum Temperature Range | | -40 °C < $T_J$ < 150 °C |

## STATIC CHARACTERISTICS

| Parameter | Conditions | Q1 Control FET | Q2 Sync FET |
|---|---|---|---|
| Maximum Drain – Source Voltage ($BV_{DSS}$) | Q1: $V_{GS}$ = 0 V, $I_D$ = 250 µA<br>Q2: $V_{GS}$ = 0 V, $I_D$ = 1 mA | 30 V | |
| Maximum Drain – Source Leakage | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | 200 µA | 800 µA |
| Maximum $R_{DS(ON)}$ | $V_{GS}$ = 5 V, $I_D$ = 25 A | 8 mΩ | 2 mΩ |
| Typical $R_{DS(ON)}$ | $V_{GS}$ = 5 V, $I_D$ = 25 A | 6 mΩ | 1.5 mΩ |
| Gate – Source Threshold Voltage | Q1: $I_D$ = 4 mA, $V_{DS}$ = $V_{GS}$<br>Q2: $I_D$ = 16 mA, $V_{DS}$ = $V_{GS}$ | 0.8 V < $V_{GS(TH)}$ < 2.5 V | |
| Gate – Source Maximum Positive Leakage | $V_{GS}$ = 5 V | 3 mA | 9 mA |
| Gate – Source Maximum Negative Leakage | $V_{GS}$ = -4 V | -200 µA | -800 µA |

$T_J$ = 25 °C unless otherwise stated

## DYNAMIC CHARACTERISTICS

| Parameter | Conditions | Typical Value | | |
|---|---|---|---|---|
| | | Q1 Control FET | Q2 Sync FET | Unit |
| $C_{ISS}$ (Input Capacitance) | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | 0.38 | 1.7 | nF |
| $C_{OSS}$ (Output Capacitance) | | 0.29 | 1.6 | |
| $C_{RSS}$ (Reverse Transfer Capacitance) | | 0.02 | 0.11 | |
| $Q_G$ (Total Gate Charge) | $V_{DS}$ = 15 V, $I_D$ = 25 A | 3.5 | 15 | nC |
| $Q_{GS}$ (Gate to Source Charge) | | 1.4 | 4.6 | |
| $Q_{GD}$ (Gate to Drain Charge) | | 0.57 | 2.6 | |
| $Q_{G(TH)}$ (Gate Charge at Threshold) | | 0.90 | 3.4 | |
| $Q_{OSS}$ (Output Charge) | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | 5.5 | 28 | |
| $Q_{RR}$ (Source-Drain Recovery Charge) | | 0 | 0 | |

$T_J$ = 25 °C unless otherwise stated

## THERMAL CHARACTERISTICS

| | | TYP | | |
|---|---|---|---|---|
| | | Q1 Control FET | Q2 Sync FET | |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 0.4 | | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction to Board (Note 2) | 1.8 | 1.2 | °C/W |
| $R_{\theta 12}$ | Thermal Resistance, Cross-Coupling | 0.85 | | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1) | 42 | | °C/W |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
Note 2: ΔT is determined by the following matrix equation:

$$\begin{pmatrix} \Delta T_{Q1} \\ \Delta T_{Q2} \end{pmatrix} = \begin{bmatrix} 1.2 & 0.85 \\ 0.85 & 1.8 \end{bmatrix} \cdot \begin{pmatrix} P_{Q1} \\ P_{Q2} \end{pmatrix}$$

This matrix equation lets you calculate the temperature rise of each FET, given the power dissipated in each FET.
Thermal models for EPC devices available at http://epc-co.com/epc/DesignSupport/DeviceModels.aspx

**Figure 1a:**

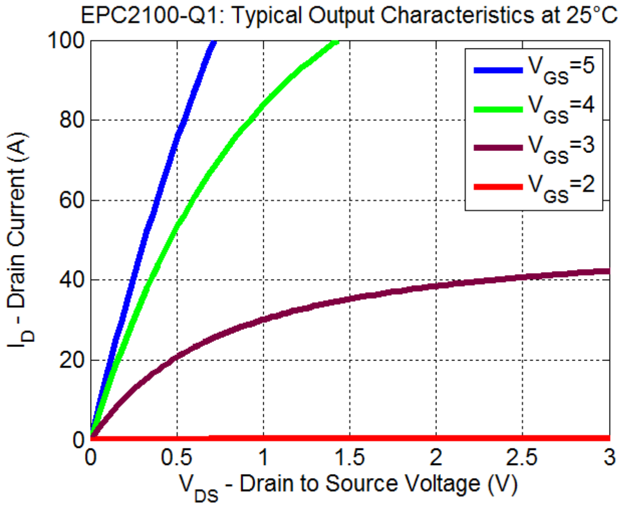



**Figure 1b:**

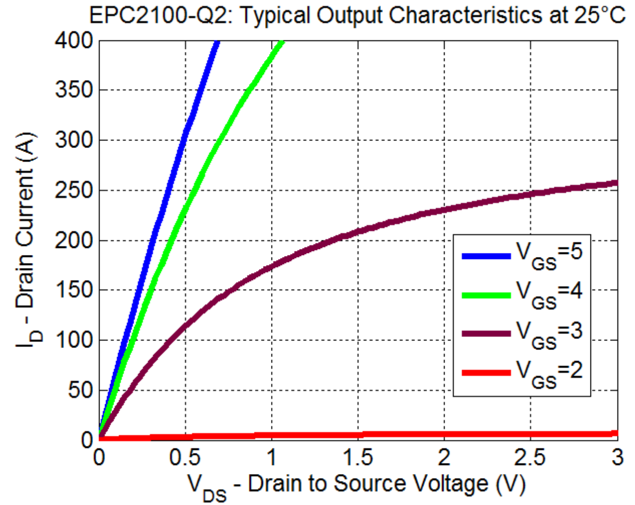



**Figure 2a:**

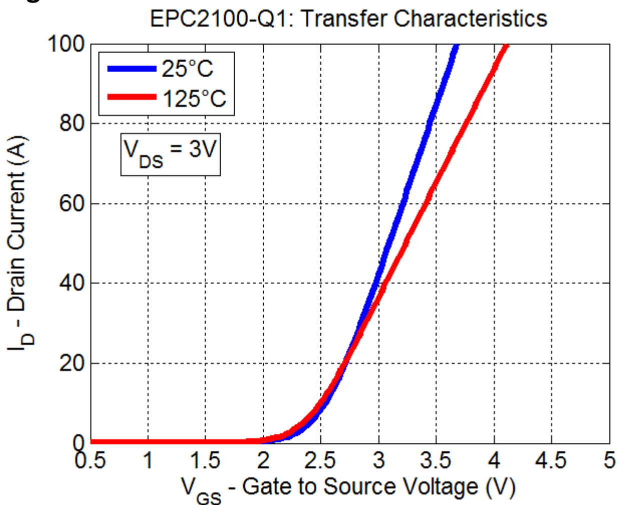



**Figure 2b:**

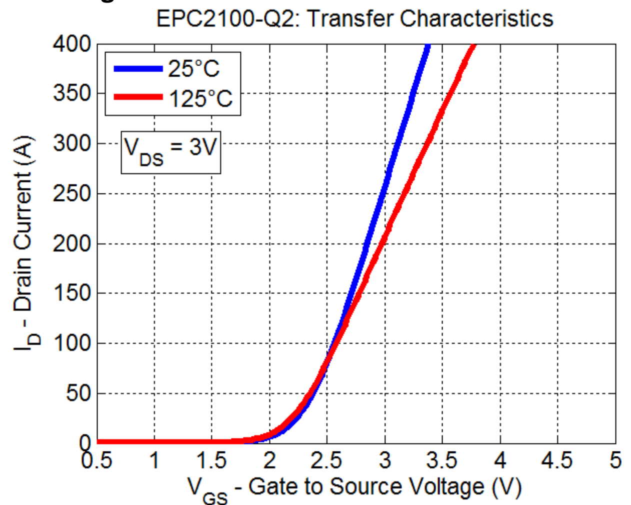



**Figure 3a:**

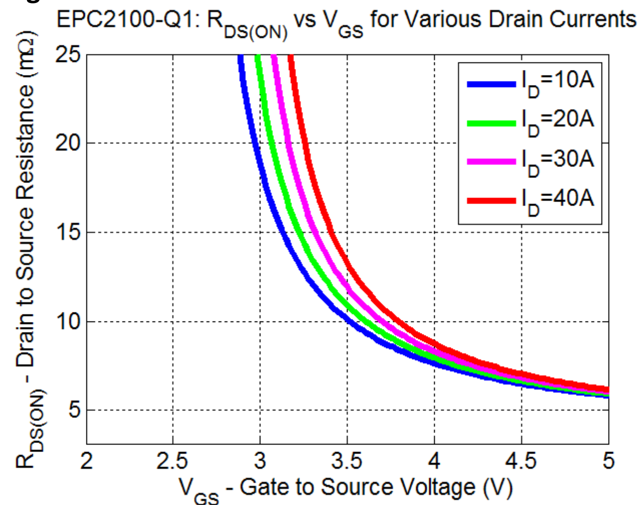



**Figure 3b:**

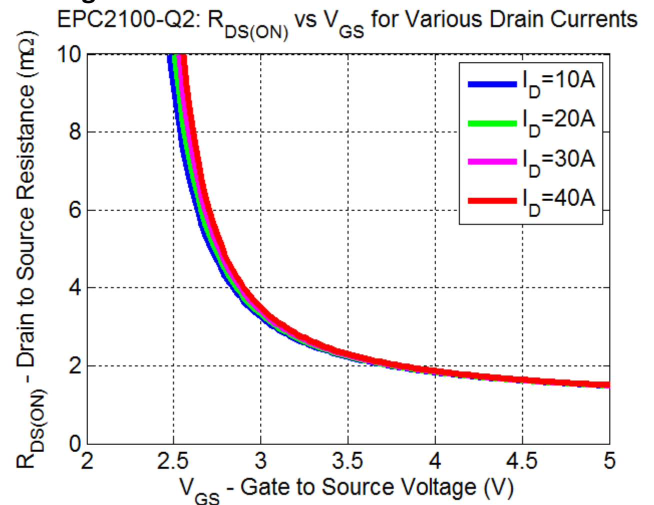


**Figure 4a:**

**Figure 4b:**

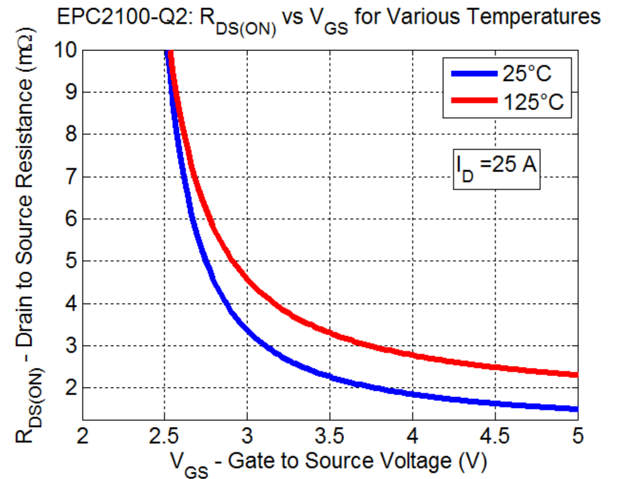



**Figure 5a:**

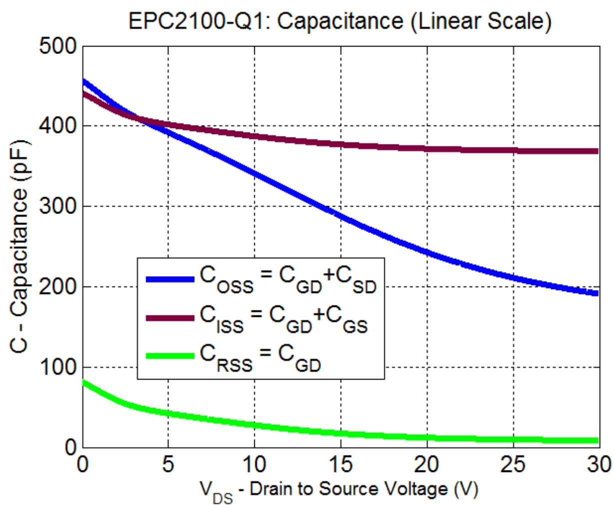



**Figure 5b:**

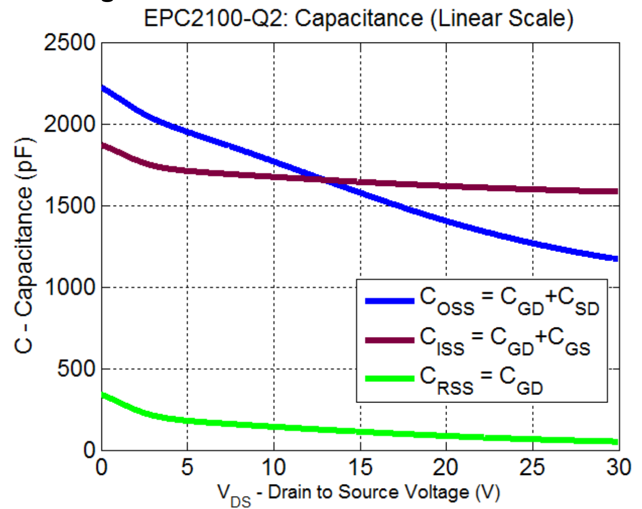



**Figure 5c:**

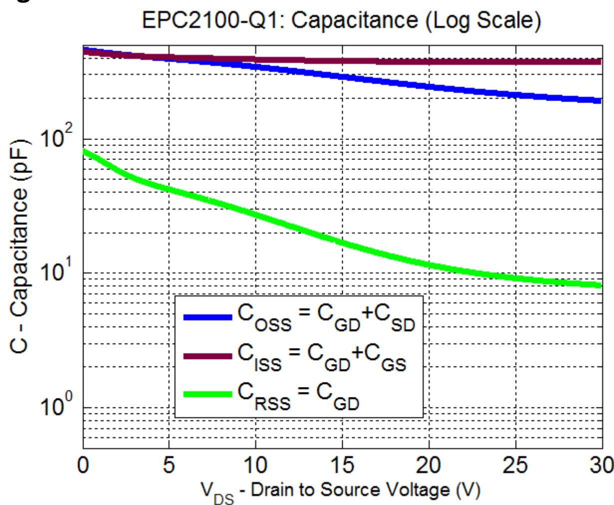



**Figure 5d:**

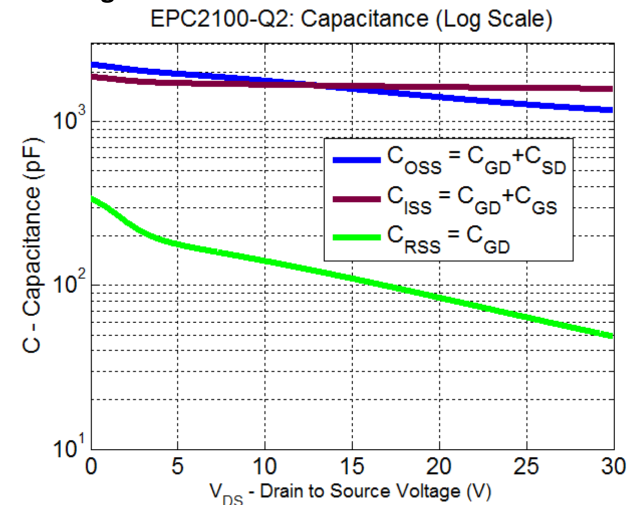


**Figure 6a:**

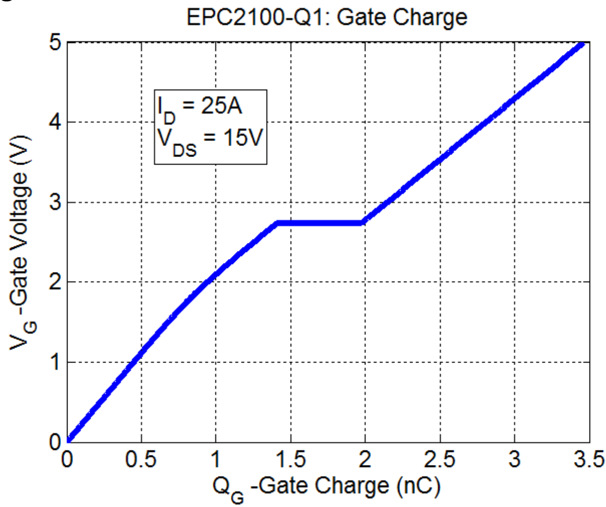



**Figure6b:**

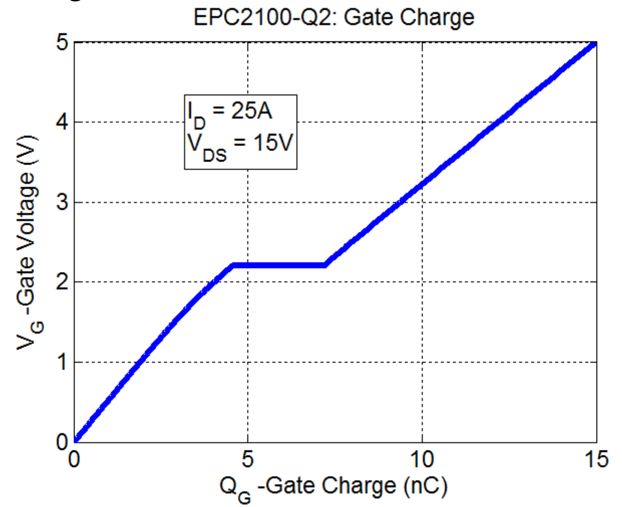



**Figure 7a:**

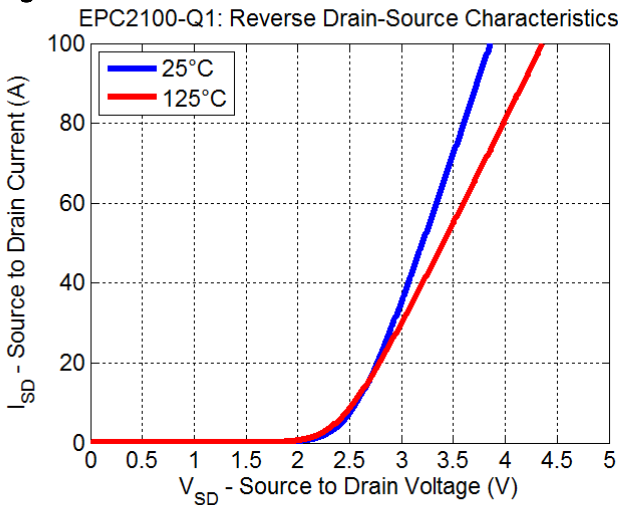



**Figure7b:**

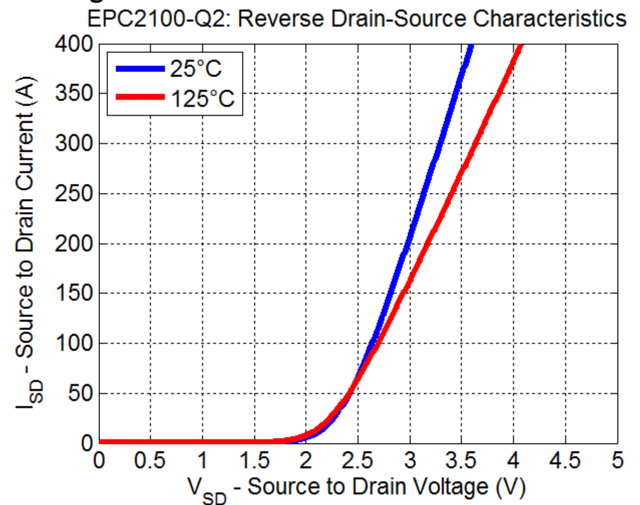



**Figure 8a:**

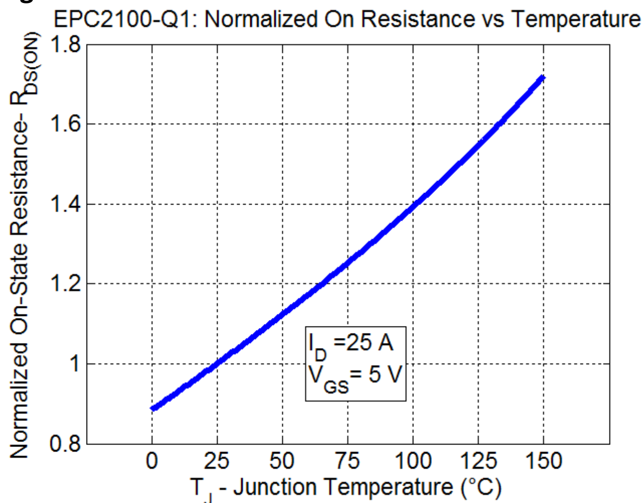



**Figure 8b:**

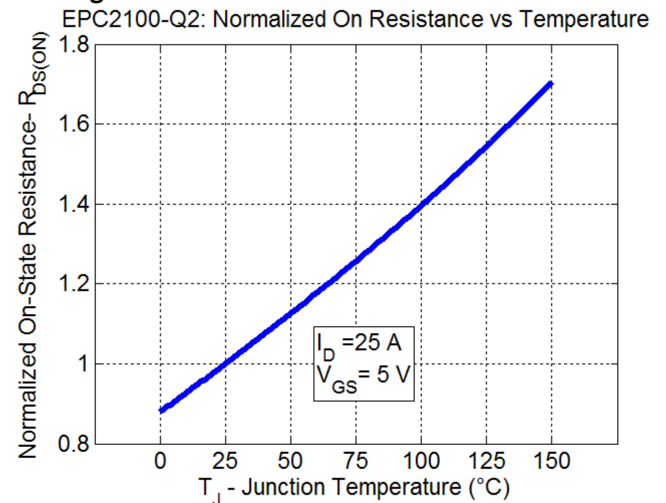


**Figure 9a:**

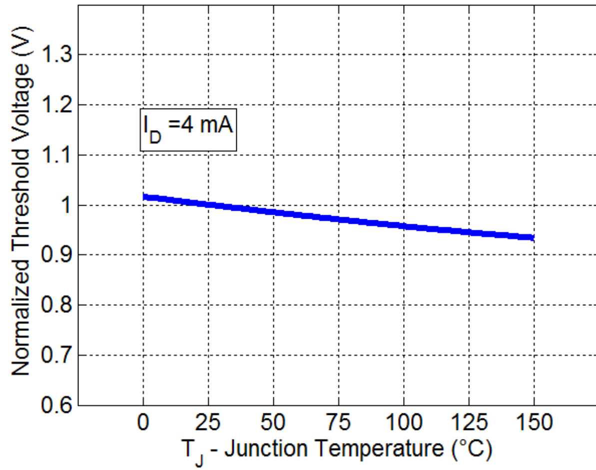
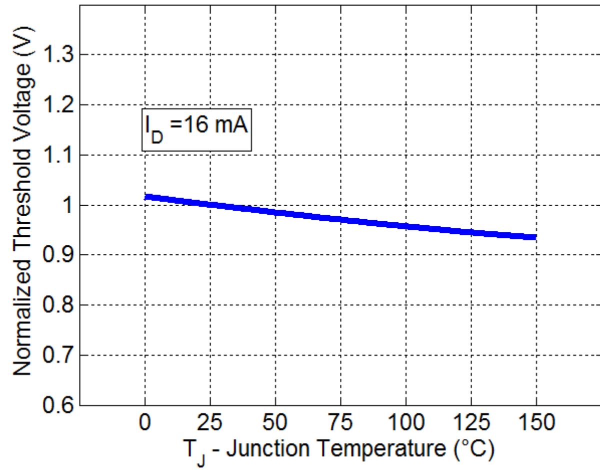
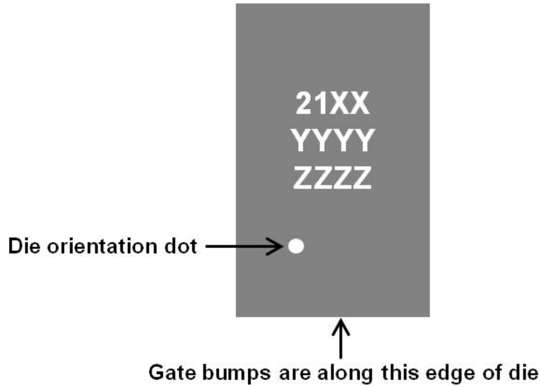



**Figure 9b:**



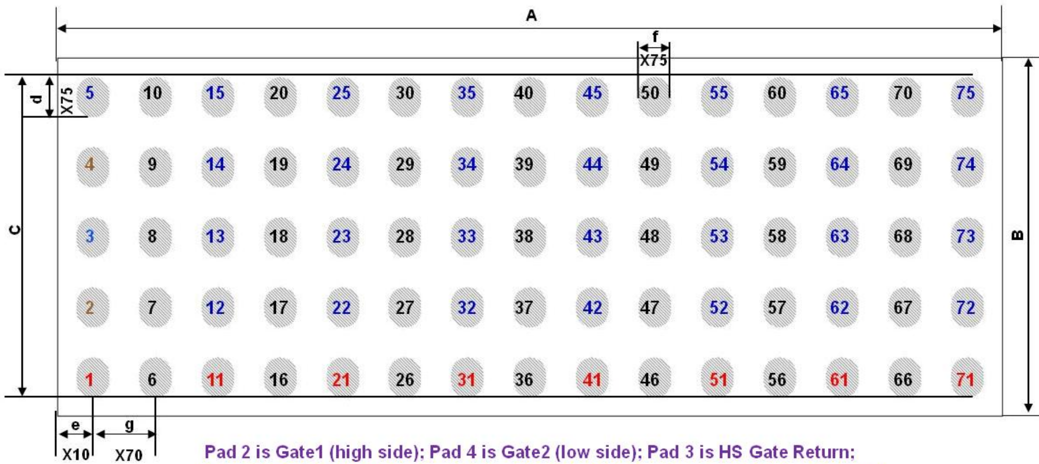
## DIE MARKINGS




| Part Number | Laser Marking | | |
|---|---|---|---|
| | Part # Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC2100ENGR | 21XX | YYYY | ZZZZ |

## DIE OUTLINE

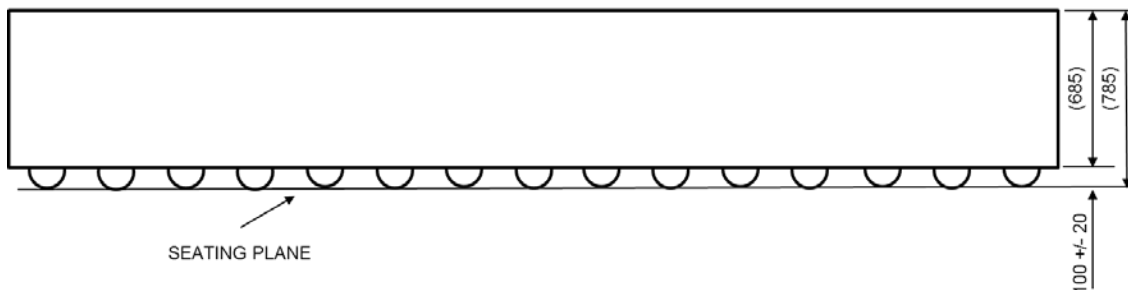
### Solder Bar View




| DIM | MICROMETERS | | |
|---|---|---|---|
| | MIN | Nominal | MAX |
| A | 6020 | 6050 | 6080 |
| B | 2270 | 2300 | 2330 |
| c | 2047 | 2050 | 2053 |
| d | 247 | 250 | 253 |
| e | 210 | 225 | 240 |
| f | 195 | 200 | 205 |
| g | 400 | 400 | 400 |

Pad 2 is Gate1 (high side); Pad 4 is Gate2 (low side); Pad 3 is HS Gate Return;
Pads 5, 12, 13, 14, 15, 22, 23, 24, 25, 32, 33, 34, 35, 42, 43, 44, 45, 52, 53, 54, 55, 62, 63, 64, 65, 72, 73, 74, 75 are Ground
Pads 1, 11, 21, 31, 41, 51, 61, 71 are $V_{IN}$
Pads 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are switch node.

### Side View

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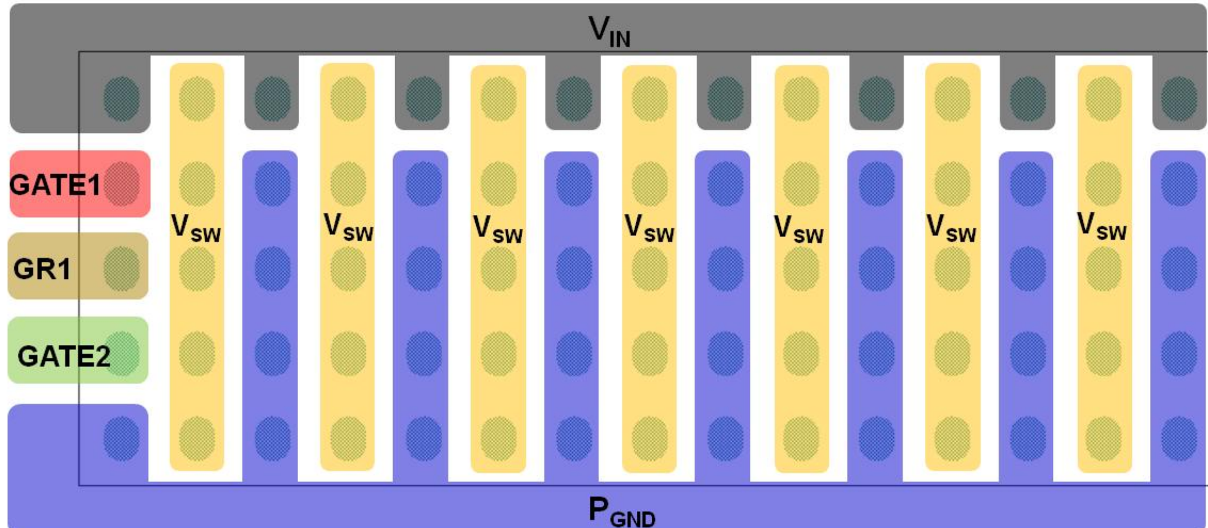
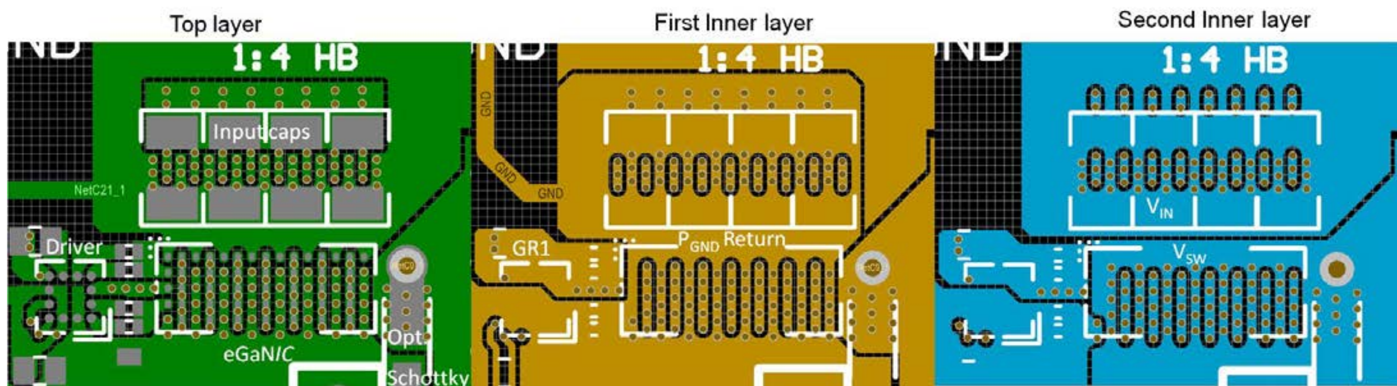
**RECOMMENDED LAND PATTERN**
(*Units in µm*)




**Land pattern is solder mask defined**.

**LAYOUT EXAMPLE**




**Recommended PCB Layout**

Gerber Files available at:
http://epc-co.com/epc/documents/gerber-files/EPC9036%20Development%20Board%20Gerbers.zip
Assembly Resources at: http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012
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