T20 Data Sheet

DST20-v3.1
February 2020
www.efinixinc.com

Contents

Introduction

The T20 FPGA features the high-density, low-power Efinix® Quantum™ architecture wrapped with an I/O interface for easy integration. With a high I/O to logic ratio and differential I/O support, T20 FPGAs supports a variety of applications that need wide I/O connectivity. The T20 also includes a MIPI D-PHY with a built-in, royalty-free CSI-2 controller, which is the most popular camera interface used in the mobile industry. Additionally, T20 FPGAs support a DDR3, LPDDR3, LPDDR2 PHY with memory controller hard IP that provides faster access to data stored in memory. The carefully tailored combination of core resources and I/O provides enhanced capability for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, power management, and LED drivers.

Features

- High-density, low-power Quantum™ architecture
- Built on SMIC 40 nm process
- Low core leakage current (6.7 mA typical)
- FPGA interface blocks
  - GPIO
  - PLL
  - LVDS 800 Mbps per lane with up to 20 TX pairs and 26 RX pairs
  - MIPI DPHY with CSI-2 controller hard IP, 1.5 Gbps per lane
  - DDR3, LPDDR3, LPDDR2 x16 PHY with memory controller hard IP, 12.8 Gbps aggregate bandwidth
- Programmable high-performance I/O
  - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces
- Flexible on-chip clocking
  - 16 low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
  - PLL support
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Optional Mask Programmable Memory (MPM) capability
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T20 FPGA Resources

LEs[1]	Global Clock Networks	Global Control Networks	Embedded Memory (kbits)	Embedded Memory Blocks (5 Kbits)	Embedded Multipliers
19,728	Up to 16	Up to 16	1044.48	204	36

[1] Logic capacity in equivalent LE counts.

Table 2: T20 Package-Dependent Resources

Resource	BGA169	BGA256	BGA324	BGA400
Available GPIO[2]	73	195	130	[3]
Global clocks from GPIO pins	4	16	5	[3]
Global controls from GPIO pins	3	16	5	[3]
PLLs	5	5	7	7
LVDS	8 TX pairs 12 RX pairs	13 TX pairs 13 RX pairs	20 TX 26 RX	20 TX 26 RX
MIPI DPHY with CSI-2 controller (4 data lanes, 1 clock lane)	2 TX instances 2 RX instances	–	2 TX instances 2 RX instances	–
DDR3/LPDDR3/LPDDR2 PHY with memory controller	–	–	1 block (x8 or x16 DQ widths)	1 block (x8 or x16 DQ widths)

Available Package Options

Table 3: Available Packages

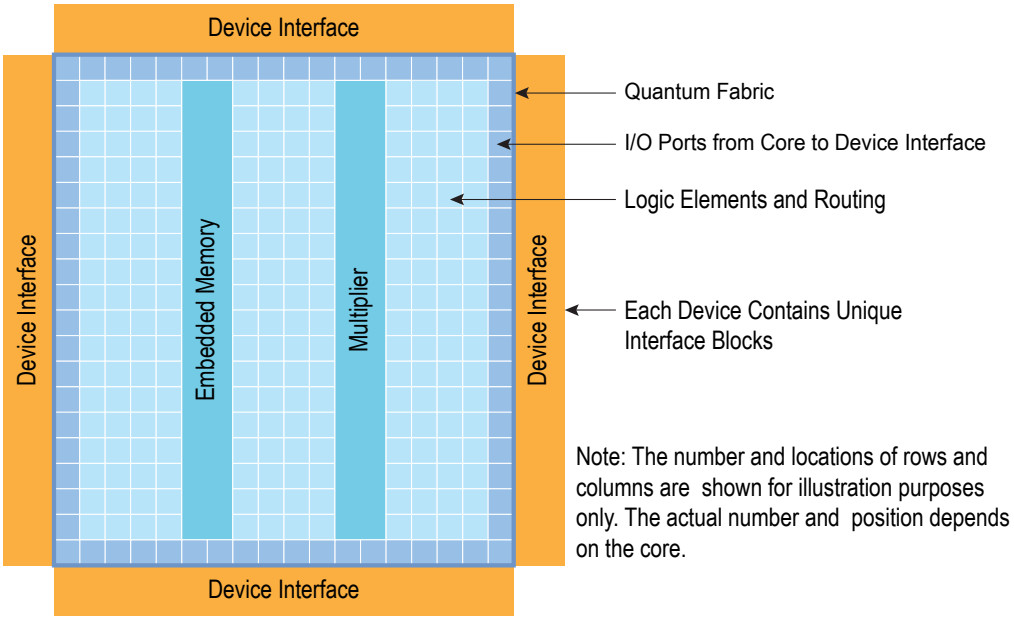
Package	Dimensions (mm x mm)	Pitch (mm)
169-ball FBGA	9 x 9	0.65
256-ball FBGA	13 x 13	0.8
324-ball FBGA	12 x 12	0.65
400-ball FBGA	16 x 16	0.8

Device Core Functional Description

T20 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Efinix has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: LEs, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of LEs, memory, and multipliers. A control block within the FPGA handles configuration.

[2] The LVDS I/O pins are dual-purpose. The full number of GPIO are avaiable when all LVDS I/O pins are in GPIO mode.
[3] Contact Efinix for the resource information for this package.

Figure 1: T20 FPGA Block Diagram



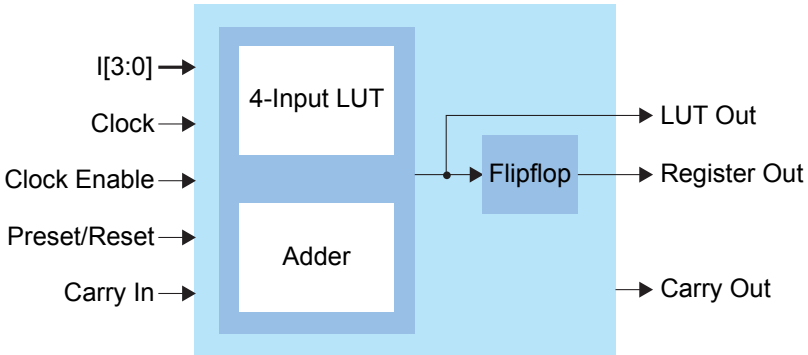
XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum™ architecture. The Efinix XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The LE comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple LEs to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Element Block Diagram



Embedded Memory

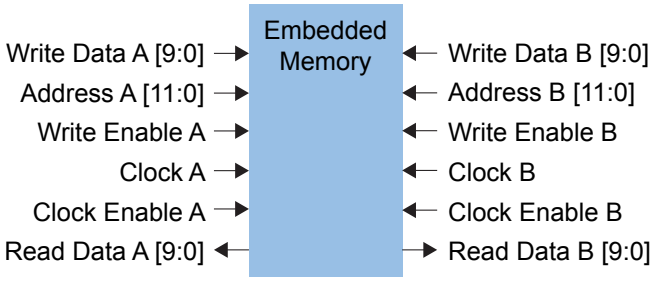
The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

The memory read and write ports have the following modes for addressing the memory (depth x width):

256 x 16	1024 x 4	4096 x 1	512 x 10
512 x 8	2048 x 2	256 x 20	1024 x 5

The read and write ports support independently configured data widths.

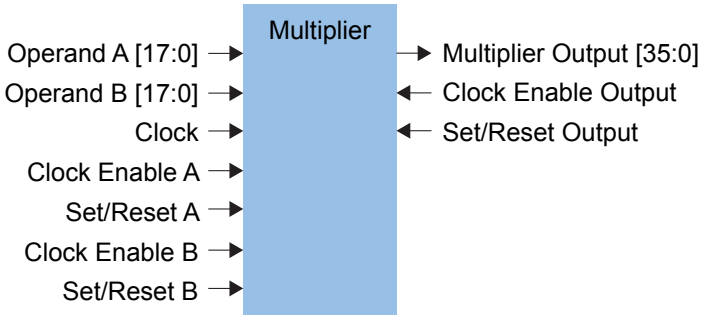
Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)



Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

Figure 4: Multiplier Block Diagram

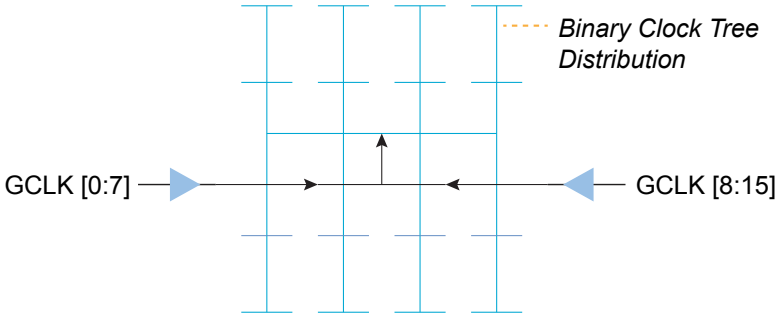


Global Clock Network

The Quantum™ core fabric supports up to 16 global clock (GCLK) signals feeding 16 pre-built global clock networks. Global clock pins (GPIO), PLL outputs, and core-generated clocks can drive the global clock network

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network



Device Interface Functional Description

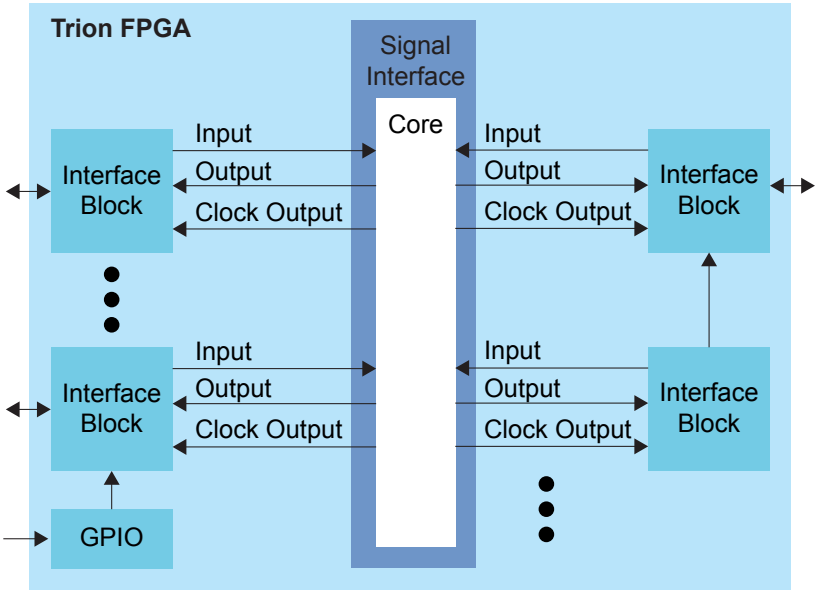
The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum™ architecture, devices in the Trion® family support a variety of interfaces to meet the needs of different applications.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion® FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block. The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the T20 interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 4: GPIO Modes

GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered. In DDIO mode, two registers sample the data on the positive and negative edges of the input clock, creating two data streams.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted. In DDIO mode, two registers capture the data on the positive and negative edges of the output clock, multiplexing them into one data stream.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

The T20 I/O buffer supports weak pull-up mode, weak pull-down mode, and the input I/O buffer supports a Schmitt trigger mode. The output I/O buffer has four settings for programmable drive strength[4] as well as an option to enable or disable the slew rate. Turn on the **Enable Slew Rate** option in the Efinity® Interface Designer for a slow slew rate; turn the option off for a fast slew rate. When the I/O buffer is disabled, the output value is tristated.

Note: Refer to Table 58: Single-Ended I/O Buffer Drive Strength Characteristics on page 43 for more information.

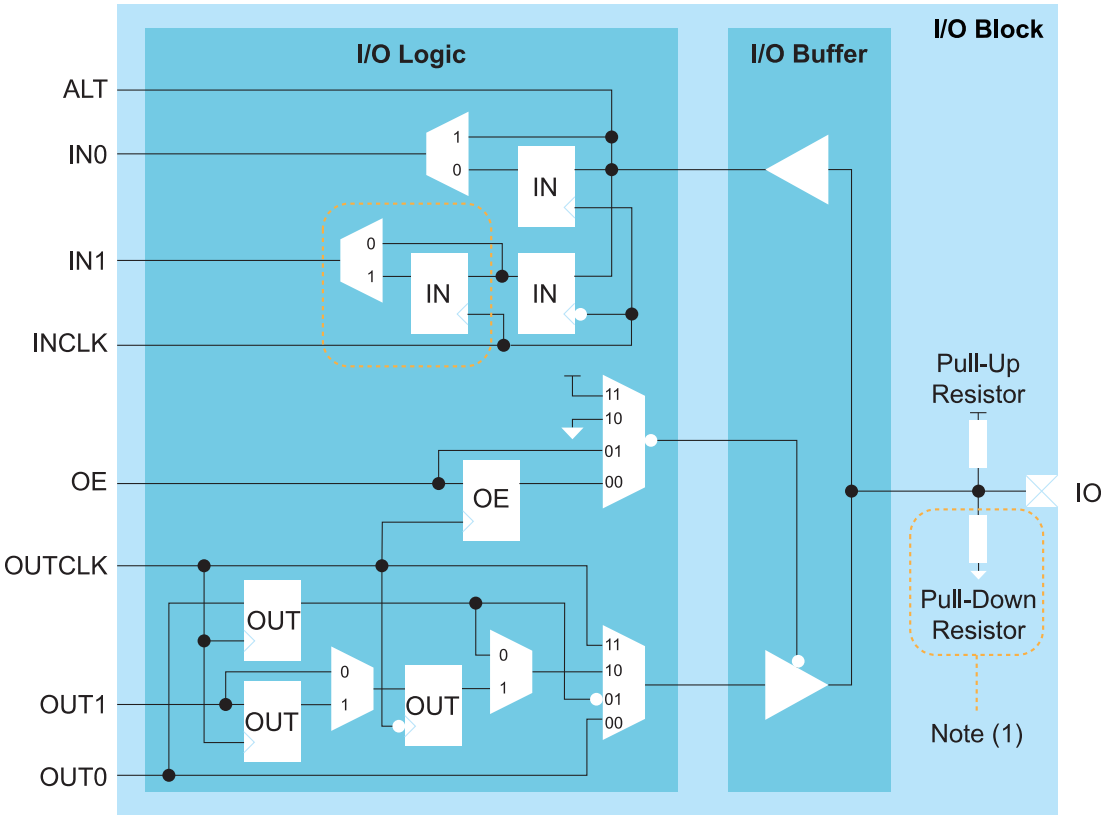
During configuration, all GPIO pins are tristated and configured in weak pull-up mode.

By default, unused GPIO pins are tristated and configured in weak pull-up mode. You can change the default mode to weak pull-down in the Interface Designer.

[4] GPIO pins using LVDS resources do not have programmable drive strength.

Complex I/O Buffer

Figure 7: I/O Interface Block



1. GPIO pins using LVDS resources do not have a pull-down resistor.

Note: LVDS pins configured as GPIO do not have double data I/O (DDIO).

Table 5: GPIO Signals

Signal	Direction	Description
IN[1:0]	Output	Input data from the GPIO pad to the core fabric. IN0 is the normal input to the core. In DDIO mode, IN0 is the data captured on the positive clock edge (HI pin name in the Interface Designer) and IN1 is the data captured on the negative clock edge (LO pin name in the Interface Designer).
ALT	Output	Alternative input connection (in the Interface Designer, **Register Option** is **none**). Alternative connections are GCLK, GCTRL, and PLLCLK.
OUT[1:0]	Input	Output data to GPIO pad from the core fabric. OUT0 is the normal output from the core. In DDIO mode, OUT0 is the data captured on the positive clock edge (HI pin name in the Interface Designer) and OUT1 is the data captured on the negative clock edge (LO pin name in the Interface Designer).
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE registers. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input registers. This clock is not visible in the user netlist.

Table 6: GPIO Pads

Signal	Direction	Description
IO	Bidirectional	GPIO pad.

Double-Data I/O

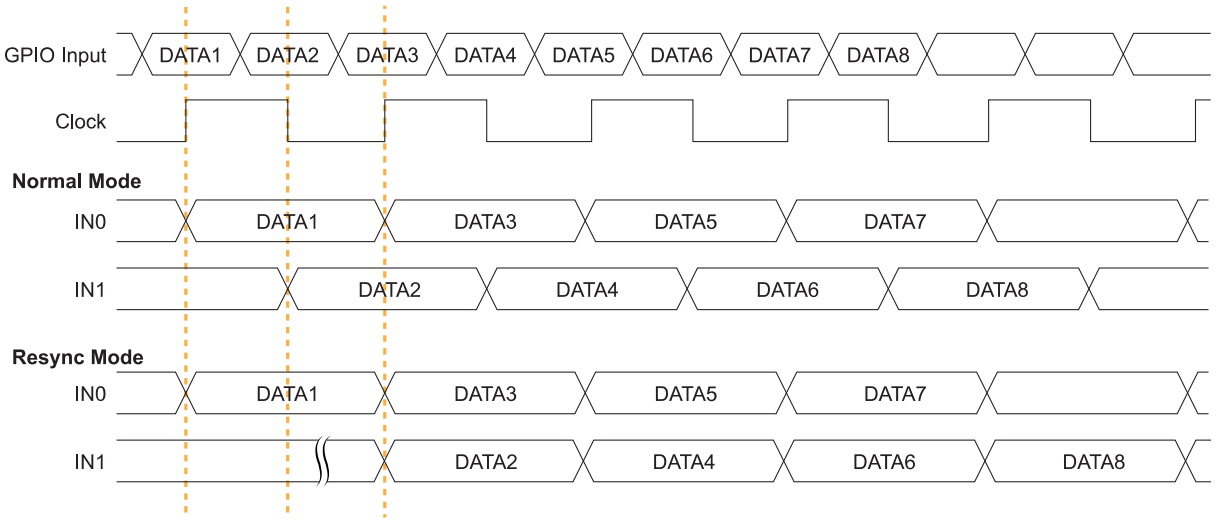
T20 FPGAs support double data I/O (DDIO) on certain input and output registers. In this mode, the DDIO register captures data on both positive and negative clock edges. The core receives 2 bit wide data from the interface.

In normal mode, the interface receives or sends data directly to or from the core on the positive and negative clock edges. In resync mode, the interface resynchronizes the data to pass both signals on the positive clock edge only.

Not all GPIO support DDIO; additionally, LVDS pins configured as GPIO (that is, single ended I/O) do not support DDIO functionality.

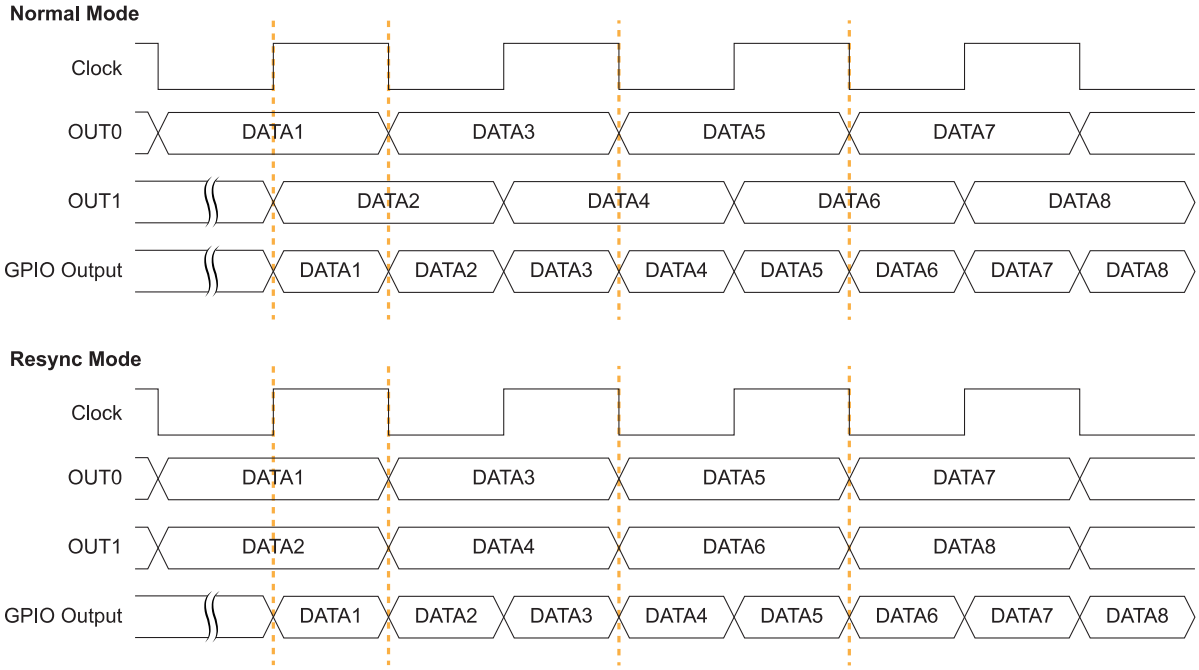
Note: The Resource Assigner in the Efinity® Interface Designer shows which GPIO support DDIO.

Figure 8: DDIO Input Timing Waveform



In resync mode, the IN1 data captured on the falling clock edge is delayed one half clock cycle.
In the Interface Designer, IN0 is the HI pin name and IN1 is the LO pin name.

Figure 9: DDIO Output Timing Waveform



In the Interface Designer, OUT0 is the HI pin name and OUT1 is the LO pin name.

Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T20 global clock network using the global clock GPIO pins, PLL outputs, and core-generated clocks. Similarly, the T20 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.

Learn more: Refer to the T20 Pinout for information on the location and names of these pins.

I/O Banks

Trion FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

The number of banks and the voltages they support vary by package.

Some I/O banks are merged at the package level by sharing VCCIO pins. Merged banks have underscores (_) between banks in the name (e.g., 1B_1C means 1B and 1C are connected).

Table 7: I/O Banks by Package

Package	I/O Banks	Voltage (V)	Banks with DDIO Support	Merged Banks
BGA169	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1B_1C_1D, 3A_3B, 3C_3D_3E
	4A, 4B	3.3	–	–
BGA256	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1B_1C, 1D_1E. 3A_3B_3C, 3D_3E
	4A, 4B	3.3	–	–
BGA324	1A - 1E, 2A - 2C, 3A - 3C, 4A, 4B, TR, BR	1.8, 2.5, 3.3	1A - 1E, 3C, TR, BR	1B_1C, 1D_1E

Learn more: Refer to the T20 Pinout for information on the I/O bank assignments.

PLL

The T20 has 5 available PLLs to synthesize clock frequencies.

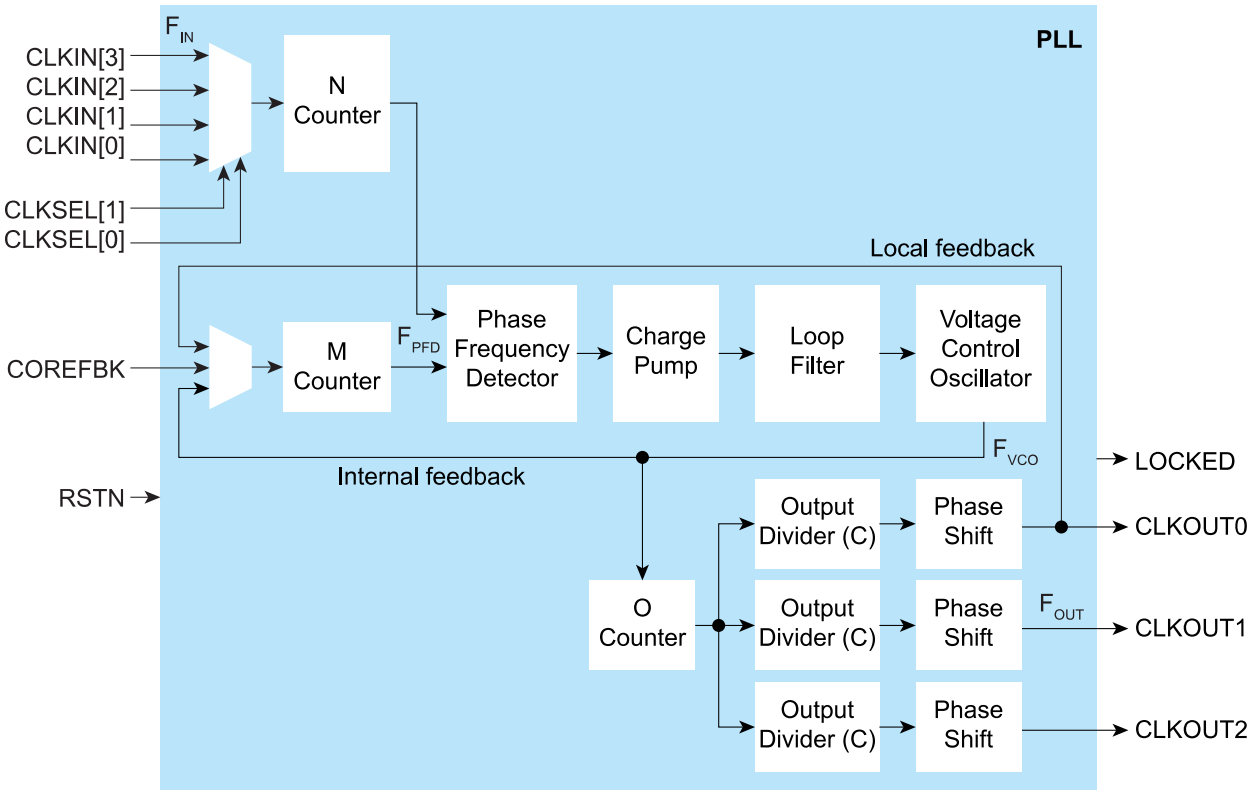
You can use the PLL to compensate for clock skew/delay via external or internal feedback to meet timing requirements in advanced application. The PLL reference clock has up to four sources. You can dynamically select the PLL reference clock with the `CLKSEL` port. (Hold the PLL in reset when dynamically selecting the reference clock source.)

One of the PLLs can use an LVDS RX buffer to input it's reference clock.

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output divider.

Note: Refer to T20 Interface Floorplan for the location of the PLLs on the die. Refer to Table 89: General Pinouts on page 54 for the PLL reference clock resource assignment.

Figure 10: PLL Block Diagram



The counter settings define the PLL output frequency:

Internal Feedback Mode	Local and Core Feedback Mode	Where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = (F_{IN} \times M) / (N \times O \times C)$	$F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$ [5] $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency C is the output divider

[5] $(M \times O \times C_{FBK})$ must be ≤ 255.

Note: The reference clock must be between 10 and 200 MHz.
The PFD input must be between 10 and 50 MHz.
The VCO frequency must be between 500 and 1,500 MHz.

Figure 11: PLL Interface Block Diagram

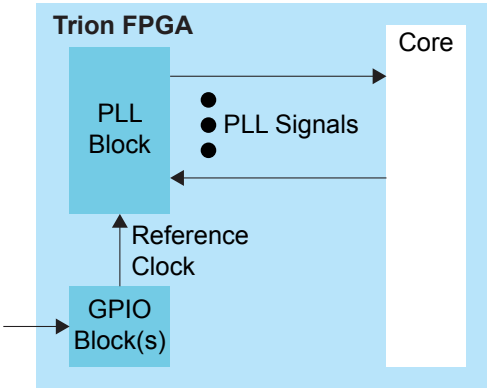


Table 8: PLL Signals (Interface to FPGA Fabric)

Signal	Direction	Description
CLKIN[3:0]	Input	Reference clocks driven by I/O pads or core clock tree.
CLKSEL[1:0]	Input	You can dynamically select the reference clock from one of the clock in pins.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL. Assert RSTN when dynamically changing the selected PLL reference clock.
COREFBK	Input	Connect to a clock out interface pin when the the PLL feedback mode is set to core.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status.

Table 9: PLL Interface Designer Settings - Properties Tab

Parameter	Choices	Notes
Instance Name	User defined	
PLL Resource		The resource listing depends on the FPGA you choose.
Clock Source	External	PLL reference clock comes from an external pin.
	Dynamic	PLL reference clock comes from an external pin or the core, and is controlled by the clock select bus.
	Core	PLL reference clock comes from the core.
Automated Clock Calculation		Pressing this button launches the PLL Clock Caclulation window. The calculator helps you define PLL settings in an easy-to-use graphical interface.

Table 10: PLL Interface Designer Settings - Manual Configuration Tab

Parameter	Choices	Notes
Reset Pin Name	User defined	
Locked Pin Name	User defined	
Feedback Mode	Internal	PLL feedback is internal to the PLL resulting in no known phase relationship between clock in and clock out.
	Local	PLL feedback is local to the PLL. Aligns the clock out phase with clock in.
	Core	PLL feedback is from the core. The feedback clock is defined by the COREFBK connection, and must be one of the three PLL output clocks. Aligns the clock out phase with clock in and removes the core clock delay.
Reference clock Frequency (MHz)	User defined	
Multiplier (M)	1 - 255 (integer)	M counter.
Pre Divider (N)	1 - 15 (integer)	N counter.
Post Divider (O)	1, 2, 4, 8	O counter.
Clock 0, Clock 1, Clock 2	On, off	Use these checkboxes to enable or disable clock 0, 1, and 2.
Pin Name	User defined	Specify the pin name for clock 0, 1, or 2.
Divider (C)	1 to 256	Output divider.
Phase Shift (Degree)	0, 45, 90, 135, 180, or 270	Phase shift CLKOUT by 0, 45, 90, 135, 180, or 270 degrees. 90, 180, and 270 require the C divider to be 2. 45 and 135 require the C divider to be 4. To phase shift 225 degrees, select 45 and invert the clock at the destination. To phase shift 315 degrees, select 135 and invert the clock at the destination.
Use as Feedback	On, off	

Table 11: PLL Reference Clock Resource Assignments (BGA169 and BGA256)

PLL	REFCLK1	REFCLK2
BR_PLL	Differential: GPIOB_CLKP0, GPIOB_CLKN0 Single Ended: GPIOB_CLKP0	GPIOR_157_PLLIN
TR_PLL0	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
TR_PLL1	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
TL_PLL0	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1
TL_PLL1	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1

Table 12: PLL Reference Clock Resource Assignments (BGA324)

PLL	REFCLK0	REFCLK1
PLL_BL0	GPIOL_15_PLLIN0	N/A
PLL_BR0	GPIOR_138_PLLIN0	Single-ended: GPIOB_TXP09_CLK0
PLL_BR1	GPIOR_139_PLLIN1	Single-ended: GPIOB_TXP15_CLK1_CDI15
PLL_BR2	GPIOR_140_PLLIN2	Single-ended: GPIOB_TXP19_CLK2
PLL_TR0	GPIOR_118_PLLIN0	Differential: GPIOT_RXP08_CLKP0, GPIOT_RXN08_CLKN0 Single-ended: GPIOT_RXP08_CLKP0

PLL	REFCLK0	REFCLK1
PLL_TR1	GPIOR_119_PLLIN0	Differential: GPIOT_RXP17_CLKP1, GPIOT_RXN17_CLKN1 Single-ended: GPIOT_RXP17_CLKP1
PLL_TR2	GPIOR_120_PLLIN0	Differential: GPIOT_RXP25_CLKP2, GPIOT_RXN25_CLKN2 Single-ended: GPIOT_RXP25_CLKP2

LVDS

The LVDS hard IP transmitters and receivers operate independently.

- LVDS TX consists of LVDS transmitter and serializer logic.
- LVDS RX consists of LVDS receiver, on-die termination, and de-serializer logic.

The T20 has one PLL for use with the LVDS receiver.

Note: You can use the LVDS TX and LVDS RX channels as 3.3 V single-ended GPIO pins, which support a weak pull-up but do not support a Schmitt trigger or variable drive strength. When using LVDS as GPIO, make sure to leave at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS pins in the same bank. This separation reduces noise. The Efinity software issues an error if you do not leave this separation.

The LVDS hard IP has these features:

- Dedicated LVDS TX and RX channels (the number of channels is package dependent), and one dedicated LVDS RX clock
- Up to 800 Mbps for LVDS data transmit or receive
- Supported serialization and deserialization factors: 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1
- 1:1 mode to bypass the serializer or deserializer
- Source synchronous clock output edge-aligned with data for LVDS transmitter and receiver
- 100 Ω on-die termination resistor for the LVDS receiver

LVDS TX

Figure 12: LVDS TX Interface Block Diagram

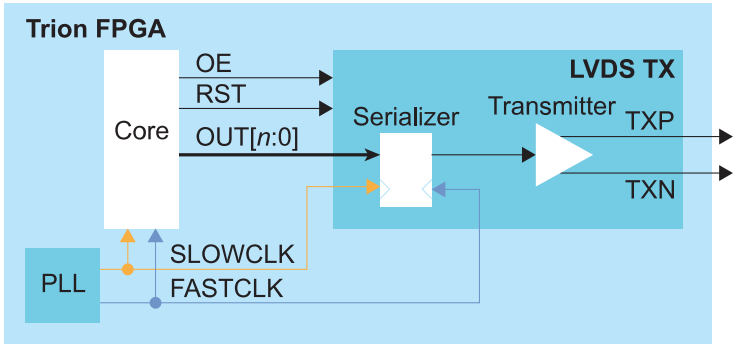


Table 13: LVDS TX Signals (Interface to FPGA Fabric)

Signal	Direction	Notes
OUT[*n*-1:0]	Input	Parallel output data where *n* is the serialization factor. A width of 1 bypasses the serializer.
OE	Input	LVDS output enable, available in simple buffer (x1) mode. Unused by default.
FASTCLK	Input	Fast clock to serialize the data to the LVDS pads.

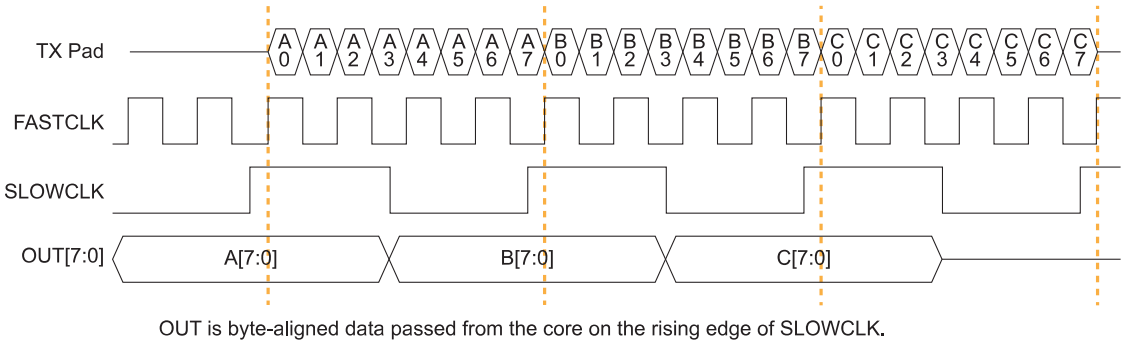
Signal	Direction	Notes
SLOWCLK	Input	Slow clock to latch the incoming data from the core.
RST	Input	Reset the serializer. Unused by default.

Table 14: LVDS TX Pads

Pad	Direction	Description
TXP	Output	Differential P pad.
TXN	Output	Differential N pad.

The following waveform shows the relationship between the fast clock, slow clock, TX data going to the pad, and byte-aligned data from the core.

Figure 13: LVDS Timing Example Serialization Width of 8



OUT is byte-aligned data passed from the core on the rising edge of SLOWCLK.

Table 15: LVDS TX Settings in Efinity® Interface Designer

Parameters	Choices	Notes
Mode	**serial data output** or **reference clock output**	**serial data output**—Simple output buffer or serialized output. **reference clock output**—Use the transmitter as a clock output.
Serialization Width	1, 2, 3, 4, 5, 6, 7, or 8	In x1 mode the serializer is bypassed and the LVDS buffer is used as a normal output.
Reduce VOD Swing	True or False	When true, enables reduced output swing (similar to slow slew rate).
Output Load	3 (default), 5, 7, or 10	Output load in pF.

LVDS RX

Figure 14: LVDS RX Interface Block Diagram

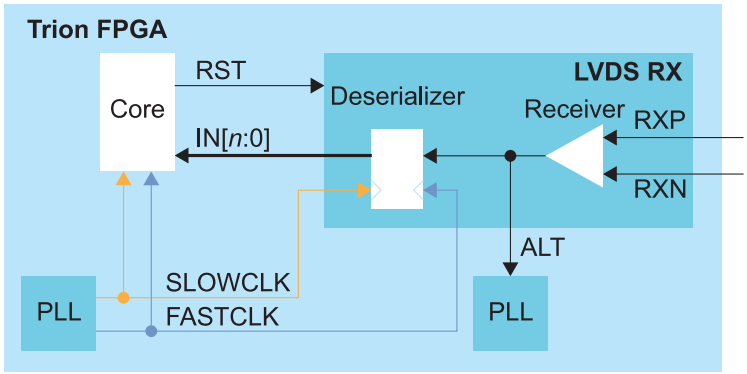


Table 16: LVDS RX Signals (Interface to FPGA Fabric)

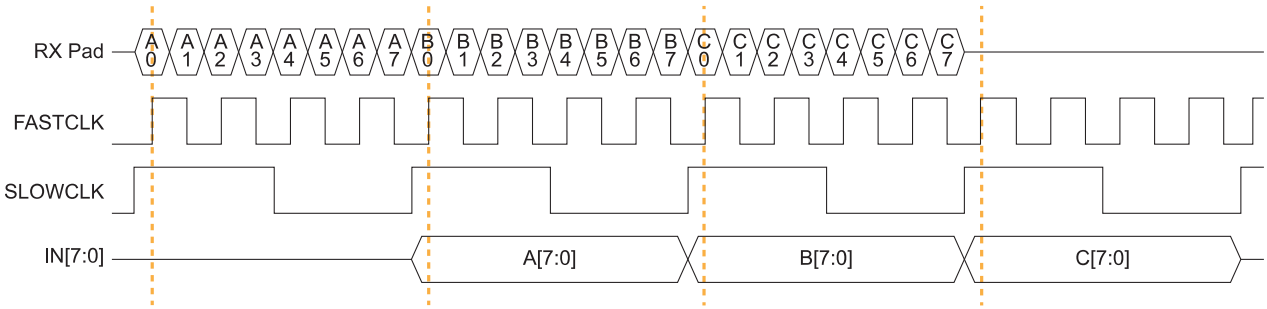
Signal	Direction	Notes
IN[*n*-1:0]	Output	Parallel input data where *n* is the de-serialization factor. A width of 1 bypasses the deserializer.
ALT	Output	Alternative input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternative connections are PLLCLK and PLLFBK.
FASTCLK	Input	Fast clock to de-serialize the data from the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data to the core.
RST	Input	Reset the de-serializer. Unused by default.

Table 17: LVDS RX Pads

Pad	Direction	Description
RXP	Input	Differential P pad.
RXN	Input	Differential N pad.

The following waveform shows the relationship between the fast clock, slow clock, RX data coming in from the pad, and byte-aligned data to the core.

Figure 15: LVDS RX Timing Example Serialization Width of 8



IN is byte-aligned data passed to the core on the rising edge of SLOWCLK.

Table 18: LVDS RX Settings in Efinity® Interface Designer

Parameter	Choices	Notes
Connection Type	**normal** or **alternate**	**alternate**—Use the alternate function of the LVDS RX resource (such as a PLL reference clock). Also choose de-serialization width of 1. **normal**—Regular RX function.
Deserialization	1, 2, 3, 4, 5, 6, 7, or 8	In x1 mode the de-serializer is bypassed and the LVDS buffer is used as a normal input.
Enable On-Die Termination	True or False	When true, enables an on-die 100-ohm resistor.

MIPI

The MIPI CSI-2 interface is the most widely used camera interface for mobile.[6]. You can use this interface to build single- or multi-camera designs for a variety of applications.

T20 FPGAs include two hardened MIPI D-PHY blocks (4 data lanes and 1 clock lane) with MIPI CSI-2 IP blocks. The MIPI RX and MIPI TX can operate independently with dedicated I/O banks.

Note: The MIPI D-PHY and CSI-2 controller are hard blocks; users cannot bypass the CSI-2 controller to access the D-PHY directly for non-CSI-2 applications.

The MIPI TX/RX interface supports the MIPI CSI-2 specification v1.3 and the MIPI D-PHY specification v1.1. It has the following features:

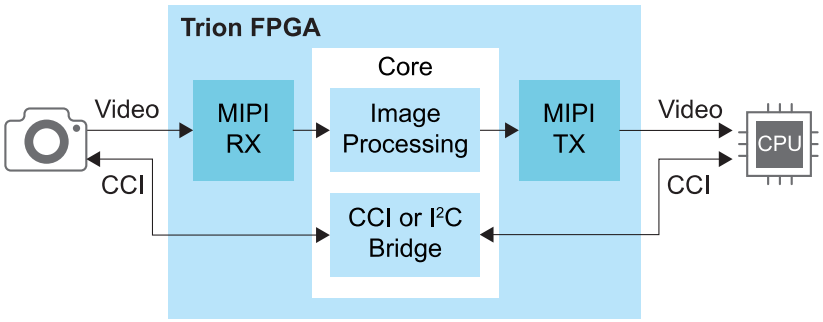
- Programmable data lane configuration supporting 1, 2, or 4 lanes
- High-speed mode supports up to 1.5 Gbps data rates per lane
- Operates in continuous and non-continuous clock modes
- 64 bit pixel interface for cameras
- Supports Ultra-Low Power State (ULPS)

Table 19: MIPI Supported Data Types

Supported Data Type	Format
RAW	RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
YUV	YUV420 8-bit (legacy), YUV420 8-bit, YUV420 10-bit, YUV420 8-bit (CSPS), YUV420 10-bit (CSPS), YUV422 8-bit, YUV422 10-bit
RGB	RGB444, RGB555, RGB565, RGB666, RGB888
User Defined	8 bit format

With more than one MIPI TX and RX blocks, Trion® FPGAs support a variety of video applications.

Figure 16: MIPI Example System

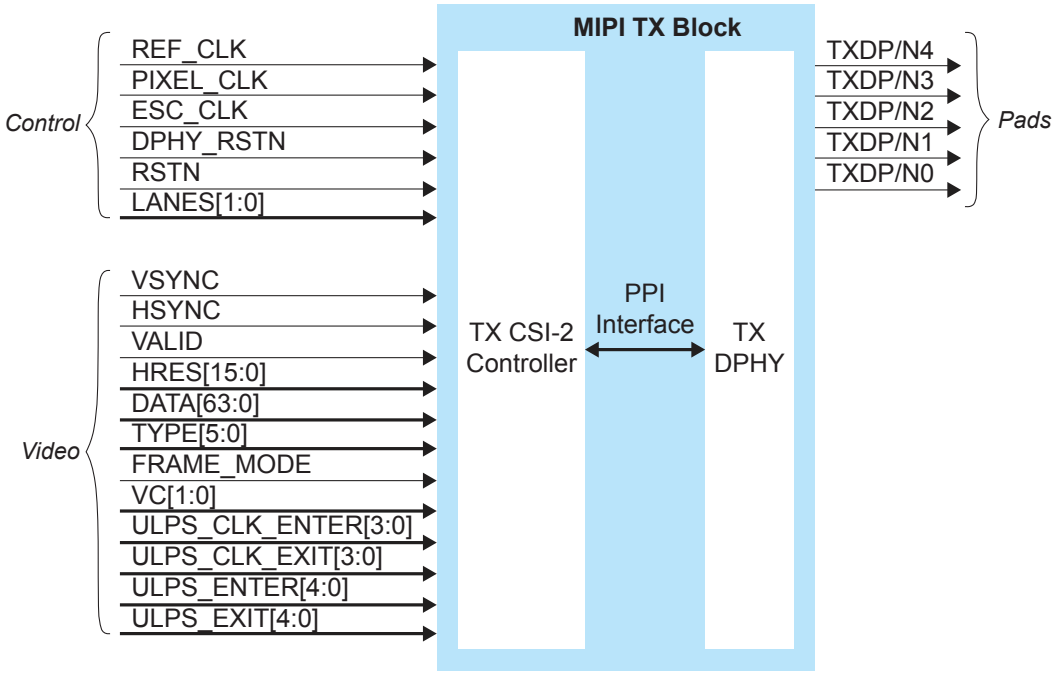


[6] Source: MIPI Alliance https://www.mipi.org/specifications/csi-2

MIPI TX

The MIPI TX is a transmitter interface that translates video data from the Trion® core into packetized data sent over the HSSI interface to the board. Five high-speed differential pin pairs (four data, one clock), each of which represent a lane, connect to the board. Control and video signals connect from the MIPI interface to the core.

Figure 17: MIPI TX x4 Block Diagram



The control signals determine the clocking and how many transceiver lanes are used. All control signals are required except the two reset signals. The reset signals are optional, however, you must use both signals or neither.

The MIPI block requires an escape clock (`ESC_CLK`) for use when the MIPI interface is in escape (low-power) mode, which runs between 11 and 20 MHz.

Note: Efinix recommends that you set the escape clock frequency as close to 20 MHz as possible.

The video signals receive the video data from the core. The MIPI interface block encodes is and sends it out through the MIPI D-PHY lanes.

The `REF_CLK` signal is a reference clock for the internal MIPI TX PLL used to generate the transmitted data. The FPGA has a dedicated GPIO resource (`MREFCLK`) that you must configure to provide the reference clock. All of the MIPI TX blocks share this resource.

Figure 18: MIPI TX Interface Block Diagram

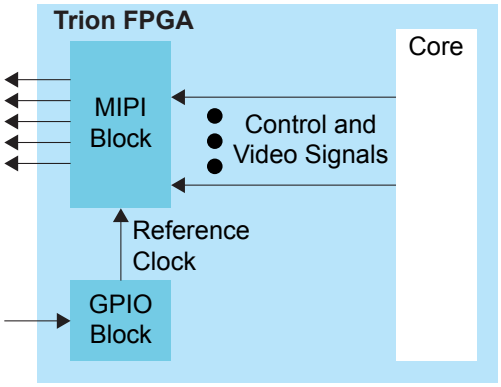


Table 20: MIPI TX Control Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
REF_CLK	Input	N/A	TX PLL reference clock. The frequency is set using Interface Designer configuration options. The software automatically assigns the GPIO resource (MREFCLK); the same resource is used for all MIPI TX instances.
PIXEL_CLK	Input	N/A	Clock used for transferring data from the core to the MIPI TX block. The frequency is based on the number of lanes and video format.
ESC_CLK	Input	N/A	Slow clock for escape mode (11 - 20 MHz).
DPHY_RSTN	Input	N/A	(Optional) Reset for the D-PHY logic, active low. Reset with the controller. See MIPI Reset Timing on page 49.
RSTN	Input	N/A	(Optional) Reset for the CSI-2 controller logic, active low. Should be reset with the PHY. See MIPI Reset Timing on page 49.
LANES[1:0]	Input	PIXEL_CLK	Determines the number of lanes enabled. Can only be changed during reset. 00: lane 0 01: lanes 0 and 1 11: all lanes

Table 21: MIPI TX Video Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
VSYNC	Input	PIXEL_CLK	Vertical sync.
HSYNC	Input	PIXEL_CLK	Horizontal sync.
VALID	Input	PIXEL_CLK	Valid signal.
HRES[15:0]	Input	PIXEL_CLK	Horizontal resolution. Can only be changed when HSYNC is low, and should be stable for at least one TX pixel clock cycle before HSYNC goes high.
DATA[63:0]	Input	PIXEL_CLK	Video data; the format depends on the data type. New data arrives on every pixel clock.
TYPE[5:0]	Input	PIXEL_CLK	Video data type. Can only be changed when HSYNC is low, and should be stable for at least one TX pixel clock cycle before HSYNC goes high.

Signal	Direction	Clock Domain	Description
FRAME_MODE	Input	PIXEL_CLK	0: general frame 1: accurate frame Can only be changed during reset.
VC[1:0]	Input	PIXEL_CLK	Virtual channel (VC). Can only be changed when VSYNC is low, and should be stable at least one TX pixel clock cycle before VSYNC goes high.
ULPS_CLK_ENTER	Input	PIXEL_CLK	Place the clock lane into ULPS mode. Should not be active at the same time as ULPS_CLK_EXIT. Each high pulse should be at least 5 µs.
ULPS_CLK_EXIT	Input	PIXEL_CLK	Remove clock lane from ULPS mode. Should not be active at the same time as ULPS_CLK_ENTER. Each high pulse should be at least 5 µs.
ULPS_ENTER[3:0]	Input	PIXEL_CLK	Place the data lane into ULPS mode. Should not be active at the same time as ULPS_EXIT[3:0]. Each high pulse should be at least 5 µs.
ULPS_EXIT[3:0]	Input	PIXEL_CLK	Remove the data lane from ULPS mode. Should not be active at the same time as ULPS_ENTER[3:0]. Each high pulse should be at least 5 µs.

Table 22: MIPI TX Pads

Pad	Direction	Description
TXDP[4:0]	Output	MIPI transceiver P pads.
TXDN[4:0]	Output	MIPI transceiver N pads.

Table 23: MIPI TX Settings in Efinity® Interface Designer

Tab	Parameter	Choices	Notes
Base	PHY Frequency (MHz)	80.00 - 1500.00	Choose one of the possible PHY frequency values.
	Frequency (reference clock)	6, 12, 19.2, 25, 26, 27, 38.4, or 52 MHz	Reference clock frequency.
	Enable Continuous PHY Clocking	On or Off	Turns continuous clock mode on or off.
Control	Escape Clock Pin Name	User defined	
	Invert Escape Clock	On or Off	
	Pixel Clock Pin Name	User defined	
	Invert Pixel Clock	On or Off	
Lane Mapping	TXD0, TXD1, TXD2, TXD3, TXD4	clk, data0, data1, data2, or data3	Map the physical lane to a clock or data lane.
	Clock Timer		
Timing	$T_{CLK-POST}$ $T_{CLK-TRAIL}$ $T_{CLK-PREPARE}$ $T_{CLK-ZERO}$	Varies depending on the PHY frequency	Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 30.
	Escape Clock Frequency (MHz)	User defined	Specify a number between 11 and 20 MHz.

Tab	Parameter	Choices	Notes
	$T_{CLK-PRE}$	Varies depending on the escape clock frequency	Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 30.
	Data Timer		
	$T_{HS-PREPARE}$ $T_{HS-ZERO}$ $T_{HS-PTRAIL}$	Varies depending on the PHY frequency	Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 30.

MIPI TX Video Data TYPE[5:0] Settings

The video data type can only be changed when HSYNC is low.

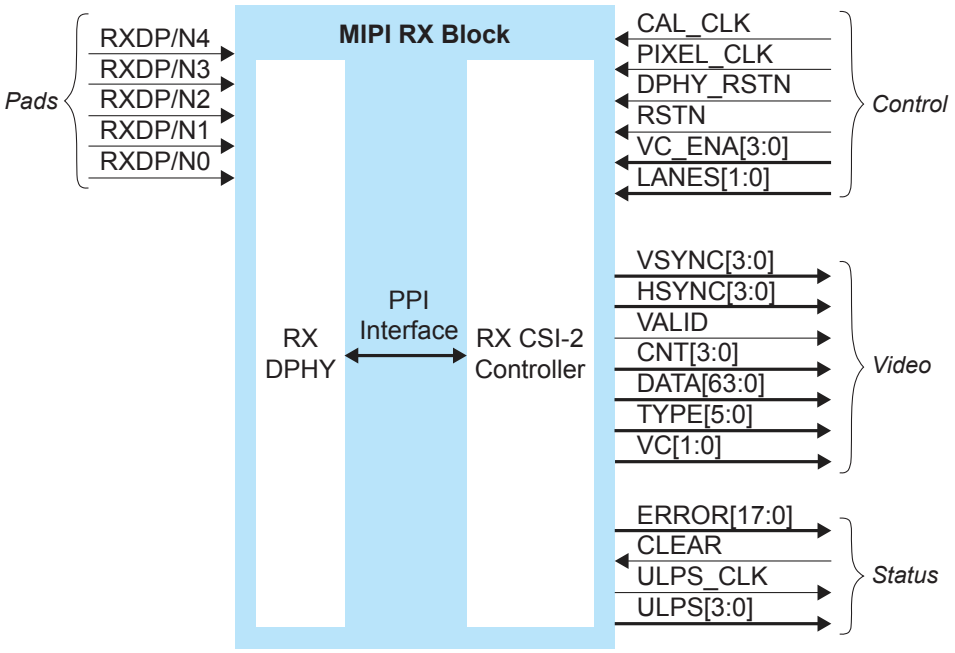
Table 24: MIPI TX TYPE[5:0]

TYPE[5:0]	Data Type	Pixel Data Bits per Pixel Clock	Pixels per Clock	Bits per Pixel	Maximum Data Pixels per Line
0x20	RGB444	48	4	12	2,880
0x21	RGB555	60	4	15	2,880
0x22	RGB565	64	4	16	2,880
0x23	RGB666	54	3	18	2,556
0x24	RGB888	48	2	24	1,920
0x28	RAW6	60	10	6	7,680
0x29	RAW7	56	8	7	6,576
0x2A	RAW8	64	8	8	5,760
0x2B	RAW10	60	6	10	4,608
0x2C	RAW12	60	5	12	3,840
0x2D	RAW14	56	4	14	3,288
0x18	YUV420 8 bit	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x19	YUV420 10 bit	Odd line: 60 Even line: 40	Odd line: 6 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1A	Legacy YUV420 8 bit	48	4	8, 16	3,840
0x1C	YUV420 8 bit (CSPS)	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x1D	YUV420 10 bit (CSPS)	Odd line: 60 Even line: 40	Odd line: 6 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1E	YUV422 8 bit	64	4	8, 24	2,880
0x1F	YUV422 10 bit	40	2	10, 30	2,304
0x30 - 37	User defined 8 bit	64	8	8	5,760

MIPI RX

The MIPI RX is a receiver interface that translates HSSI signals from the board to video data in the Trion® core. Five high-speed differential pin pairs (one clock, four data), each of which represent a lane, connect to the board. Control, video, and status signals connect from the MIPI interface to the core.

Figure 19: MIPI RX x4 Block Diagram



The control signals determine the clocking, how many transceiver lanes are used, and how many virtual channels are enabled. All control signals are required except the two reset signals. The reset signals are optional, however, you must use both signals or neither.

The video signals send the decoded video data to the core. All video signals must fully support the MIPI standard.

The status signals provide optional status and error information about the MIPI RX interface operation.

Figure 20: MIPI RX Interface Block Diagram

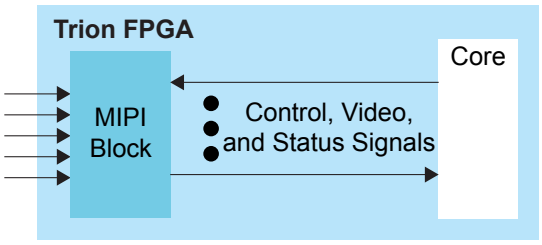


Table 25: MIPI RX Control Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
CAL_CLK	Input	N/A	Used for D-PHY calibration; must be between 80 and 120 MHz.
PIXEL_CLK	Input	N/A	Clock used for transferring data to the core from the MIPI RX block. The frequency based on the number of lanes and video format.
DPHY_RSTN	Input	N/A	(Optional) Reset for the D-PHY logic, active low. Must be used if RSTN is used. See MIPI Reset Timing on page 49.
RSTN	Input	N/A	(Optional) Reset for the CSI-2 controller logic, active low. Must be used if DPHY_RSTN is used. See MIPI Reset Timing on page 49.
VC_ENA[3:0]	Input	PIXEL_CLK	Enables different VC channels by setting their index high.
LANES[1:0]	Input	PIXEL_CLK	Determines the number of lanes enabled: 00: lane 0 01: lanes 0 and 1 11: all lanes Can only be set during reset.

Table 26: MIPI RX Video Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
VSYNC[3:0]	Output	PIXEL_CLK	Vsync bus. High if vsync is active for this VC.
HSYNC[3:0]	Output	PIXEL_CLK	Hsync bus. High if hsync is active for this VC
VALID	Output	PIXEL_CLK	Valid signal.
CNT[3:0]	Output	PIXEL_CLK	Number of valid pixels contained in the pixel data.
DATA[63:0]	Output	PIXEL_CLK	Video data, format depends on data type. New data every pixel clock.
TYPE[5:0]	Output	PIXEL_CLK	Video data type.
VC[1:0]	Output	PIXEL_CLK	Virtual channel (VC).

Table 27: MIPI RX Status Signals (Interface to FPGA Fabric)

Signal	Direction	Signal Interface	Clock Domain	Notes
ERROR[17:0]	Output	IN	PIXEL_CLK	Error bus register. Refer to Table 28: MIPI RX Error Signals (ERROR[17:0]) on page 28 for details.
CLEAR	Input	OUT	PIXEL_CLK	Reset the error registers.
ULPS_CLK	Output	IN	PIXEL_CLK	High when the clock lane is in the Ultra-Low-Power State (ULPS).
ULPS[3:0]	Output	IN	PIXEL_CLK	High when the lane is in the ULPS mode.

Table 28: MIPI RX Error Signals (ERROR[17:0])

Bit	Name	Description
0	ERR_ESC	Escape Entry Error. Asserted when an unrecognized escape entry command is received.
1	CRC_ERROR_VC0	CRC Error VC0. Set to 1 when a checksum error occurs.
2	CRC_ERROR_VC1	CRC Error VC1. Set to 1 when a checksum error occurs.
3	CRC_ERROR_VC2	CRC Error VC2. Set to 1 when a checksum error occurs.
4	CRC_ERROR_VC3	CRC Error VC3. Set to 1 when a checksum error occurs.
5	HS_RX_TIMEOUT_ERR	HS RX Timeout Error. The protocol should time out when no EoT is received within a certain period in HS RX mode.
6	ECC_1BIT_ERROR	ECC Single Bit Error. Set to 1 when there is a single bit error.
7	ECC_2BIT_ERROR	ECC 2 Bit Error. Set to 1 if there is a 2 bit error in the packet.
8	ECCBIT_ERROR	ECC Error. Asserted when an error exists in the ECC.
9	ECC_NO_ERROR	ECC No Error. Asserted when an ECC is computed with a result zero. This bit is high when the receiver is receiving data correctly.
10	FRAME_SYNC_ERROR	Frame Sync Error. Asserted when a frame end is not paired with a frame start on the same virtual channel.
11	INVLD_PKT_LEN	Invalid Packet Length. Set to 1 if there is an invalid packet length.
12	INVLD_VC	Invalid VC ID. Set to 1 if there is an invalid CSI VC ID.
13	INVALID_DATA_TYPE	Invalid Data Type. Set to 1 if the received data is invalid.
14	ERR_FRAME	Error In Frame. Asserted when VSYNC END received when CRC error is present in the data packet.
15	CONTROL_ERR	Control Error. Asserted when an incorrect line state sequence is detected.
16	SOT_ERR	Start-of-Transmission (SoT) Error. Corrupted high-speed SoT leader sequence while proper synchronization can still be achieved.
17	SOT_SYNC_ERR	SoT Synchronization Error. Corrupted high-speed SoT leader sequence while proper synchronization cannot be expected.

Table 29: MIPI RX Pads

Pad	Direction	Description
RXDP[4:0]	Output	MIPI transceiver P pads.
RXDN[4:0]	Output	MIPI transceiver N pads.

Table 30: MIPI RX Settings in Efinity® Interface Designer

Tab	Parameter	Choices	Notes
Control	DPHY Calibration Clock Pin Name	User defined	
	Invert DPHY Calibration Clock	On or Off	
	Pixel Clock Pin Name	User defined	
	Invert Pixel Clock	On or Off	

Tab	Parameter	Choices	Notes
Status	Enable Status	On or Off	Indicate whether you want to use the status pins.
Lane Mapping	RXD0, RXD1, RXD2, RXD3, RXD4	clk, data0, data1, data2, or data3	Map the physical lane to a clock or data lane.
	Swap P&N Pin	On or Off	Reverse the P and N pins for the physical lane.
Timing	Calibration Clock Freq (MHz)	User defined	Specify a number between 80 and 120 MHz.
	Clock Timer ($T_{CLK-SETTLE}$)	40 - 2,590 ns	Changes the MIPI receiver timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 30.
	Data Timer ($T_{HS-SETTLE}$)	40 - 2,590 ns	Changes the MIPI receiver timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 30.

MIPI RX Video Data TYPE[5:0] Settings

The video data type can only be changed when HSYNC is low.

Table 31: MIPI RX TYPE[5:0]

TYPE[5:0]	Data Type	Pixel Data Bits per Pixel Clock	Pixels per Clock	Bits per Pixel	Maximum Data Pixels per Line
0x20	RGB444	48	4	12	2,880
0x21	RGB555	60	4	15	2,880
0x22	RGB565	64	4	16	2,880
0x23	RGB666	54	3	18	2,556
0x24	RGB888	48	2	24	1,920
0x28	RAW6	48	8	6	7,680
0x29	RAW7	56	8	7	6,576
0x2A	RAW8	64	8	8	5,760
0x2B	RAW10	40	4	10	4,608
0x2C	RAW12	48	4	12	3,840
0x2D	RAW14	56	4	14	3,288
0x18	YUV420 8 bit	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x19	YUV420 10 bit	Odd line: 40 Even line: 40	Odd line: 4 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1A	Legacy YUV420 8 bit	48	4	8, 16	3,840
0x1C	YUV420 8 bit (CSPS)	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x1D	YUV420 10 bit (CSPS)	Odd line: 40 Even line: 40	Odd line: 4 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1E	YUV422 8 bit	64	4	8, 24	2,880
0x1F	YUV422 10 bit	40	2	10, 30	2,304
0x30 - 37	User defined 8 bit	64	8	8	5,760

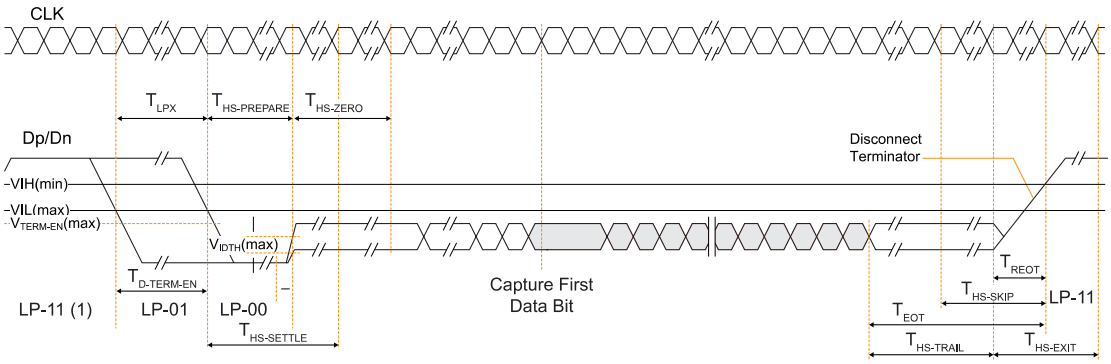
D-PHY Timing Parameters

During CSI-2 data transmission, the MIPI D-PHY alternates between low power mode and high-speed mode. The D-PHY specification defines timing parameters to facilitate the correct hand-shaking between the MIPI TX and MIPI RX during mode transitions.

You set the timing parameters to correspond to the specifications of your hardware in the Efinity® Interface Designer.

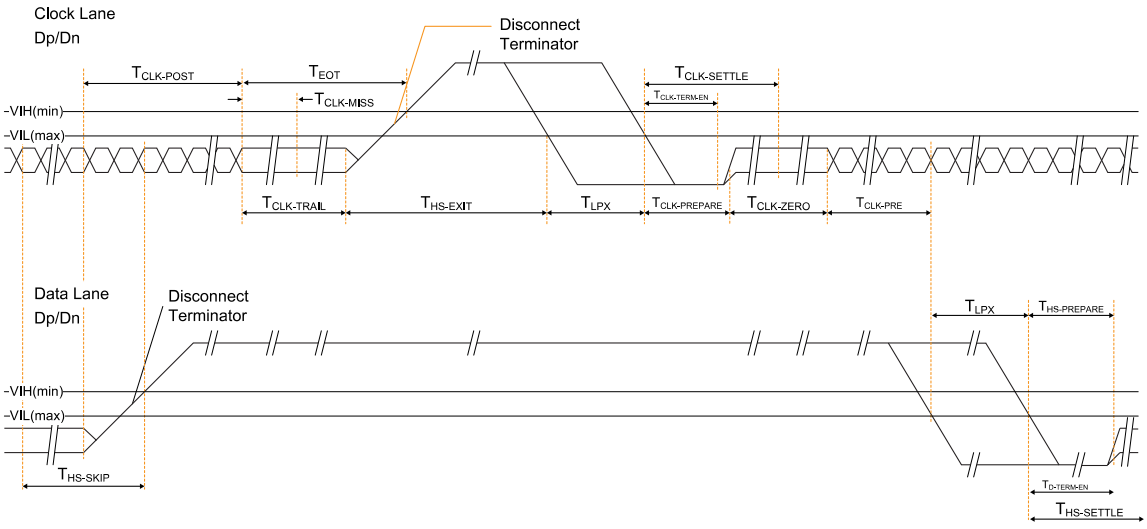
- *RX parameters*—$T_{CLK-SETTLE}$, $T_{HS-SETTLE}$ (see Table 25: MIPI RX Control Signals (Interface to FPGA Fabric) on page 27)
- *TX parameters*—$T_{CLK-POST}$, $T_{CLK-TRAIL}$, $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, $T_{CLK-PRE}$, $T_{HS-PREPARE}$, $T_{HS-ZERO}$, $T_{HS-TRAIL}$ (see Table 23: MIPI TX Settings in Efinity Interface Designer on page 24)

Figure 21: High-Speed Data Transmission in Bursts Waveform



Note:
1. To enter high-speed mode, the D-PHY goes through states LP-11, LP-01, and LP-00. The D-PHY generates LP-11 to exit high-speed mode.

Figure 22: Switching the Clock Lane between Clock Transmission and Low Power Mode Waveform

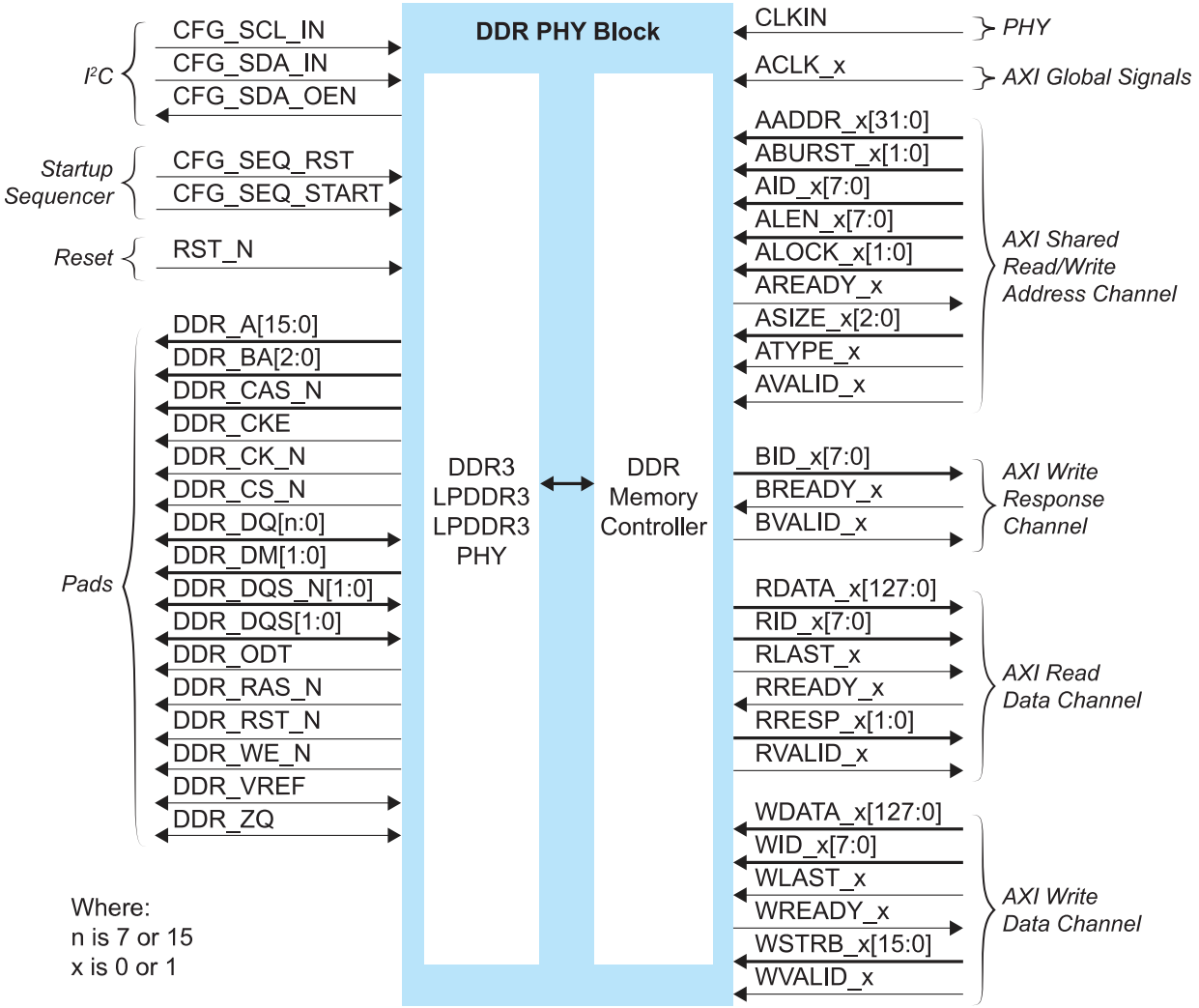


DDR DRAM

T20 FPGAs have a x16 DDR PHY interface supporting DDR3, DDR3L, DDR3U, LPDDR3, and LPDDR2 as well as a memory controller hard IP block. The DDR PHY supports data rates up to 1066 Mbps per lane. The memory controller provides two 128 bit AXI buses to communicate with the FPGA core.

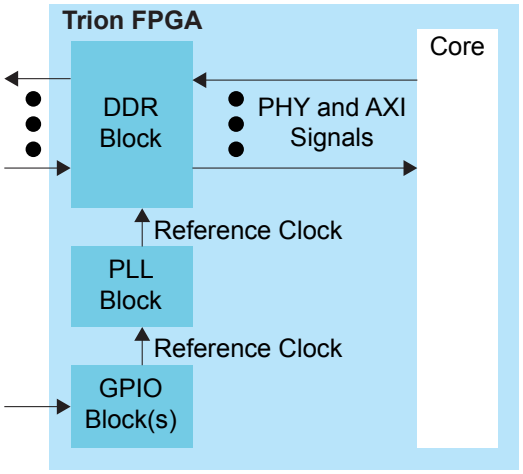
Note: The DDR PHY and controller are hard blocks; you cannot bypass the DDR DRAM memory controller to access the PHY directly for non-DDR memory controller applications.

Figure 23: DDR DRAM Block Diagram



The DDR DRAM block supports an I²C calibration bus that can read/write the DDR configuration registers. You can use this bus to fine tune the DDR PHY for high performance.

Figure 24: DDR DRAM Interface Block Diagram



Note: Although the PLL reference clock can be driven by I/O pads or the core clock tree, Efinix recommends using an I/O pad. The clock tree may induce additional jitter and degrade the DDR performance. Refer to PLL on page 15 for more information about the PLL block.

Table 32: DDR DRAM Performance

DDR DRAM Interface	Voltage (V)	Maximum Data Rate (Mbps) per Lane
DDR3 DDR3L DDR3U	1.5 1.35 1.25	1066
LPDDR3	1.2	1066
LPDDR2	1.2	1066

Table 33: PHY Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
CLKIN	Input	N/A	High-speed clock to drive the DDR PHY. A PLL must generate this clock. The clock runs at half of the PHY data rate (for example, 800 Mbps requires a 400 MHz clock). The DDR DRAM block uses the PLL_BR0 resource as the PHY clock. When used as the PHY clock, PLL_BR0 CLKOUT0 can only drive the DDR PHY and you cannot use CLKOUT1 and CLKOUT2.

Table 34: AXI Gobal Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
ACLK_0, ACLK_1	Input	N/A	AXI clock inputs.

Table 35: AXI Shared Read/Write Signals (Interface to FPGA Fabric)

Signal x is 0 or 1	Direction	Clock Domain	Description
AADDR_*x*[31:0]	Input	ACLK_x	Address. ATYPE defines whether it is a read or write address. It gives the address of the first transfer in a burst transaction.
ABURST_*x*[1:0]	Input	ACLK_x	Burst type. The burst type and the size determine how the address for each transfer within the burst is calculated.
AID_*x*[7:0]	Input	ACLK_x	Address ID. This signal identifies the group of address signals. Depends on ATYPE, the ID can be for a read or write address group.
ALEN_*x*[7:0]	Input	ACLK_x	Burst length. This signal indicates the number of transfers in a burst.
ALOCK_*x*[1:0]	Input	ACLK_x	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
AREADY_*x*	Output	ACLK_x	Address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
ASIZE_*x*[2:0]	Input	ACLK_x	Burst size. This signal indicates the size of each transfer in the burst.
ATYPE_*x*	Input	ACLK_x	This signal distinguishes whether is it is a read or write operation. 0 = read and 1 = write.
AVALID_*x*	Input	ACLK_x	Address valid. This signal indicates that the channel is signaling valid address and control information.

Table 36: AXI Write Response Channel Signals (Interface to FPGA Fabric)

Signal x is 0 or 1	Direction	Clock Domain	Description
BID_*x*[7:0]	Output	ACLK_x	Response ID tag. This signal is the ID tag of the write response.
BREADY_*x*	Input	ACLK_x	Response ready. This signal indicates that the master can accept a write response.
BVALID_*x*	Output	ACLK_x	Write response valid. This signal indicates that the channel is signaling a valid write response.

Table 37: AXI Read Data Channel Signals (Interface to FPGA Fabric)

Signal x is 0 or 1	Direction	Clock Domain	Description
RDATA_*x*[127:0]	Output	ACLK_x	Read data.
RID_*x*[7:0]	Output	ACLK_x	Read ID tag. This signal is the identification tag for the read data group of signals generated by the slave.
RLAST_*x*	Output	ACLK_x	Read last. This signal indicates the last transfer in a read burst.
RREADY_*x*	Input	ACLK_x	Read ready. This signal indicates that the master can accept the read data and response information.
RRESP_*x*[1:0]	Output	ACLK_x	Read response. This signal indicates the status of the read transfer.
RVALID_*x*	Output	ACLK_x	Read valid. This signal indicates that the channel is signaling the required read data.

Table 38: AXI Write Data Channel Signals (Interface to FPGA Fabric)

Signal x is 0 or 1	Direction	Clock Domain	Description
WDATA_*x*[127:0]	Input	ACLK_x	Write data.
WID_*x*[7:0]	Input	ACLK_x	Write ID tag. This signal is the ID tag of the write data transfer.
WLAST_*x*	Input	ACLK_x	Write last. This signal indicates the last transfer in a write burst.
WREADY_*x*	Output	ACLK_x	Write ready. This signal indicates that the slave can accept the write data.
WSTRB_*x*[15:0]	Input	ACLK_x	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
WVALID_*x*	Input	ACLK_x	Write valid. This signal indicates that valid write data and strobes are available.

Table 39: DDR DRAM I^2C Interface Signals

Signal	Direction	Description
CFG_SCL_IN	Input	Clock input.
CFG_SDA_IN	Input	Data input.
CFG_SDA_OEN	Output	SDA output enable.

Table 40: DDR DRAM Startup Sequencer Signals

Signal	Direction	Description
CFG_SEQ_RST	Input	Active-high DDR configuration controller reset.
CFG_SEQ_START	Input	Start the DDR configuration controller.

Table 41: DDR DRAM Reset Signal

Signal	Direction	Description
RST_N	Input	Active-low master DDR DRAM reset. After you de-assert RST_N, you need to reconfigure and initialize before performing memory operations.

Table 42: DDR DRAM Pads

Signal	Direction	Description
DDR_A[15:0]	Output	Address signals to the memories.
DDR_BA[2:0]	Output	Bank signals to/from the memories.
DDR_CAS_N	Output	Active-low column address strobe signal to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK	Output	Active-high clock signals to/from the memories. The clock to the memories and to the memory controller must be the same clock frequency and phase.
DDR_CK_N	Output	Active-low clock signals to/from the memories.The clock to the memories and to the memory controller must be the same clock frequency and phase.
DDR_CS_N	Output	Active-low chip select signals to the memories.

Signal	Direction	Description
DDR_DQ[*n*:0]	Bidirectional	Data bus to/from the memories. For writes, the pad drives these signals. For reads, the memory drives these signals. These signals are connected to the DQ inputs on the memories. *n* is 7 or 15 depending on the DQ Width Configuration setting.
DDR_DM[*n*]	Output	Active-high data-mask signals to the memories. *n* is 0 or 1:0 depending on the DQ width.
DDR_DQS_N[*n*:0]	Bidirectional	Differential data strobes to/from the memories. For writes, the pad drives these signals. For reads, the memory drives these signals. These signals are connected to the DQS inputs on the memories. *n* is 0 or 1:0 depending on the DQ width.
DDR_DQS[*n*:0]	Bidirectional	
DDR_ODT	Output	ODT signal to the memories.
DDR_RAS_N	Output	Active-low row address strobe signal to the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_WE_N	Output	Active-low write enable strobe signal to the memories.
DDR_VREF	Bidirectional	Reference voltage.
DDR_ZQ	Bidirectional	ZQ calibration pin.

DDR Interface Designer Settings

The following tables describe the settings for the DDR block in the Interface Designer.

Table 43: Base Tab

Parameter	Choices	Notes
DDR Resource	None, DDR_0	Only one resource available.
Instance Name	User defined	Indicate the DDR instance name. This name is the prefix for all DDR signals.
Memory Type	DDR3, LPDDR2, LPDDR3	Choose the memory type you want to use.

Table 44: Configuration Tab

Parameter	Choices	Notes
Select Preset		The **Select Preset** button opens a list of popular DDR memory configurations. Choose a preset to populate the configuration choices. If you do not want to use a preset, you can specify the memory configuration manually.
DQ Width	x8, x16	DQ bus width.
Type	DDR3, LPDDR2, LPDDR3	Memory type.
DDR3		
Speed Grade	1066E, 1066F, 1066G, 800D, 800E	Memory speed.
Width	x8, x16	Memory width.
Density	1G, 2G, 4G, 8G	Memory density.
LPDDR2		
Speed Grade	400, 533, 667, 800, 1066	Memory speed.

Parameter	Choices	Notes
Width	x16	Memory width.
Density	512MB, 1G, 2G, 4G	Memory density.
LPDDR3		
Speed Grade	800, 1066	Memory speed.
Width	x16	Memory width.
Density	4G, 8G	Memory density.

Table 45: Advanced Options Tab - FPGA Setting Subtab

Parameter	Choices	Notes
FPGA Input Termination	Varies depending on the memory type	Specify the termination value for the FPGA input/output pins.
FPGA Output Termination		

Table 46: Advanced Options Tab - Memory Mode Register Settings Subtab

Parameter	Choices	Notes
DDR3		
Burst Length	8	Specify the burst length (only 8 is supported).
DLL Precharge Power Down	On, Off	Specify whether the DLL in the memory device is off or on during precharge power-down.
Memory Auto Self-Refresh	Auto, Manual	Turn on or off auto-self refresh feature in memory device.
Memory CAS Latency (CL)	5 - 15	Specify the number of clock cycle between read command and the availability of output data at the memory device.
Memory Write CAS Latency (CWL)	5 - 12	Specify the number of clock cycle from the releasing of the internal write to the latching of the first data in at the memory device.
Memory Dynamic ODT (Rtt_WR)	Off, RZQ/2, RZQ/4	Specify the mode of dynamic ODT feature of memory device.
Memory Input Termination (Rtt_nom)	Off, RZQ/2, RZQ/4, RZQ/6, RZQ/8, RZQ/12	Specify the input termination value of the memory device.
Memory Output Termination	RZQ/6, RZQ/7	Specify the output termination value of the memory device.
Read Burst Type	Interleaved, Sequential	Specify whether accesses within a give burst are in sequential or interleaved order.
Sef-Refresh Temperature	Extended, Normal	Specify whether the self refresh temperature is normal or extended mode.
LPDDR2		
Burst Length	8	Specify the burst length (only 8 is supported).
Output Drive Strength	34.3, 40, 48, 50, 80, 120	Specify the output termination value of memory device.
Read Burst Type	Interleaved, Sequential	Specify whether accesses within a given burst are in sequential or interleaved order.

Parameter	Choices	Notes
Read/Write Latency	RL=3/WL=1, RL=4/WL=2 RL=5/WL=2, RL=6/WL=3 RL=7/WL=4, RL=8/WL=4	Specify the read/write latency of the memory device.
LPDDR3		
DQ ODT	Disable, RZQ1, RZQ2, RZQ4	Specify the input termination value of memory device.
Output Drive Strength	34.3 34.3 pull-down/40 pull up 34.3 pull-down/48 pull up 40 40 pull down/48 pull up 48	Specify the output termination value of memory device.
Read/Write Latency	RL=3/WL=1, RL=6/WL=3 RL=8/WL=4, RL=9/WL=5	Specify the read/write latency of the memory device.

Table 47: Advanced Options Tab - Memory Timing Settings Subtab

Parameter	Choices	Notes
tFAW, Four Bank Active Window (ns)	User defined	Enter the timing parameters from the memory device's data sheet.
tRAS, Active to Precharge Command Period (ns)		
tRC, Active to Actrive or REF Command Period (ns)		
tRCD, Active to Read or Write Delay (ns)		
tREFI, Average Periodic Refresh Interval (ns)		
tRFC, Refresh to Active or Refresh to Refresh Delay (ns)		
tRP, Precharge Command Period (ns)		
tRRD, Active to Active Command Period (ns)		
tRTP, Internal Read to Precharge Delay (ns)		
tWTR, Internal Write to Read Command Delay (ns)		

Table 48: Advanced Options Tab - Controller Settings Subtab

Parameter	Choices	Notes
Controller to Memory Address Mapping	BANK-ROW-COL ROW-BANK-COL ROW-COL_HIGH-BANK-COL_LOW	Specify the mapping between the address of AXI interface and column, row, and bank address of memory device.
Enable Auto Power Down	Active, Off, Pre-Charge	Specify whether to allow automatic entry into power-down mode (pre-charge or active) after a specific amount of idle time.
Enable Self Refresh Controls	No, Yes	Specify whether to enable automatic entry into self-refresh mode after specific amount of idle period.

Table 49: Advanced Options Tab - Gate Delay Tuning Settings Subtab

Parameter	Choices	Notes
Enable Gate Delay Override	On or off	Turning this option on allows you to fine-tine the gate-delay values. This is an expert only setting.

Parameter	Choices	Notes
Gate Coarse Delay Tuning	0 - 5	
Gate Fine Delay Tuning	0 - 255	

Table 50: Control Tab

Option	Notes
Disable Control	When selected, this option disables calibration and user reset.
Enable Calibration	Turn on to enable optional PHY calibration pins (master reset, SCL, and SDA pins). Efinix recommends that you use the default pin names. The names are prefixed with the instance name you specified in the Base tab.
User Reset	Turn on to enable optional reset pins (master reset and sequencer start/reset). Efinix recommends that you use the default pin names. The names are prefixed with the instance name you specified in the Base tab.

Table 51: AXI 0 and AXI 1 Tabs

Parameter	Choices	Notes
Enable Target 0 Enable Target 1	On or off	Turn on to enable the AXI 0 interface. Turn on to enable the AXI 0 interface.
AXI Clock Input Pin name	User defined	Specify the name of the AXI input clock pin.
Invert AXI Clock Input	On or off	Turn on to invert the AXI clock.
Shared Read/Write Address Channel tab Write Response Channel tab Read Data Channel tab Write Data Channel tab	User defined	This tab defines the AXI signal names. Efinix recommends that you use the default names. The signals are prefixed with the instance name you specified in the Base tab.

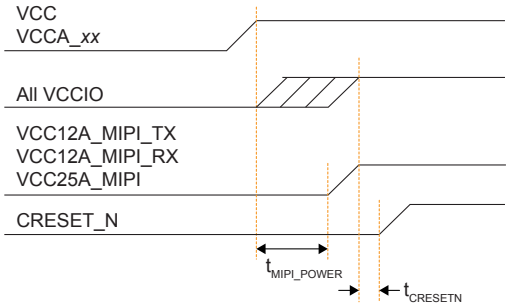
Power Up Sequence

Efinix® recommends following this power up sequence when powering Trion® FPGAs:

1. Power up VCC and VCCA_*xx* first.
2. When VCC and VCCA_*xx* are stable, power up all VCCIO pins. There is no specific timing delay between the VCCIO pins.
3. Apply power to VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI at least t_{MIPI_POWER} after VCC is stable.
4. After all power supplies are stable, hold CRESET_N high or trigger CRESET_N from low to high for a duration of t_{CRESET_N} to trigger active SPI programming (the FPGA loads the configuration data from an external flash device).

Note: Refer to Configuration Timing on page 51 and MIPI Power-Up Timing on page 49 for timing information.

Figure 25: Trion® FPGA Power Up Sequence

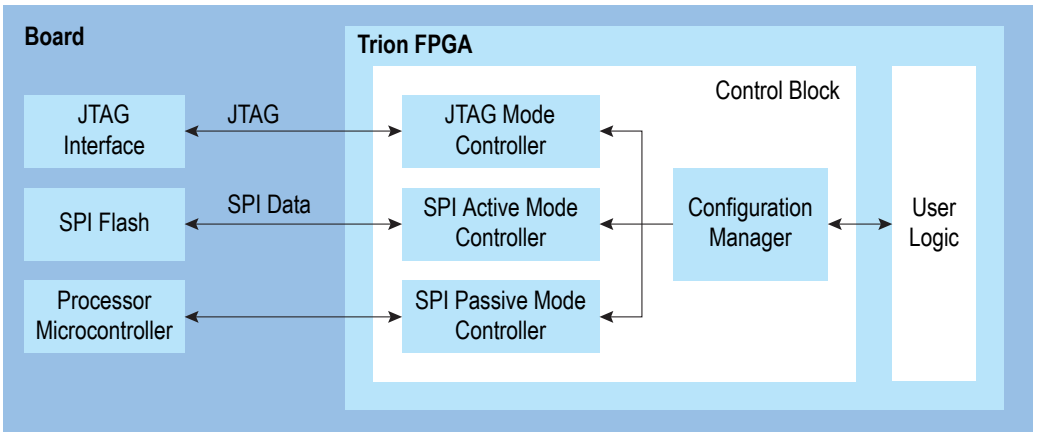


Configuration

The T20 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the T20 FPGA(s) in active, passive, or JTAG mode.

Learn more: Refer to AN 006: Configuring Trion FPGAs for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 26: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 μs before issuing a fast read command to read the content of SPI flash from address 24h'000000.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 52: T20 Configuration Modes by Package

Configuration Mode	Width	BGA256	BGA169	BGA324
Active	x1	✓	✓	✓[7]
	x2	✓	✓	✓
	x4	✓	✓	✓
Passive	x1	✓	✓	✓
	x2	✓	✓	✓
	x4	✓	✓	✓
	x8	✓		✓
	x16	✓		✓
	x32	✓		✓
JTAG	x1	✓	✓	✓

Learn more: Refer to AN 006: Configuring Trion FPGAs for more information.

Mask-Programmable Memory Option

The T20 FPGA is equipped with one-time programmable MPM. With this feature, you use on-chip MPM instead of an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

[7] This package does not support active SPI multi-image configuration in x1 mode. Instead, use x2 or x4, or alternatively, use the internal reconfiguration feature as described in AN 010: Using the Internal Reconfiguration Feature to Remotely Update Trion FPGAs.

DC and Switching Characteristics (BGA169 and BGA256)

T20 FPGAs in BGA169 and BGA256 packages have the following DC and switching characteristics.

Table 53: Absolute Maximum Ratings

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	-0.5	2.75	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.2 V TX analog power supply for MIPI	-0.5	1.42	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.2 V RX analog power supply for MIPI	-0.5	1.42	V
T_J	Operating junction temperature	-40	125	°C

Table 54: Recommended Operating Conditions [8]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.15	1.2	1.25	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.15	1.2	1.25	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	2.38	2.5	2.63	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.2 V TX analog power supply for MIPI	1.15	1.2	1.25	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.2 V RX analog power supply for MIPI	1.15	1.2	1.25	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

[8] Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.

Table 55: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	0.01	10	V/ms

Table 56: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 57: Single-Ended I/O DC Electrical Characteristics

Voltage (V)	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 58: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	4.4	5.1
2	19.1	10.5	12.2	10.5	5.8	6.8
3	23.9	13.3	15.2	13.4	7.3	8.6
4	28.7	15.8	18.2	15.9	8.6	10.3

Table 59: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4

Table 60: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

Voltage (V)	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	±10	±10

Table 61: LVDS Pins as Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	Drive Strength	
	I_{OH} (mA)	I_{OL} (mA)
3.3 V	37.6	22

Table 62: Block RAM Characteristics

Symbol	Description	C4, I4 Speed Grades	C3 Speed Grades	Units
f_{MAX}	Block RAM maximum frequency.	400	310	MHz

Table 63: DSP Block Characteristics

Symbol	Description	C4, I4 Speed Grades	C3 Speed Grades	Units
f_{MAX}	DSP block maximum frequency.	400	310	MHz

DC and Switching Characteristics (BGA324 and BGA400)

T20 FPGAs in BGA324 and BGA400 packages have the following DC and switching characteristics.

Important: All specifications are preliminary and pending hardware characterization.

Table 64: Absolute Maximum Ratings

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	-0.5	2.75	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.2 V TX analog power supply for MIPI	-0.5	1.42	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.2 V RX analog power supply for MIPI	-0.5	1.42	V
T_J	Operating junction temperature	-40	125	°C

(9) Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.

Table 65: Recommended Operating Conditions [9]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.15	1.2	1.25	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.15	1.2	1.25	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	2.38	2.5	2.63	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.2 V TX analog power supply for MIPI	1.15	1.2	1.25	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.2 V RX analog power supply for MIPI	1.15	1.2	1.25	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

Table 66: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	0.01	10	V/ms

Table 67: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 68: Single-Ended I/O DC Electrical Characteristics

Voltage (V)	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 69: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	4.4	5.1
2	19.1	10.5	12.2	10.5	5.8	6.8
3	23.9	13.3	15.2	13.4	7.3	8.6
4	28.7	15.8	18.2	15.9	8.6	10.3

Table 70: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 71: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

Voltage (V)	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	±10	±10

Table 72: LVDS Pins as Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	Drive Strength	
	I_{OH} (mA)	I_{OL} (mA)
3.3 V	37.6	22

Table 73: Block RAM Characteristics

Symbol	Description	C4, I4 Speed Grades	C3 Speed Grades	Units
f_{MAX}	Block RAM maximum frequency.	400	310	MHz

Table 74: DSP Block Characteristics

Symbol	Description	C4, I4 Speed Grades	C3 Speed Grades	Units
f_{MAX}	DSP block maximum frequency.	400	310	MHz

LVDS I/O Electrical Specifications

The LVDS pins comply with the EIA/TIA electrical specifications.

Table 75: LVDS I/O Electrical Specifications

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CCIO}	LVDS I/O Supply Voltage	–	2.97	3.3	3.63	V
LVDS TX						
V_{OD}	Output Differential Voltage	–	250	–	450	mV
ΔV_{OD}	Change in V_{OD}	–	–	–	50	mV
V_{OCM}	Output Common Mode Voltage	RT = 100 Ω	1,125	1,250	1,375	mV
ΔV_{OCM}	Change in V_{OCM}	–	–	–	50	mV
V_{OH}	Output High Voltage	RT = 100 Ω	–	–	1475	mV
V_{OL}	Output Low Voltage	RT = 100 Ω	925	–	–	mV
I_{SAB}	Output Short Circuit Current	–	–	–	24	mA
LVDS RX[10]						
V_{ID}	Input Differential Voltage	–	100	–	600	mV
V_{ICM}	Input Common Mode Voltage	–	100	–	2,000	mV
V_{TH}	Differential Input Threshold	–	-100	–	100	mV
I_{IL}	Input Leakage Current	–	–	–	20	µA

ESD Performance

Refer to the Trion Reliability Report for ESD performance data.

[10] The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standard.

MIPI Electrical Specifications and Timing

The MIPI D-PHY transmitter and receiver are compliant to the MIPI Alliance Specification for D-PHY Revision 1.1.

Table 76: High–Speed MIPI D–PHY Transmitter (TX) DC Specifications[11]

Parameter	Description	Min	Typ	Max	Unit
V_{CMTX}	High–speed transmit static common–mode voltage	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential–1 or Differential–0	–	–	5	mV
$\|V_{OD}\|$	High–speed transmit differential voltage	140	200	270	mV
$\|\Delta V_{CMTX}\|$	VOD mismatch when output is Differential–1 or Differential–0	–	–	14	mV
V_{OHHS}	High–speed output high voltage	–	–	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	–	–	10	%

Table 77: Low–Power MIPI D–PHY Transmitter (TX) DC Specifications[11]

Parameter	Description	Min	Typ	Max	Unit
V_{OH}	Thevenin output high level	0.99	–	1.21	V
V_{OL}	Thevenin output low level	–50	–	50	mV
Z_{OLP}	Output impedance of low–power transmitter	110	–	–	Ω

Table 78: High–Speed MIPI D–PHY Receiver (RX) DC Specifications[11]

Parameter	Description	Min	Typ	Max	Unit
$V_{CMRX(DC)}$	Common mode voltage high–speed receive mode	70	–	330	mV
V_{IDTH}	Differential input high threshold	–	–	70	mV
V_{IDTL}	Differential input low threshold	–70	–	–	mV
V_{IHHS}	Single–ended input high voltage	–	–	460	mV
V_{ILHS}	Single–ended input low voltage	–40	–	–	mV
$V_{TERM–EN}$	Single–ended threshold for high–speed termination enable	–	–	450	mV
Z_{ID}	Differential input impedance	80	100	125	Ω

[11] Pending hardware characterization.

Table 79: Low–Power MIPI D–PHY Receiver (RX) DC Specifications[11]

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880	–	–	mV
V_{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV
$V_{IL–ULPS}$	Logic 0 input voltage, ULP state	–	–	300	mV
V_{HYST}	Input hysteresis	25	–	–	mV

MIPI Power-Up Timing

Apply power to VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI at least t_{MIPI_POWER} after VCC is stable. See Power Up Sequence on page 39 for a power-up sequence diagram.

Table 80: MIPI Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{MIPI_POWER}	Minimum time after VCC and VCCA_*xx* are stable before powering VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI.	1	–	–	µs

MIPI Reset Timing

The MIPI RX and TX interfaces have two signals (RSTN and DPHY_RSTN) to reset the CSI-2 and D-PHY controller logic. These sginals are active low, and you should use them together to reset the MIPI interface.

After the rising edge of RSTN and DPHY_RSTN, the t_{INIT} time must be greater than or equal to 100 μs.

Figure 27: RSTN and DPHY_RSTN Timing Diagram

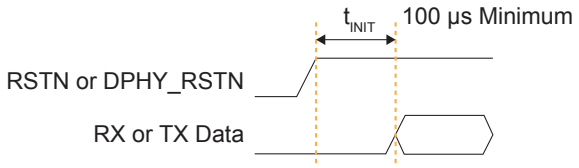


Table 81: MIPI Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{INIT}	Minimum time between the rising edge of RSTN or DPHY_RSTN and the start of MIPI RX or TX data.	100	–	–	µs

PLL Timing and AC Characteristics

The following tables describe the PLL timing and AC characteristics.

Table 82: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{IN}	Input clock frequency.	10	–	200	MHz
F_{OUT}	Output clock frequency.	0.24	–	500	MHz
F_{OUT}	Output clock frequency for PLL BR0 CLKOUT0 (DDR PHY input clock). BGA324 and BGA400 packages only.	0.24	–	800	MHz
F_{VCO}	PLL VCO frequency.	500	–	1,500	MHz
F_{PFD}	Phase frequency detector input frequency.	10	–	50	MHz

Table 83: PLL AC Characteristics[12]

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	45	50	55	%
t_{OPJIT} (PK - PK) [13]	Output clock period jitter (PK-PK).			200	ps
t_{LOCK}	PLL lock-in time.	–	–	0.5	ms

[12] Test conditions at 3.3 V and room temperature.
[13] The output jitter specification applies to the PLL jitter when an input jitter of 20 ps is applied.

Configuration Timing

The T20 FPGA has the following configuration timing specifications. Refer to AN 006: Configuring Trion FPGAs for detailed configuration information.

Timing Waveforms

Figure 28: SPI Active Mode (x1) Timing Sequence

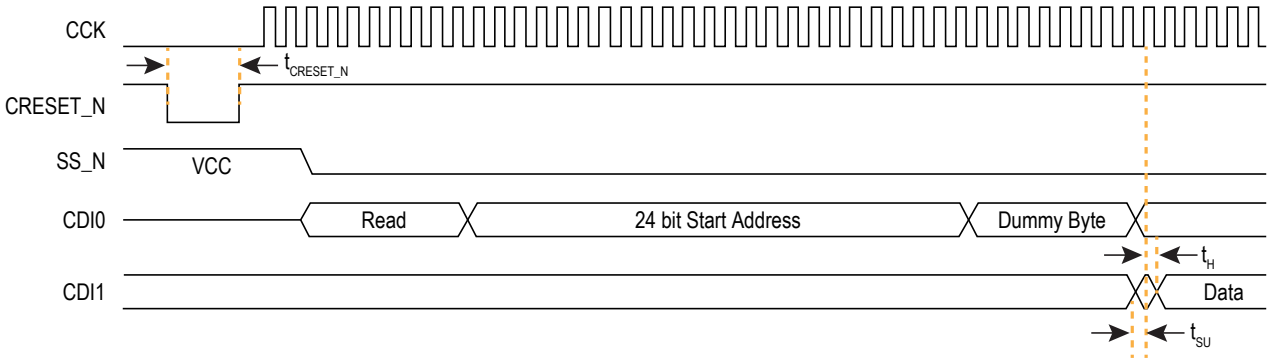


Figure 29: SPI Passive Mode (x1) Timing Sequence

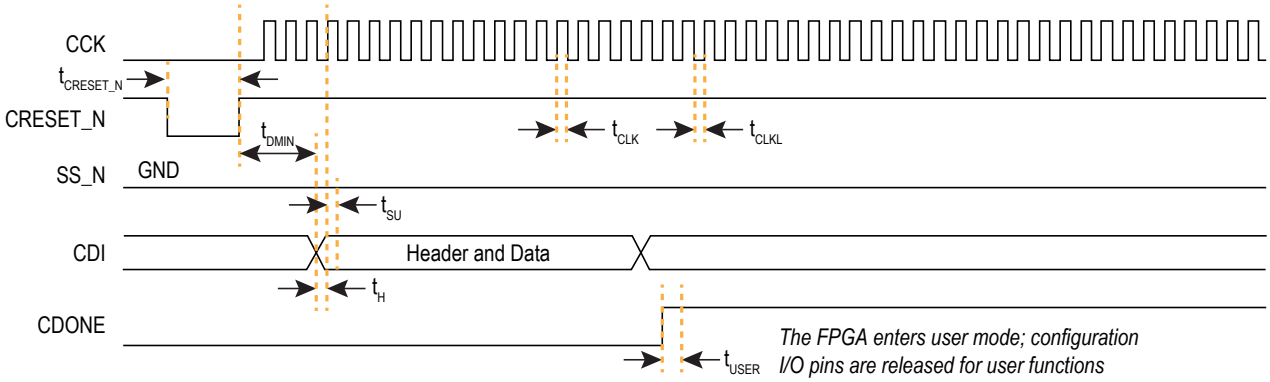
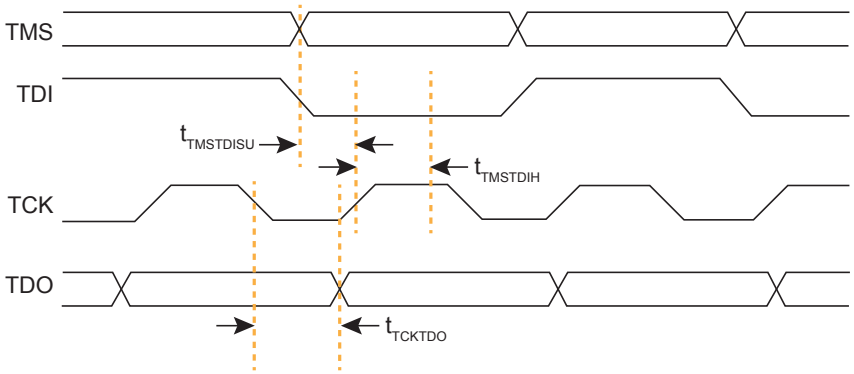


Figure 30: Boundary Scan Timing Waveform



Timing Parameters

Table 84: All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum creset_n low pulse width required to trigger re-configuration.	320	–	–	ns
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode.[14]	8	–	–	µs

Table 85: Active Mode

Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode configuration clock frequency.	DIV4	14	20	26	MHz
		DIV8	7	10	13	MHz
t_{SU}	Setup time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	7.5	–	–	ns
t_{H}	Hold time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	1	–	–	ns

Table 86: Passive Mode

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode configuration clock frequency.	–	–	100	MHz
t_{CLKH}	Configuration clock pulse width high.	4.8	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	4.8	–	–	ns
t_{SU}	Setup time.	6	–	–	ns
t_{H}	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Table 87: JTAG Mode (BGA169 and BGA256 Packages)

Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	33	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	1	–	–	ns
t_{TMSSU}	TMS setup time.	3	–	–	ns
t_{TMSH}	TMS hold time.	1	–	–	ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5[15]	ns

[14] The FPGA may go into user mode before t_{USER} has elapsed. However, Efinix recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

[15] 0 pf output loading.

Table 88: JTAG Mode (BGA324 Packages)

Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	33	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	2.5	–	–	ns
t_{TMSSU}	TMS setup time.	3	–	–	ns
t_{TMSH}	TMS hold time.	2.5	–	–	ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5	ns

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 89: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates location: TL: Top left, TR: Top right, BR: bottom right
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location: 1A: Bank 1A, 3E: Bank 3E 4A: Bank 4A (only for 3.3 V) , 4B: Bank 4B (only for 3.3 V)
VCCIO*xx_yy_zz*	Power	–	Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C VCCIO3C_TR_BR shorts banks 3C, TR, and BR
GND	Ground	–	Ground.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock resource. There are 5 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.
MREFCLK	Alternate	Input	MIPI PLL reference clock source.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: Indicates the bank; left (L), right (R), or bottom (B). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function. *zzzn*: Indicates LVDS TX or RX and number.
TXN*n*, TXP*n*	LVDS	I/O	LVDS transmitter (TX). *n*: Indicates the number.
RXN*n*, RXP*n*	LVDS	I/O	LVDS receiver (RX). *n*: Indicates the number.
CLKN*n*, CLKP*n*	LVDS	I/O	Dedicated LVDS receiver clock input. *n*: Indicates the number.
RXN*n*_EXTFB*n* RXP*n*_EXTFB*n*	LVDS	I/O	LVDS PLL external feedback. *n*: Indicates the number.
REF_RES	–	–	LVDS reference resistor pin. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground.

Table 90: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

Pins	Direction	Description	Use External Weak Pull-Up
CDONE	Output	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold CDONE low, the device will not enter user mode. CDONE is an open-drain output.	✓
CRESET_N	Input	Configuration reset pin (active low). Pulse CRESET_N low for t_{creset} time to reset the FPGA.	✓
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	✓
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	✓
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	✓
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	✓

Table 91: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. Connect to weak pull-up resistors if using default mode (x1).	✓
CBSEL[1:0]	Input	Optional multi-image selection input (if multi-image configuration mode is enabled).	N/A
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.	N/A
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O.	N/A
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for configuration.	✓

Pins	Direction	Description	Use External Weak Pull-Up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. This pin is active when there is a synchronization pattern mismatch or not found. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SS_N	Input	SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode. The FPGA senses the value of `SS_N` when it comes out of reset (pulse `CRESET_N` low to high). 0: Passive mode 1: Active mode	✓
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During configuration, rely on the external weak pull-up or drive this pin high.	✓
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. BGA49 and BGA81 packages only.	N/A

Table 92: MIPI Pinouts (Dedicated)

n Indicates the number. *L* indicates the lane

Function	Group	Direction	Description
VCC25A_MIPI0 VCC25A_MIPI1	Power	–	MIPI 2.5 V analog power supply.
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	Power	–	MIPI 1.2 V TX analog power supply.
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	Power	–	MIPI 1.2 V RX analog power supply.
GNDA_MIPI	Ground	–	Ground for MIPI analog power supply.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	MIPI	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	MIPI	I/O	MIPI differential receive data lane.
MREFCLK	Clock	Input	MIPI PLL reference clock source.

Table 93: DDR Pinouts (Dedicated)

n indicates the number.

Function	Direction	Description
VCCIO_DDR	–	DDR power supply.
DDR_A[*n*]	Output	Address signals to the memories.
DDR_BA[*n*]	Output	Bank signals to the memories.
DDR_CAS_N	Output	Active-low column address strobe signal to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[*n*]	I/O	Data bus to/from the memories.
DDR_DM[*n*]	Output	Active-high data-mask signals to the memories.
DDR_DQS_N[*n*]	I/O	Differential data strobes to/from the memories.
DDR_DQS[*n*]	I/O	Differential data strobes to/from the memories.
DDR_ODT	Output	ODT signal to the memories.
DDR_RAS_N	Output	Active-low row address strobe signal to the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_WE_N	Output	Active-low write enable strobe signal to the memories.
DDR_VREF	I/O	Reference voltage.
DDR_ZQ	I/O	ZQ calibration pin.

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The software-generated bitstream file configures the T20 FPGA. The software supports the Verilog HDL and VHDL languages.

T20 Interface Floorplans

Note: The numbers in the floorplan figures indicate the GPIO and LVDS number ranges. Some packages may not have all GPIO or LVDS pins in the range bonded out. Refer to the T20 pinout for information on which pins are available in each package.

Figure 31: Floorplan Diagram for FPGAs in BGA169 Packages (with MIPI)

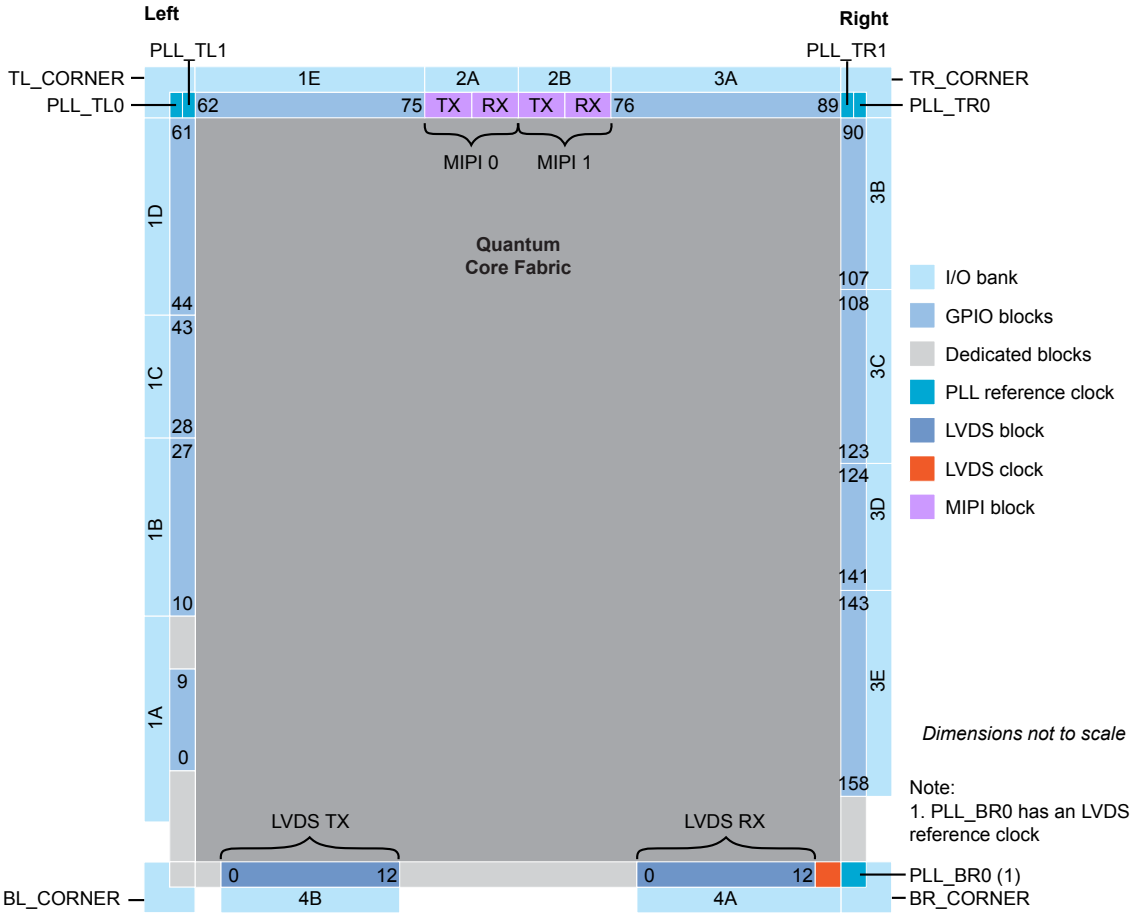


Figure 32: Floorplan Diagram for FPGAs in BGA256 Packages

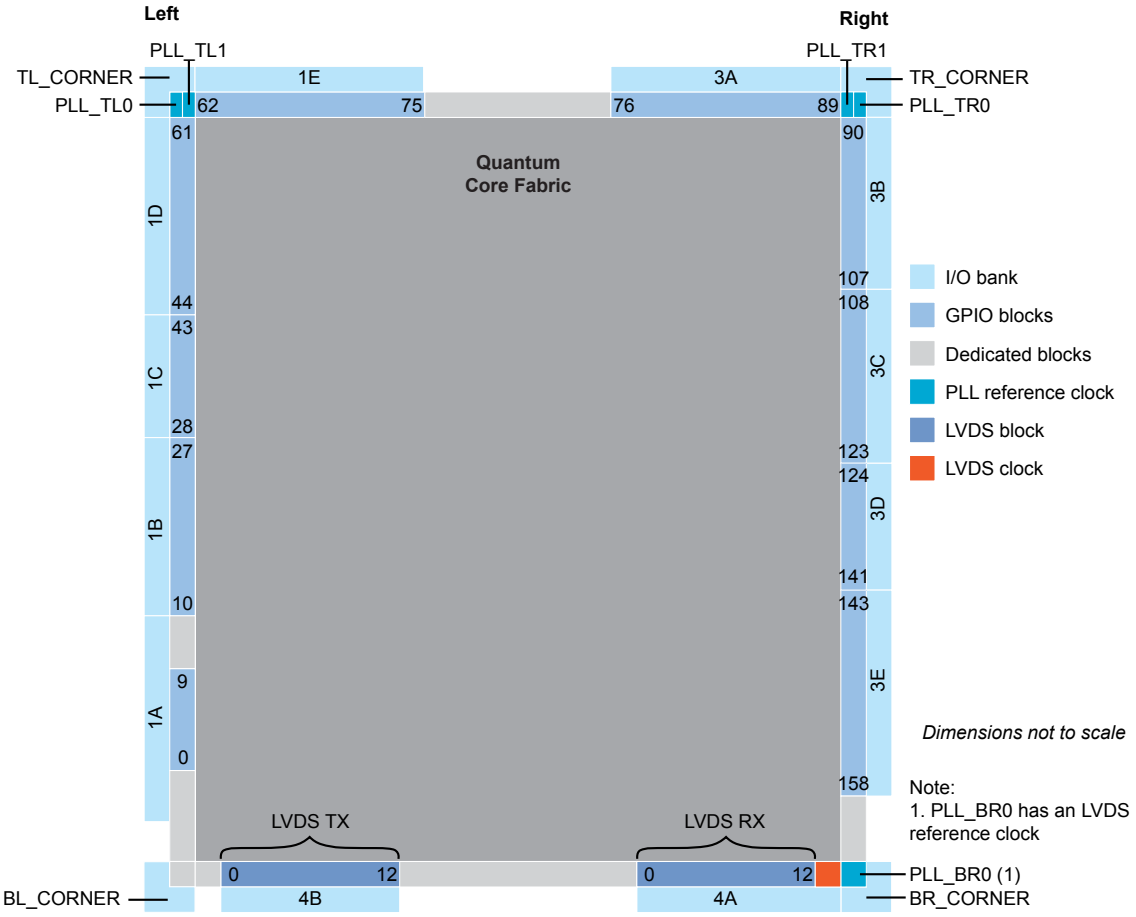
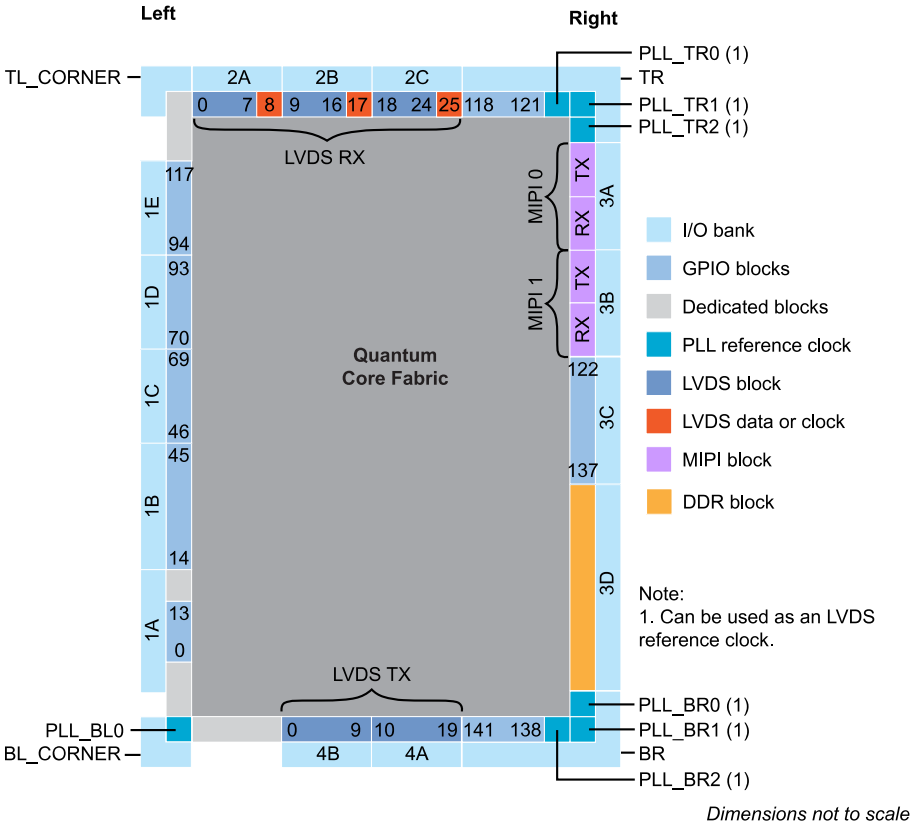


Figure 33: Floorplan Diagram for FPGAs in BGA324 and BGA400 Packages (with DDR and MIPI)



Ordering Codes

Refer to the Trion Selector Guide for the full listing of T20 ordering codes.

Revision History

Table 94: Revision History

Date	Version	Description
February 2020	3.1	Added f_{MAX} for DSP blocks and RAM blocks. Added JTAG timing parameters for T20 FPGAs in BGA324 packages. In MIPI RX and TX interface description, updated maximum data pixels for RAW10 data type. Added MIPI reset timing information. Added Trion power-up sequence. MIPI power-up moved to this topic. VCC12A_MIPI_TX, VCC12A_MIPI_RX maximum recommended operating condition changed to 1.25 V. Added a note to the Supported Configuration Modes topic to clarify that T20 BGA324 FPGAs do not support multi-image configuration in SPI active x1 mode. Added the maximum PLL output clock speed for PLL BR0 CLKOUT0 (DDR PHY input clock). Corrected the read and write signal directions in the DDR block diagram. Corrected write strobe bus width. Added number of global clocks and controls that can come from GPIO pins to package resources table.
December 2019	3.0	Updated DDR block description. Updated PLL Interface Designer settings. Removed MIPI data type bit settings. Refer to AN 015: Designing with the Trion MIPI Interface for the bit settings. Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported. Added note to LVDS electrical specifications about RX differential I/O standard support.
October 2019	2.1	Added explanation that 2 unassigned pairs of LVDS pins should be located between and GPIO and LVDS pins in the same bank. Updated the reference clock pin assignments for TL_PLL0 and TL_PLL1. Added waveforms for configuration timing. Clarified I/O bank information.
August 2019	2.0	Updated MIPI interface description. Under Ordering Codes, added link to Trion FPGA Selector Guide.
May 2019	1.0	Updated MIPI description, DC characteristics, and pin information. Updated DDR description. Updated timing specifications. Added information on the signal interface.
January 2019	0.5	Added information on DDIO support.
December 2018	0.4	Updated package options.
November 2018	0.3	Added GNDA_*xx* (PLL analog ground) to pinout. Change VSS*xx*A_MIPI pinout to GND*xx*A_MIPI. Updated PLL block diagram and clarified feedback paths. Added floorplan information. Updated pinout table.
October 2018	0.2	Updated I/O logic and buffer topic for DDR mode. Updated LVDS serialization factors. Indicated which I/O banks support DDR mode.

Date	Version	Description
October 2018	0.1	Initial release.