THIS SPEC IS OBSOLETE

Spec No: 38-07518

Spec Title: CY23FS08, FAILSAFE 2.5 V/3.3 V ZERO DELAY
                BUFFER

Replaced by: None

Failsafe 2.5 V/3.3 V Zero Delay Buffer

Features

■ Internal DCXO for continuous glitch-free operation

■ Zero input-output propagation delay

■ 100 ps typical output cycle-to-cycle jitter

■ 110 ps typical output-output skew

■ 1 MHz to 200 MHz reference input

■ Supports industry standard input crystals

■ 200 MHz (commercial), 166 MHz (industrial) outputs

■ 5 V tolerant inputs

■ Phase-locked loop (PLL) bypass mode

■ Dual reference inputs

■ 28-pin SSOP

■ Split 2.5 V or 3.3 V output power supplies

■ 3.3 V core power supply

■ Industrial temperature available

Functional Description

The CY23FS08 is a FailSafe™ Zero Delay Buffer with two reference clock inputs and eight phase-aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.
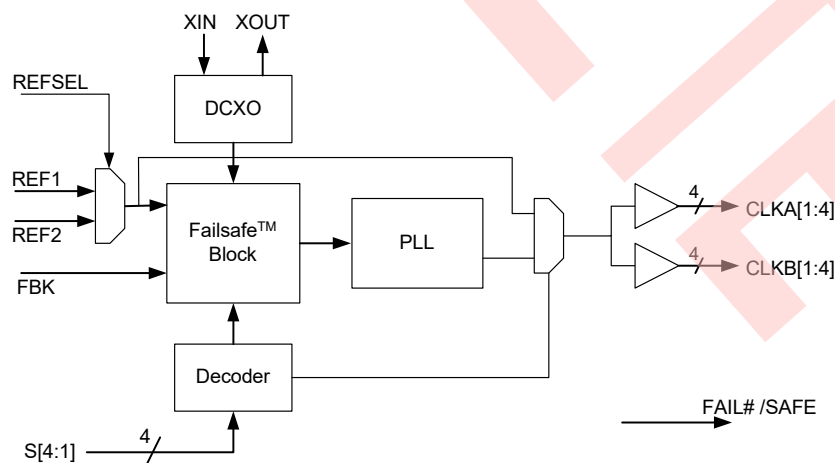
Continuous, glitch-free operation is achieved by using a DCXO, which serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

The unique feature of the CY23FS08 is that the DCXO is in fact the primary clocking source, which is synchronized (phase-aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal connected to the DCXO, must be chosen to be an integer factor of the frequency of the reference clock. This factor is set by four select lines: S[4:1]. see Configuration Table on page 4. The CY23FS08 has three split power supplies; one for core, another for Bank A outputs, and the third for Bank B outputs. Each output power supply, except VDDC can be connected to either 2.5 V or 3.3 V. VDDC is the power supply pin for internal circuits and must be connected to 3.3 V.

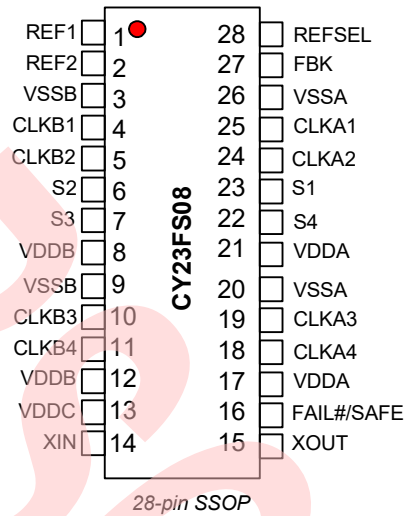For a complete list of related documentation, click here.

Logic Block Diagram

Contents

Pinouts

Figure 1. 28-pin SSOP pinout

28-pin SSOP

Pin Definitions

Pin Number	Pin Name	Description
1, 2	REF1, REF2	**Reference clock inputs.**[1] 5 V tolerant.
4, 5, 10, 11	CLKB[1:4]	**Bank B clock outputs.**[2, 3]
25, 24, 19, 18	CLKA[1:4]	**Bank A clock outputs.**[2, 3]
27	FBK	**Feedback input to the PLL.**[2]
23, 6, 7, 22	S[1:4]	**Frequency select pins/PLL and DCXO bypass.**[4]
14	XIN	**Reference crystal input.**
15	XOUT	**Reference crystal output.**
16	FAIL#/SAFE	**Valid reference indicator.** A high level indicates a valid reference input.
13	VDDC	**3.3 V power supply for the internal circuitry.**
8, 12	VDDB	**2.5 V or 3.3 V power supply for Bank B outputs.**
3, 9	VSSB	**Ground.**
17, 21	VDDA	**2.5 V or 3.3 V power supply for Bank A outputs.**
20, 26	VSSA	**Ground.**
28	REFSEL	**Reference select.** Selects the active reference clock from either REF1 or REF2. When REFSEL = 1, REF1 is selected. When REFSEL = 0, REF2 is selected.

Notes
1. Weak pull downs on these inputs.
2. For normal operation, connect either one of the eight clock outputs to the FBK input.
3. Weak pull downs on all CLK outputs.
4. Weak pull ups on these inputs.

Configuration Table

S[4:1]	XTAL (MHz)		REF (MHz)		OUT (MHz)		REF:OUT Ratio	REF:XTAL Ratio	Out:XTAL Ratio
	Min	Max	Min	Max	Min	Max			
0000					PLL and DCXO Bypass mode				
1000	8.33	30	16.67	60.00	8.33	30.00	÷2	2	1
1110	9.50	30	57.00	180.00	28.50	90.00	÷2	6	3
0101	8.50	30	6.80	24.00	1.70	6.00	÷4	4/5	1/5
1011	8.33	30	25.00	90.00	6.25	22.50	÷4	3	3/4
0011	8.33	30	2.78	10.00	2.78	10.00	×1	1/3	1/3
1001	8.33	30	8.33	30.00	8.33	30.00	×1	1	1
1111	8.00	25	32.00	100.00	32.00	100.00	×1	4	4
1100	8.00	25	64.00	200.00	64.00	200.00	×1	8	8
0001	8.33	30	1.04	3.75	2.08	7.50	×2	1/8	1/4
0110	8.33	30	4.17	15.00	8.33	30.00	×2	1/2	1
1101	8.33	30	16.67	60.00	33.33	120.00	×2	2	4
0100	8.33	30	4.17	15.00	16.67	60.00	×4	1/2	2
1010	8.33	30	12.50	45.00	50.00	180.00	×4	3/2	6
0010	8.33	30	1.39	5.00	11.11	40.00	×8	1/6	4/3
0111	8.33	30	6.25	22.50	50.00	180.00	×8	3/4	6

FailSafe Function

The CY23FS08 is targeted at clock distribution applications that requires or may require continued operation if the main reference clock fails. Existing approaches to this requirement have used multiple reference clocks with either internal or external methods to switch between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another, often requiring complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the PLL, greatly simplifying system design.

The CY23FS08 PLL is driven by the crystal oscillator, which is phase-aligned to an external reference clock so that the output of the device is effectively phase-aligned to reference via the external feedback loop. This is accomplished by using a digitally controlled capacitor array to pull the crystal frequency over an approximate range of ±300 ppm from its nominal frequency.

In this mode, if the reference frequency fails (that is, stops or disappears), the DCXO maintains its last setting and a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS08 provides four select bits, S1 through S4 to control the reference to crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag is set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag is cleared, indicating to the system that the selected reference is valid.

Figure 2. Fail#/Safe Timing for Input Reference Failing Catastrophically
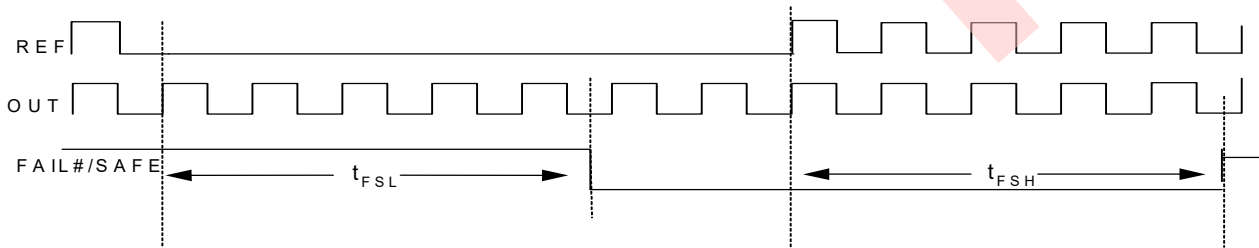
Figure 3. Fail#/Safe Timing Formula

$$t_{FSL(max)} = 2 \left(t_{REF} \times n \right) + 25\,ns$$
$$n = \frac{F_{REF}}{F_{XTAL}} = 4 \quad (\text{in above example})$$

$$t_{FSH(min)} = 12 \left(t_{REF} \times n \right) + 25\,ns$$

Table 1. Failsafe Timing Table

Parameter	Description	Conditions	Min	Max	Unit
t_{FSL}	Fail#/Safe Assert Delay	Measured at 80% to 20%, Load = 15 pF	–	See Figure 3	ns
t_{FSH}	Fail#/Safe Deassert Delay	Measured at 80% to 20%, Load = 15 pF	See Figure 3	–	ns

Figure 4. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range
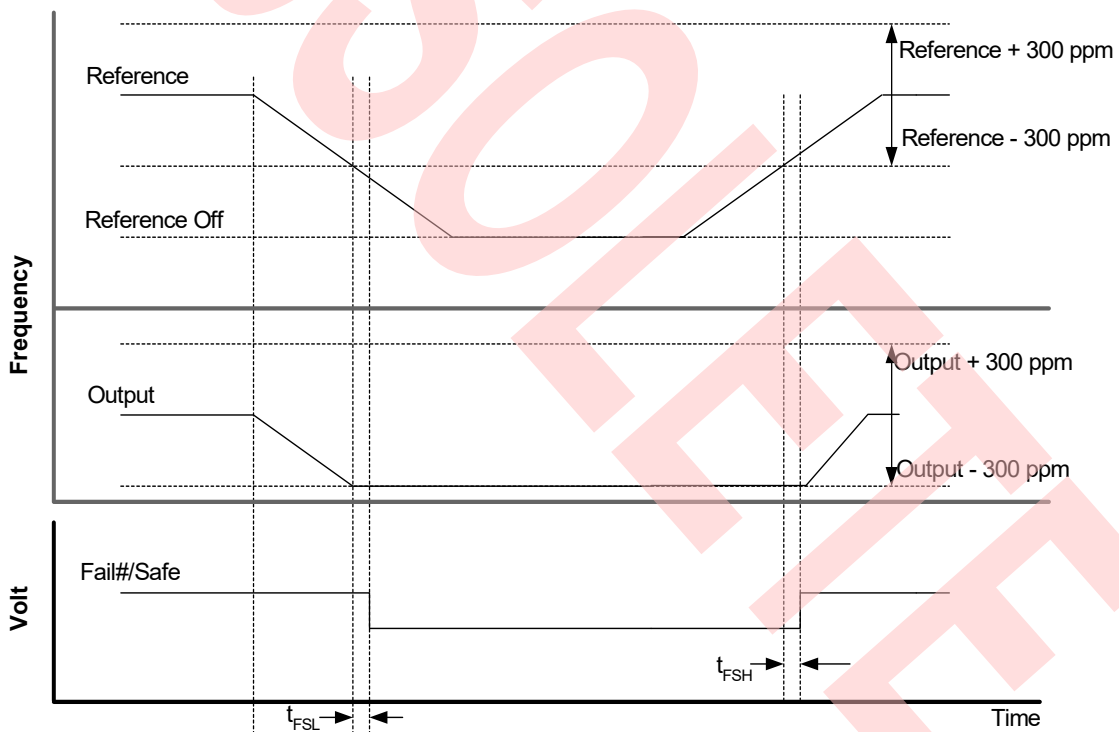
**Figure 5. FailSafe Reference Switching Behavior**

Failsafe typical frequency settling time
Initial valid Ref1 = 20 MHz +100 ppm, then switching to REF2 = 20 MHz
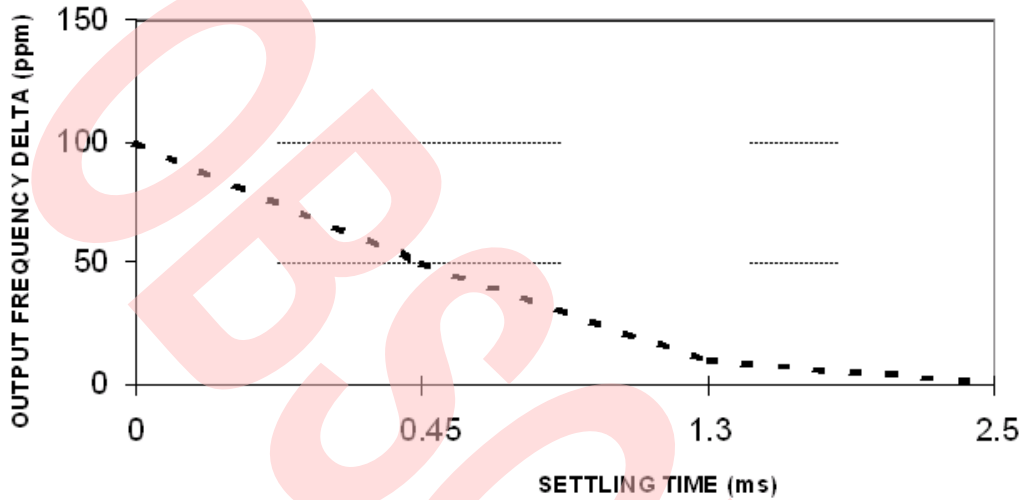
Because of the DCXO architecture, the CY23FS08 has a much lower bandwidth than a typical PLL-based clock generator. This is shown in Figure 6. This low bandwidth makes the CY23FS08 also useful as a jitter attenuator. The loop bandwidth curve is also known as the jitter transfer curve.

Figure 6. FailSafe Effective Loop Bandwidth (min)
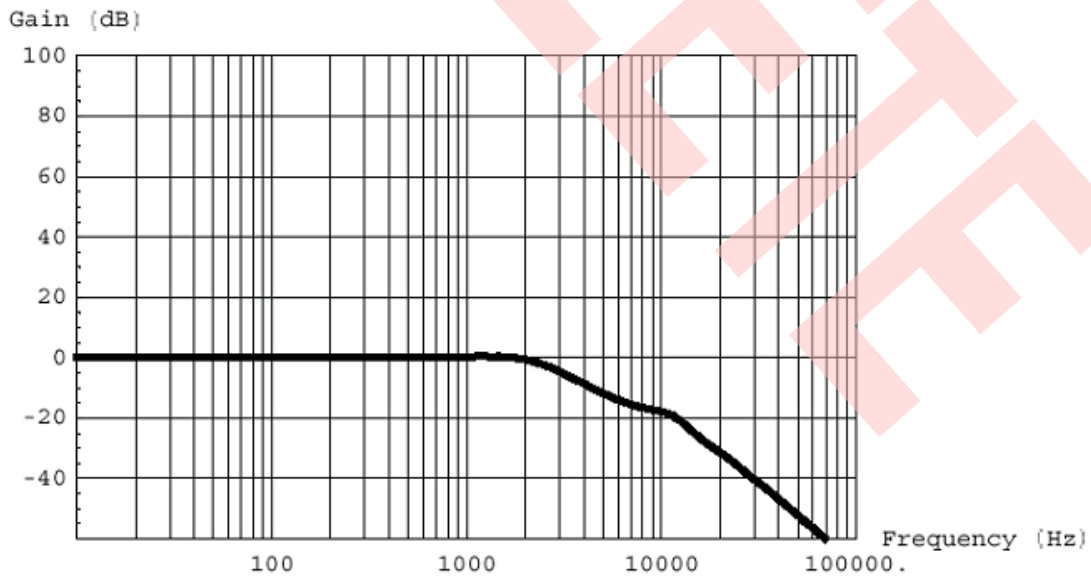
XTAL Selection Criteria and Application Example

Selecting the appropriate XTAL ensures the FailSafe device is able to span an appropriate frequency of operation. Also, the XTAL parameters determine the holdover frequency stability. Critical parameters are given here. Cypress recommends that you choose:

■ Low C0/C1 ratio (240 or less) so that the XTAL has enough range of pullability.

■ Low temperature frequency variation

■ Low manufacturing frequency tolerance

Example:

$C_{LOADMIN}$ = (12 pF IC input cap + 0 pF pulling cap + 6 pF trace cap on board) / 2 = 9 pF

$C_{LOADMAX}$ = (12 pF IC input cap + 48 pF pulling cap + 6 pF trace cap on board) / 2 = 33 pF

Pull Range = $(fC_{LOADMIN} - fC_{LOADMAX}) / fC_{LOADMIN} = (C1 / 2) \times [(1 / (C0 + C_{LOADMIN})) - (1 / (C0 + C_{LOADMAX}))]$

Pull Range in ppm = $(C1 / 2) \times [(1 / (C0 + C_{LOADMIN})) - (1 / (C0 + C_{LOADMAX}))] \times 10^6$

■ Low aging

C0 is the XTAL shunt capacitance (3 pF to 7 pF typ).

C1 is the XTAL motional capacitance (10 fF to 30 fF typ).

The capacitive load as "seen" by the XTAL is across its terminals. It is named $C_{LOADMIN}$ (for minimum value), and $C_{LOADMAX}$ (for maximum value).These are used for calculating the pull range.

Note that the C_{LOAD} range "center" is approximately 20 pF, but we may not want a XTAL calibrated to that load. This is because the pullability is not linear, as represented in the equation below. Plotting the pullability of the XTAL shows this expected behavior as shown in Figure 7. In this example, specifying a XTAL calibrated to 16 pF load provides a balanced ppm pullability range around the nominal frequency.

Figure 7. Frequency vs. C_{LOAD} Behavior for Example XTAL
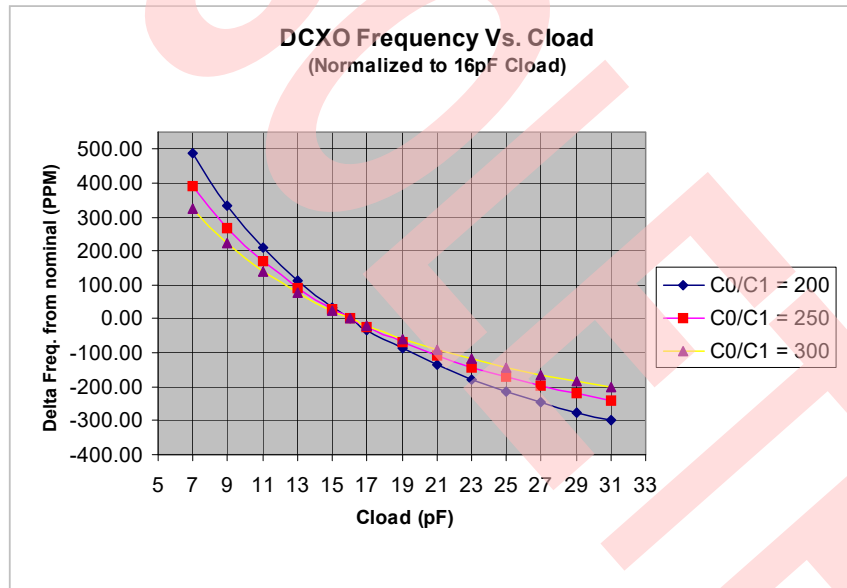
Table 2. Pullability Range from XTAL with Different C_0/C_1 Ratio

C_L	Calculated Pull Range in ppm, (Normalized)		
(pF)	$C_0/C_1 = 200$	$C_0/C_1 = 250$	$C_0/C_1 = 300$
7	489.13	391.30	326.09
9	332.88	266.30	221.92
11	211.35	169.08	140.90
13	114.13	91.30	76.09
15	34.58	27.67	23.06
16	0.00	0.00	0.00
17	–31.70	–25.36	–21.14
19	–87.79	–70.23	–58.53
21	–135.87	–108.70	–90.58
23	–177.54	–142.03	–118.36
25	–213.99	–171.20	–142.66
27	–246.16	–196.93	–164.11
29	–274.76	–219.81	–183.17
31	–300.34	–240.27	–200.23

Calculated value of the pullability range for the XTAL with C_0/C_1 ratio of 200, 250, and 300 are shown in Table 2. For this calculation $C_{LOADMIN}$ = 7 pF and $C_{LOADMAX}$ = 31 pF is used. Using a XTAL that has a nominal frequency specified at load capacitance of 16 pF, almost symmetrical pullability range is obtained.

Next, it is important to calculate the pullability range including error tolerances. This is the **capture range** of the input reference frequency that the FailSafe device and XTAL combination can reliably span.

Calculating the **capture range** involves subtracting error tolerances as follows:

Parameter .... f error (ppm)

Manufacturing frequency tolerance 15

Temperature stability 30

Aging 3

Board/trace variation 5

Total **53**

Example: Capture Range for XTAL with C0/C1 Ratio of 200

Negative Capture Range = –300 ppm + 53 ppm = –247 ppm

Positive Capture Range = 489 ppm – 53 ppm = +436 ppm

It is important to note that the XTAL with lower C_0/C_1 ratio has wider **pullability/capture range** as compared to the higher C_0/C_1 ratio. This helps to select the appropriate XTAL for use in the FailSafe application.

Important Notes

Following are some important notes that should be considered when designing with the Failsafe device:

1...
The trace capacitance of the XTAL inputs, XIN and XOUT must be kept as small as possible.

2...
Specify the DCXO for C_0/C_1 ratio to be less than 250 and the XTAL Load Capacitance to be approximately 16 pF. A typical DCXO specification from Ecliptek is attached here (please see page 6) for reference.

3. XTAL with low temperature frequency variation, low manufacturing frequency tolerance and low aging must be chosen.

4. Pull range must be checked for its upper and lower frequency symmetry from the nominal value as described in this application note.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	150	°C
T_J	Temperature, Junction	Functional	–	125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL–94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		3		

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Recommended Pullable Crystal Specifications

Parameter [5]	Description	Condition	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	8.00	–	30.00	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F_{3SEPLI}	Third overtone separation from $3 \times F_{NOM}$	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from $3 \times F_{NOM}$	Low side	–	–	–150	ppm
C0	Crystal shunt capacitance		–	–	7	pF
C0/C1	Ratio of shunt to motional capacitance		180	–	250	
C1	Crystal motional capacitance		14.4	18	21.6	fF

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DDC}	3.3 V Supply Voltage	3.135	3.465	V
V_{DDA}, V_{DDB}	2.5 V Supply Voltage Range	2.375	2.625	V
	3.3 V Supply Voltage Range	3.135	3.465	V
T_A	Ambient Operating Temperature, Commercial	0	70	°C
	Ambient Operating Temperature, Industrial	–40	85	°C
C_L	Output Load Capacitance (Fout $\leq$ 100 MHz)	–	30	pF
	Output Load Capacitance (Fout > 100 MHz)	–	15	pF
C_{IN}	Input Capacitance (except XIN)	–	7	pF
C_{XIN}	Crystal Input Capacitance (all internal caps off)	10	13	pF
t_{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	CMOS Levels, 30% of V_{DD}	–	–	$0.3 \times V_{DD}$	V
V_{IH}	Input High Voltage	CMOS Levels, 70% of V_{DD}	$0.7 \times V_{DD}$	–	–	V
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$ (100k pull up only)	–	–	50	µA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$ (100k pull down only)	–	–	50	µA
I_{OL}	Output Low Current	V_{OL} = 0.5 V, V_{DD} = 2.5 V	–	18	–	mA
		V_{OL} = 0.5 V, V_{DD} = 3.3 V	–	20	–	mA
I_{OH}	Output High Current	$V_{OH} = V_{DD}$ – 0.5 V, V_{DD} = 2.5 V	–	18	–	mA
		$V_{OH} = V_{DD}$ – 0.5 V, V_{DD} = 3.3 V	–	20	–	mA
I_{DDQ}	Quiescent Current	All Inputs grounded, PLL and DCXO in bypass mode, Reference Input = 0	–	–	250	µA

Thermal Resistance

Parameter [6]	Description	Test Conditions	28-pin SSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
θ_{JC}	Thermal resistance (junction to case)		30	°C/W

Notes
5. Ecliptek crystals ECX-5788-13.500M, ECX-5807-19.440M, ECX-5872-19.53125M, ECX-6362-18.432M, ECX-5808-27.000M, ECX-5884-17.664M, ECX-5883-16.384M, ECX-5882-19.200M, ECX-5880-24.576M meet these specifications.
6. These parameters are guaranteed by design and are not tested.

Switching Characteristics

Parameter [7]	Description	Test Conditions	Min	Typ	Max	Unit
f_{REF}	Reference Frequency	Commercial Grade	1.04	–	200	MHz
		Industrial Grade	1.04	–	166.7	MHz
f_{OUT}	Output Frequency	15 pF Load, Commercial Grade	1.70	–	200	MHz
		15 pF Load, Industrial Grade	1.70	–	166.7	MHz
f_{XIN}	DCXO Frequency		8.0	–	30	MHz
t_{DC}	Duty Cycle	Measured at $V_{DD}/2$	47	–	53	%
$t_{SR(I)}$	Input Slew Rate	Measured on REF1 Input, 30% to 70% of V_{DD}	0.5	–	4.0	V/ns
$t_{SR(O)}$	Output Slew Rate	Measured from 20% to 80% of V_{DD} = 3.3 V, 15 pF Load	0.8	–	4.0	V/ns
		Measured from 20% to 80% of V_{DD} =2.5V, 15 pF Load	0.4	–	3.0	V/ns
$t_{SK(O)}$	Output to Output Skew	All outputs equally loaded, measured at $V_{DD}/2$	–	110	200	ps
$t_{SK(IB)}$	Intrabank Skew	All outputs equally loaded, measured at $V_{DD}/2$	–	–	75	ps
$t_{SK(PP)}$	Part to Part Skew	Measured at $V_{DD}/2$	–	–	500	ps
$t_{(\phi)}$ [8]	Static Phase Offset	Measured at $V_{DD}/2$	–	–	250	ps
$t_{D(\phi)}$ [8]	Dynamic Phase Offset	Measured at $V_{DD}/2$	–	–	500	ps
$t_{J(CC)}$	Cycle-to-Cycle Jitter	Load = 15 pF, $f_{OUT} \geq 6.25$ MHz	–	100	200	ps
			–	18	35	ps_{RMS}
t_{LOCK}	Lock Time	At room temperature with 18.432 MHz Crystal	–	70	–	ms

Notes
7. Parameters guaranteed by design and characterization, not 100% tested in production.
8. The $t_{(\phi)}$ reference feedback input delay is guaranteed for a maximum 4:1 input edge ratio between the two signals as long as $t_{SR(I)}$ is maintained.

Switching Waveforms

Figure 8. Duty Cycle

Duty Cycle - t_{DC} = t_1 / t_2

V_{DD}/2 V_{DD}/2 V_{DD}/2 V_{DD}

0V

t_1

t_2

Figure 9. Input Slew Rate

70%   70% V_{DD}

30%   30%   0V

$t_{SR(I)}$ $t_{SR(I)}$
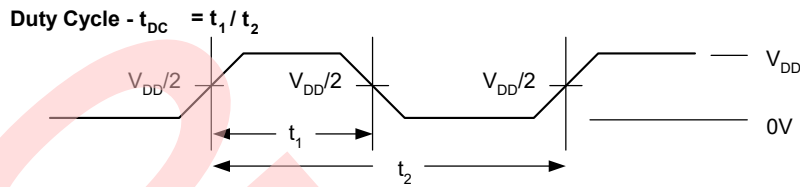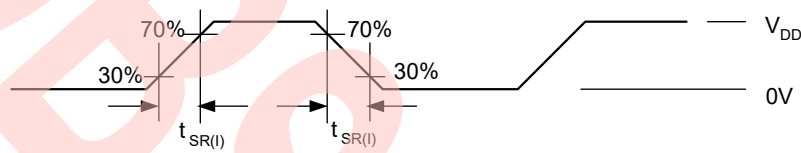
Figure 10. Output Slew Rate

80%   80% V_{DD}

20%   20%   0V

$t_{SR(O)}$ $t_{SR(O)}$
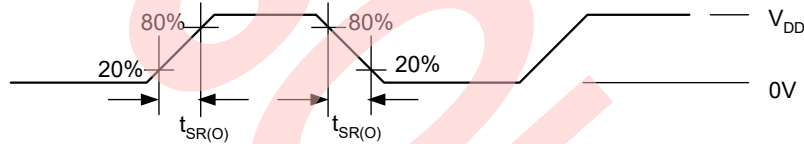
Figure 11. Output to Output Skew and Intrabank Skew

V_{DD}/2

V_{DD}/2

t_{SK}
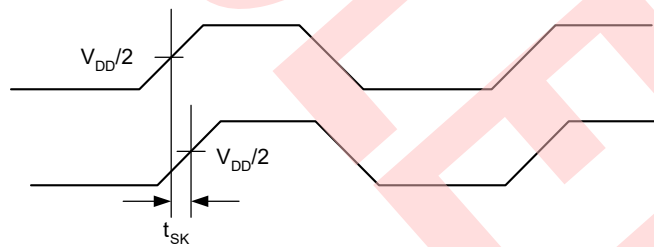
Figure 12. Part to Part Skew

FBK,
Part 1 V_{DD}/2

FBK,
Part 2 V_{DD}/2

$t_{SK(PP)}$
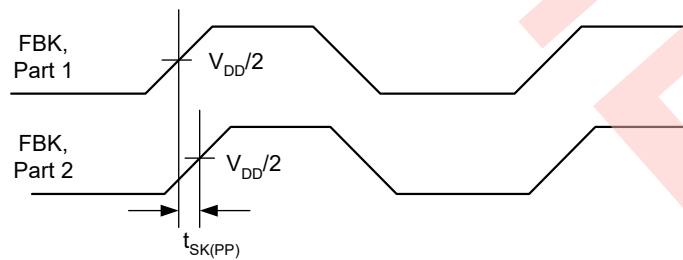
Switching Waveforms (continued)

Figure 13. Phase Offset
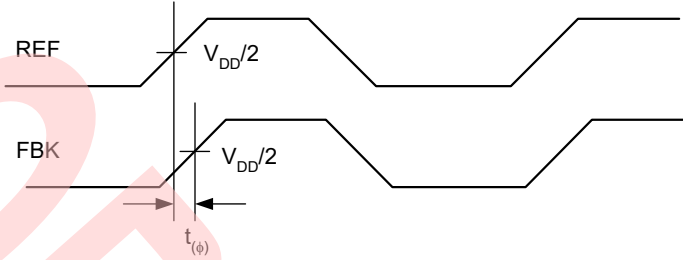
Ordering Information

Part Number	Package Type	Product Flow
Pb-free		
CY23FS08OXI	28-pin SSOP	Industrial, –40 °C to 85 °C
CY23FS08OXIT	28-pin SSOP – Tape and Reel	Industrial, –40 °C to 85 °C
CY23FS08OXC	28-pin SSOP	Commercial, 0 °C to 70 °C
CY23FS08OXCT	28-pin SSOP – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions

CY 23FS08 O X X - X

X = blank or T
blank = Tube; T = Tape and Reel

Temperature Range: X = I or C
I = Industrial; C = Commercial

Pb-free

Package Type:
O = 28-pin SSOP

Device Number

Company ID: CY = Cypress
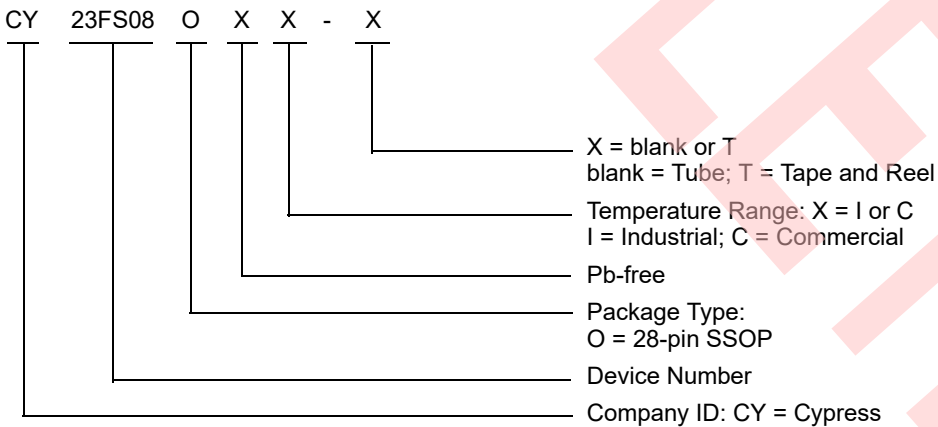
Package Diagram

Figure 14. 28-pin SSOP (210 Mils) Package Outline, 51-85079

28 Lead (5.3mm) SSOP

DIMENSIONS IN MILLIMETERS $\frac{MIN.}{MAX.}$

51-85079 *F
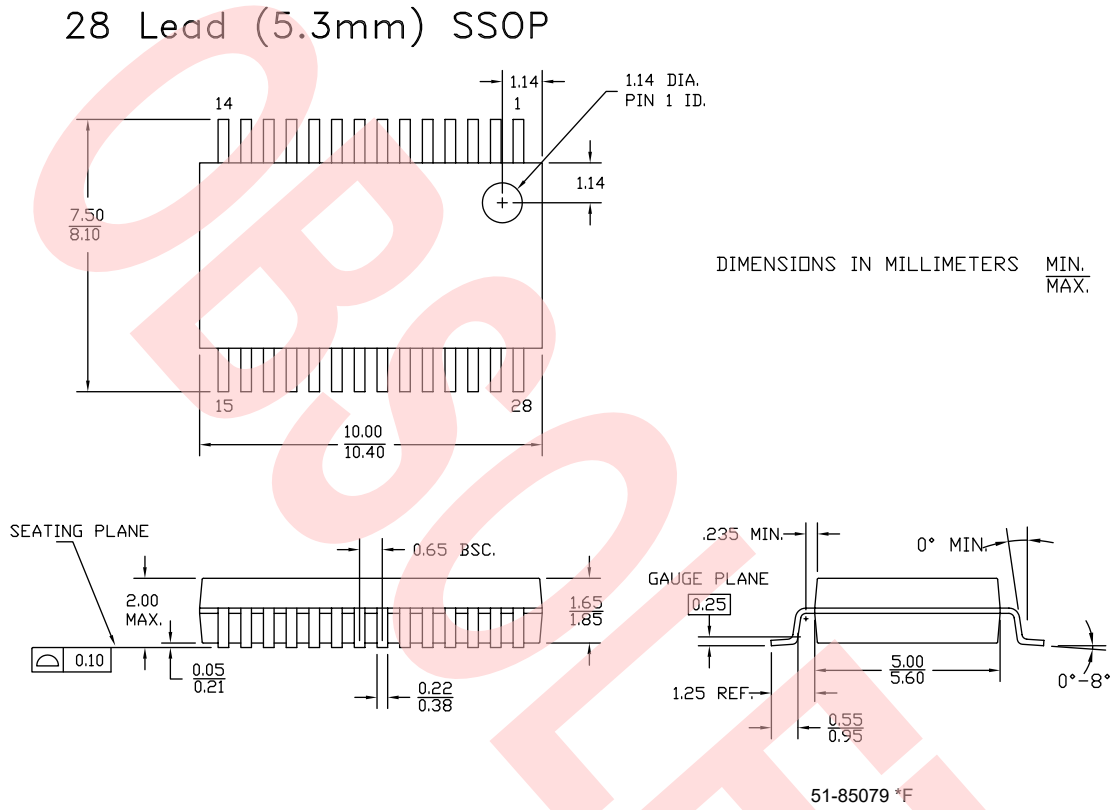
Acronyms

Acronym	Description
DCXO	Digitally Controlled Crystal Oscillator
ESD	Electrostatic Discharge
PLL	Phase Locked Loop
RMS	Root Mean Square
SSOP	Shrunk Small Outline Package
XTAL	Crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
ppm	parts per million
pF	picofarad
ps	picosecond
W	watt
V	volt

Document History Page

Document Title: CY23FS08, Failsafe 2.5 V/3.3 V Zero Delay Buffer **Document Number: 38-07518**			

Revision	ECN	Submission Date	Description of Change
**	123699	04/23/2003	New data sheet.
*A	224067	05/10/2004	Updated XTAL Selection Criteria and Application Example: Updated Table 2. Updated Recommended Pullable Crystal Specifications: Removed CR load, ESR, T_O parameters and their details. Added F_{NOM}, C_{LNOM}, R_1, R_3/R_1, DL, F_{3SEPLI}, F_{3SEPLO}, C_0, C_1 parameters and their details. Updated all details corresponding to C_0/C_1 parameter.
*B	276749	10/12/2004	Updated Switching Characteristics: Removed t_{LOCK} parameter and its corresponding details.
*C	417645	01/02/2006	Updated Switching Characteristics: Added "Typ" column and included values in that column for tSK(O), tD(φ), tJ(CC) parameters. Added t_{LOCK} parameter and its corresponding details. Updated Ordering Information: Updated part numbers. Updated to new template.
*D	2865396	01/25/2010	Updated FailSafe Function: Removed figure "Sample Timing of Muxing Between Two Reference Clocks 180 °C Out of Phase and Resulting Output Phase Offset Typical Settling Time (105 MHz)". Added Figure 9. Added Figure 11. Updated XTAL Selection Criteria and Application Example: Replaced "Cl" with "C_{LOAD}". Updated Absolute Maximum Conditions: Removed T_A parameter and its corresponding details. Updated Recommended Pullable Crystal Specifications: Updated Note 5 (Replaced ECX–5806–18.432M with ECX–6362–18.432M). Removed Note "Includes typical board trace capacitance of 6–7pF each XIN, XOUT.". Updated Ordering Information: Replace "Lead-free" with "Pb-free". Updated part numbers. Updated Package Diagram: Replaced "O28" with "SP28" in figure caption of spec 51-85079. spec 51-85079 – Changed revision from *C to *D. Updated to new template.
*E	2925613	04/30/2010	Post to external web.
*F	3130032	01/06/2011	Updated Switching Characteristics: Removed typical value (150 ps) of $t_{D(\phi)}$ parameter. Changed maximum value of $t_{D(\phi)}$ parameter from 200 ps to 500 ps. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Completing Sunset Review.
*G	3695670	08/03/2012	Updated XTAL Selection Criteria and Application Example: Updated Figure 7. Updated Table 2. Updated Package Diagram: spec 51-85079 – Changed revision from *D to *E.
*H	4276658	02/10/2014	Updated to new template. Completing Sunset Review.

Document History Page (continued)

Document Title: CY23FS08, Failsafe 2.5 V/3.3 V Zero Delay Buffer			
Document Number: 38-07518			
Revision	**ECN**	**Submission Date**	**Description of Change**
*I	4580588	12/05/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Completing Sunset Review.
*J	5275836	05/27/2016	Updated Absolute Maximum Conditions: Removed $\varnothing_{JC}$, $\varnothing_{JA}$ parameters and their details. Changed value of MSL parameter from "1" to "3". Added Thermal Resistance. Updated Package Diagram: spec 51-85079 – Changed revision from *E to *F. Updated to new template.
*K	5992905	12/13/2017	Updated Cypress Logo and Copyright.
*L	6070919	02/14/2018	No technical updates. Completing Sunset Review.
*M	6817301	02/26/2020	Obsolete document. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support