FEATURES

- TI AM1810 ARM9 Application Processor
  - **375 MHz ARM926EJ-S MPU**
    - 16 KB L1 Program Cache
    - 16 KB L1 Data Cache
    - 8 KB Internal RAM
    - 64 KB boot ROM
    - JTAG Emulation/Debug
- Up To 256 MB mDDR2 CPU RAM
- Up To 512 MB Parallel NAND FLASH
- 8 MB SPI based NOR FLASH
- Integrated Power Management
- Standard SO-DIMM-200 Interface
  - 10/100 EMAC MII / RMII / MDIO
  - 2 UARTS
  - 2 McBSPs, 2 SPI, 2HPI
  - 2 USB Ports
  - Video, LCD Output
  - Camera/Video Input
  - MMC/SD
  - SATA
  - ePWM, eCAP
  - EMIFA
  - Single 3.3V Power Supply
- PROFIBUS Interface
  - Certified by PI International
  - Real-Time Linux Drivers
  - Up to 6Mbaud operation

(actual size)

APPLICATIONS

- Process Automation
- Factory Automation
- Industrial Automation
- Industrial Instrumentation
- Embedded Control Processing
- Test and Measurement

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and Interface Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Real-Time Linux Kernel 2.6
  - QNX 6.4
  - Windows Embedded CE Ready
  - ThreadX Real Time OS

DESCRIPTION

The MitySOM-1810 is a highly configurable, very small form-factor processor card that features a Texas Instruments AM1810 375MHz ARM Applications Processor for PROFIBUS, FLASH (NAND, and NOR) and mDDR2 RAM memory subsystems. The MitySOM-1810 provides a complete and flexible CPU infrastructure necessary for the most demanding embedded applications development.

The AM1810 includes an ARM926EJ-S micro-processor unit (MPU) capable of running the rich software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux, QNX and Windows XP embedded. Linux drivers are available for all interfaces, including the PROFIBUS interface.

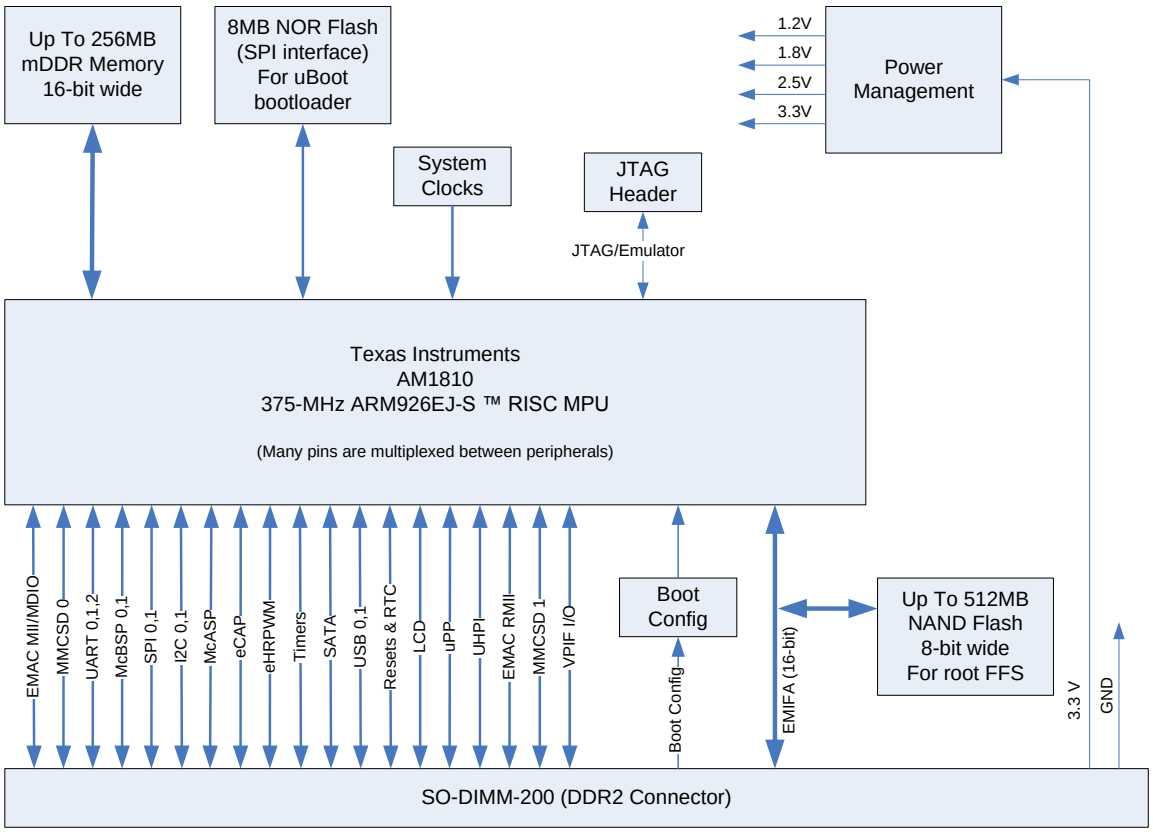

Figure 1 MitySOM-1810 Block Diagram

Figure 1 provides a top level block diagram of the MitySOM-1810 processor card. As shown in the figure, the primary interface to the MitySOM-1810 is through a standard SO-DIMM-200 card edge interface. The interface provides power, synchronous serial connectivity, and a rich set of interfaces available for application defined interfacing. Details of the SO-DIMM-200 connector interface are included in the SO-DIMM-200 Interface Description, below.

PROFIBUS Interface

Texas Instruments Inc. (TI) has integrated PROFIBUS functionality into its AM1810 Sitara ARM microprocessor (MPU). The solution utilizes one of the onboard UARTS and connects directly to the RS-485 transceiver and therefore eliminates the need of an external PROFIBUS ASIC or FPGA. Customers using the MitySOM-1810 in their industrial application can save cost and reduce design complexity as well as PCB space. Furthermore, the industrial application benefits from the low-power architecture of the Sitara ARM MPU and the MitySOM-1810 platform from TI and Critical Link.

The AM1810 Sitara ARM MPU PROFIBUS Slave solution has been certified by PROFIBUS International (PI).

The PROFIBUS real-time frame handler (Fieldbus Data Link or FDL) is encapsulated in the Programmable Real-Time Unit Subsystem (PRUSS), which is part of the AM1810

Sitara ARM MPU on-chip peripherals. The PRUSS uses one Universal Asynchronous Receiver/Transmitter (UART) and a timer to generate PROFIBUS-compliant frames. The industrial application and the PROFIBUS DP-Protocol (Layer 7) are operated on the ARM. The solution can be completed with an RS-485 transceiver suitable for harsh environments, such as TI's ISO1176T or ISO1176 placed on the base board to the MitySOM-1810.

The PROFIBUS subsystem uses the PRUs that implement real-time frame handling; PROFIBUS message transmission, frame validation and communication with the ARM processor. The PROFIBUS subsystem interfaces with one of the UARTs in the AM1810 Sitara ARM MPU, which is designated for PROFIBUS communication at up to 6Mbaud data rate. The PRU uses interrupts to interact with the ARM where the PROFIBUS stack (Layer 7, DP Protocol) and the industrial application is run. All process data handling like cyclic, acyclic and service access point (SAP) between the PROFIBUS stack on ARM and the PRU is through the internal memory.

Additional details about the AM1810 Sitara ARM MPU, available peripherals and their features are provided in the data sheet at the TI website (www.ti.com/am1810).

AM1810 mDDR2 Memory Interface
The AM1810 includes a dedicated DDR2 SDRAM memory interface. The MitySOM-1810 includes up to 256 MB of mDDR2 RAM integrated with the AM1810 processor. The bus interface is capable of burst transfer rates of 532 MB / second. Note that the OSCIN frequency to the AM1810 processor on the module is 24MHz.

AM1810 SPI NOR FLASH Interface
The MitySOM-1810 includes 8 MB of SPI NOR FLASH. This FLASH memory is intended to store a factory provided bootloader, and typically a compressed image of a linux kernel for the ARM core processor.

EMIFA / NAND FLASH Interface
The Asynchronous External Memory Interface (EMIFA) interface available on the AM1810 is available on the SO-DIMM-200 connector. The EMIFA interface includes 3 chip select spaces. The EMIF interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, and 16 bit data word sizes may be used.

Up to 512 MB of on-board NAND FLASH memory is connected to the AM1810 using the EMIFA bus. The FLASH memory is 8 bits wide and is connected to the third chip select line of the EMIFA (CE1). The FLASH memory is typically used to store the following types of data:

- ARM Linux / Windows Embedded CE / QNX embedded root file-system
- runtime ARM software
- runtime application data (non-volatile storage)

AM1810 Camera and Video Interfaces
The AM1810 includes an optional video port I/O interface commonly used to drive LCD screens as well as a camera input interface. These interfaces have been routed directly to the SO-DIMM-200 connector.

Debug Interface
The JTAG signals for the AM1810 processor have been brought out to a Hirose header that is intended for use with an available Critical Link breakout adapter. This header can be removed for production units; please contact your Critical Link representative for details.

This adapter is not included with individual modules but is included with each Critical Link Development Kit that is ordered. If an adapter, Critical Link (CL) part number 80-000286, is needed please contact your Critical Link representative.

Software and Application Development Support
Users of the MitySOM-1810 are encouraged to develop applications using the MitySOM-1810 software development kit provided by Critical Link LLC. The development kit includes an implementation of an OpenEmbedded board support package providing an Angstrom based Linux distribution and compatible gcc compiler tool-chain with debugger.

Growth Options
The MitySOM-1810 has been designed to support several upgrade options. These options include various speed grades, memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	3.5 V
Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range Commercial	0°C to 70°C
Ambient Temperature Range Industrial	-40°C to 85°C
Humidity	0 to 95% Non-condensing
MIL-STD-810F	Contact Critical Link for Details

SO-DIMM-200 Interface Description

The primary interface connector for the MitySOM-1810 is the SO-DIMM card edge interface which contains 4 classes of signals:

Power (PWR)
Dedicated signals mapped to the AM-1810 device (D)
Dedicated signals when NAND memory is populated on the module (D*)
Multi-function signals mapped to the AM1810 device (M)

Table 1 contains a summary of the MitySOM-1810 pin mapping.

Table 1 SO-DIMM Pin-Out

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
1	-	PWR	-	+3.3 V in	2	-	PWR	-	+3.3 V in
3	-	PWR	-	+3.3 V in	4	-	PWR	-	+3.3 V in
5	-	PWR	-	+3.3 V in	6	-	PWR	-	+3.3 V in
7	-	PWR	-	GND	8	-	PWR	-	GND
9	-	PWR	-	GND	10	-	PWR	-	GND
11	K14	D	I	RESET_IN#	12	-	D	I	EXT_BOOT#
13	J1	D	O	SATA_TX_P	14	A4	M	I/O	GP0_7
15	J2	D	O	SATA_TX_N	16	A3	M	I/O	GP0_10
17	L1	D	I	SATA_RX_P	18	A2	M	I/O	GP0_11
19	L2	D	I	SATA_RX_N	20	A1	M	I/O	GP0_15
21	P16	D	I	USB0_ID	22	B4	M	I/O	GP0_6
23	P18	D	I/O	USB1_D_N	24	B1	M	I/O	GP0_14
25	P19	D	I/O	USB1_D_P	26	B2	M	I/O	GP0_12
27	N19	D	O	USB0_VBUS	28	B3	M	I/O	GP0_5
29	M18	D	I/O	USB0_D_N	30	C2	M	I/O	GP0_13
31	M19	D	I/O	USB0_D_P	32	C3	M	I/O	GP0_1
33	K18	D	O	USB0_DRVVBUS	34	C4	M	I/O	GP0_4
35	-	D	-	3V RTC Battery	36	C5	M	I/O	GP0_3
37	-	PWR	-	+3.3 V in	38	-	PWR	-	+3.3 V in
39	-	PWR	-	+3.3 V in	40	-	PWR	-	+3.3 V in

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
41	-	PWR	-	GND	42	-	PWR	-	GND
43	H17	D	I/O	SPI1_MISO	44	D4	M	I/O	GP0_2
45	G17	D	I/O	SPI1_MOSI	46	E4	M	I/O	GP0_0
47	H16	D	I/O	SPI1_ENA	48	F4	M	I/O	GP0_8
49[1]	G19	D	I/O	SPI1_CLK	50	D5	M	I/O	GP0_9
51	F18	M	I/O	SPI1_SCS[1]	52	A12	M	I/O	MMCSD0_DAT[7]
53	-	D	-	Reserved	54	C11	M	I/O	MMCSD0_DAT[6]
55[2]	G16	D	I/O	I2C0_SCL	56	E12	M	I/O	MMCSD0_DAT[5]
57[2]	G18	D	I/O	I2C0_SDA	58	B11	M	I/O	MMCSD0_DAT[4]
59	F16	M	I/O	UART2_TXD / I2C1_SDA	60	E11	M	I/O	MMCSD0_DAT[3]
61	F17	M	I/O	UART2_RXD / I2C1_SCL	62	C10	M	I/O	MMCSD0_DAT[2]
63	-	PWR	-	GND	64	-	PWR	-	GND
65	F19	M	O	UART1_TXD	66	A11	M	I/O	MMCSD0_DAT[1]
67	E18	M	I	UART1_RXD	68	B10	M	I/O	MMCSD0_DAT[0]
69	E16	M	O	MDIO_CLK	70	A10	M	I/O	MMCSD0_CMD
71	D17	M	I/O	MDIO_D	72	E9	M	O	MMCSD0_CLK
73	D19	M	I	MII_RXCLK	74	D3	M	I	MII_TXCLK
75	C17	M	I	MII_RXDV	76	E3	M	O	MII_TXD[3]
77	D16	M	I	MII_RXD[0]	78	E2	M	O	MII_TXD[2]
79	E17	M	I	MII_RXD[1]	80	E1	M	O	MII_TXD[1]
81	D18	M	I	MII_RXD[2]	82	F3	M	O	MII_TXD[0]
83	C19	M	I	MII_RXD[3]	84	C1	M	O	MII_TXEN
85	-	PWR	-	GND	86	-	PWR	-	GND
87	C18	M	I	MII_CRS	88	D1	M	I	MII_COL
89	C16	M	I	MII_RXER	90	-	D	-	NC
91	A18	M	O	EMA_CS[0]	92	W15	M	I/O	UPP_CHA_START
93	B15	D*	O	EMA_OE	94	V15	M	I	VP_CLKIN1
95	C15	M	O	EMA_BA[0]	96	U18	M	I/O	UPP_D[15] / RMII_TXD[1]
97	A15	M	O	EMA_BA[1]	98	V16	M	I/O	UPP_D[14] / RMII_TXD[0]
99	C14	M	O	EMA_A[0]	100	R14	M	I/O	UPP_D[13] / RMII_TXEN
101	D15	D*	O	EMA_A[1]	102	W16	M	I/O	UPP_D[12] / RMII_RXD[1]
103	B14	D*	O	EMA_A[2]	104	V17	M	I/O	UPP_D[11] / RMII_RXD[0]
105	D14	M	O	EMA_A[3]	106	W17	M	I/O	UPP_D[10] / RMII_RXER
107	-	PWR	-	GND	108	-	PWR	-	GND
109	A14	M	O	EMA_A[4]	110	W18	M	I/O	UPP_D[9] / RMII_REF_CLK
111	C13	M	O	EMA_A[5]	112	W19	M	I/O	UPP_D[8] / RMII_CRS_DV
113	E13	M	O	EMA_A[6]	114	V18	M	I/O	UPP_D[7]
115	B13	M	O	EMA_A[7]	116	V19	M	I/O	UPP_D[6]
117	A13	M	O	EMA_A[8]	118	U16	M	I/O	UPP_CHA_ENABLE
119	D12	M	O	EMA_A[9]	120	U19	M	I/O	UPP_D[5]
121	C12	M	O	EMA_A[10]	122	T16	M	I/O	UPP_D[4]

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
123	B12	M	O	EMA_A[11]	124	R18	M	I/O	UPP_D[3]
125	D13	M	O	EMA_A[12]	126	R19	M	I/O	UPP_D[2]
127	D11	M	O	EMA_A[13]	128	T15	M	I/O	UPP_CHA_WAIT
129	-	PWR	-	GND	130	-	PWR	-	GND
131	E6	D*	I/O	EMA_D[15]	132	R15	M	I/O	UPP_D[1]
133	C7	D*	I/O	EMA_D[14]	134	P17	M	I/O	UPP_D[0]
135	B6	D*	I/O	EMA_D[13]	136	U17	M	I/O	UPP_CHA_CLK
137	A6	D*	I/O	EMA_D[12]	138	J4	M	I/O	UPP_CHB_ENABLE
139	D6	D*	I/O	EMA_D[11]	140	K3	M	O	VP_CLKOUT2
141	A7	D*	I/O	EMA_D[10]	142	H3	M	I	VP_CLKIN2
143	D9	D*	I/O	EMA_D[9]	144	G3	M	I/O	UPP_CHB_WAIT
145	E10	D*	I/O	EMA_D[8]	146	G2	M	I/O	UPP_CHB_START
147	D7	D*	I/O	EMA_D[7]	148	G1	M	I/O	UPP_CHB_CLK
149	C6	D*	I/O	EMA_D[6]	150	W14	M	I	VP_CLKIN0
151	-	PWR	-	GND	152	-	PWR	-	GND
153	E7	D*	I/O	EMA_D[5]	154	P4	M	I/O	LCD_D[15]
155	B5	D*	I/O	EMA_D[4]	156	R3	M	I/O	LCD_D[14]
157	E8	D*	I/O	EMA_D[3]	158	R2	M	I/O	LCD_D[13]
159	B8	D*	I/O	EMA_D[2]	160	R1	M	I/O	LCD_D[12]
161	A8	D*	I/O	EMA_D[1]	162	T3	M	I/O	LCD_D[11]
163	C9	D*	I/O	EMA_D[0]	164	T2	M	I/O	LCD_D[10]
165	C8	M	O	EMA_WEN_DQM[0]	166	T1	M	I/O	LCD_D[9]
167	A5	M	O	EMA_WEN_DQM[1]	168	U3	M	I/O	LCD_D[8]
169	D8	M	O	EMA_SDCKE	170	U2	M	I/O	LCD_D[7]
171[3]	B7	M	O	EMA_CLK	172	U1	M	I/O	LCD_D[6]
173	-	PWR	-	GND	174	-	PWR	-	GND
175	B9	D*	O	EMA_WE	176	G4	M	O	LCD_VSYNC
177	A9	M	O	EMA_CAS	178	H4	M	O	LCD_HSYNC
179	A16	M	O	EMA_RAS	180	V3	M	I/O	LCD_D[5]
181	B17	M	O	EMA_CS[2]	182	F1	M	O	LCD_PCLK
183	F9	M	O	EMA_CS[4]	184	V2	M	I/O	LCD_D[4]
185	B16	M	O	EMA_CS[5]	186	V1	M	I/O	LCD_D[3]
187	T17	D	O	RESET_OUT	188	W3	M	I/O	LCD_D[2]
189	J3	M	I	VP_CLKIN3	190	W2	M	I/O	LCD_D[1]
191	K4	M	O	VP_CLKOUT3	192	W1	M	I/O	LCD_D[0]
193	F2	M	O	LCD_MCLK	194	R5	M	O	LCD_AC_ENB_CS
195	-	PWR	-	GND	196	-	PWR	-	GND
197[4]	D10	M	O	EMA_A_RW	198	B18[4]	D*	I	EMA_WAIT[0]
199[4]	A17	D*	O	EMA_CS[3]	200	B19[4]	M	I	EMA_WAIT[1]

Note 1: Pin 49, SPI1_CLK, has a 100K Ohm pull-down resistor on the module
Note 2: Pins 55 and 57 have 4.70K pull-up resistors on the module
Note 3: Pin 171, EMA_CLK, has a 49.9 Ohm resistor in series with the signal on the module
Note 4: Pins 197, 198, 199 and 200 have 1.00K Ohm resistors in series with the signals on the module

The signal group description for the above pins is included in Table 2

Table 2 Signal Group Description

Signal / Group	Type	Description
3.3 V in	N/A	3.3 volt input power referenced to GND.
EXT_BOOT#	I	Bootstrap configuration pin. Pull low to configure booting from external UART1.
RESET_IN#	I	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the processor.
SPI1_*	I/O	Serial Peripheral Interface 1 pins. These pins are direct connects to the corresponding SPI1_* pins on the AM1810 processor. The SPI1_* function pins are multiplexed with other functions. These include PWM, Timers, UARTs, I2C0, and GPIO. For details please refer to the AM1810 processor specifications.
MII_*	I/O	Media Independent Interface (Ethernet) pins. These pins are direct connects to the corresponding MII_* pins on the AM1810 processor. The MII_* function pins are multiplexed with other functions. These include SPI0, PWM, Timers, UART0, MCBSP, MCASP, and GPIO. For details please refer to the AM1810 processor specifications.
MDIO_DAT MDIO_CLK	I/O	MII/RMII Management Interface pins. The MDIO_CLK and MDIO_DAT signals are direct connects to the corresponding MDIO_* signals on the AM1810 processor. The MDIO_* function pins are multiplexed with other functions. These include SPI0 and Timer functions. For details please refer to the AM1810 processor specifications.
GP0_*	I/O	General Purpose / multiplexed pins. These pins are direct connects to the corresponding GP0[*] pins on the AM1810 processor. The include support for the McASP, general purpose I/O, UART flow control, and McBSP 1. For details please refer to the AM1810 processor specifications.
SATA_TX_P SATA_TX_N	O	Serial ATA Controller Transmit pins. These pins are direct connects to the corresponding SATA_TX_* pins on the AM1810 processor. For details please refer to the AM1810 processor specifications.
SATA_RX_P SATA_RX_N	I	Serial ATA Controller Receive pins. These pins are direct connects to the corresponding SATA_RX_* pins on the AM1810 processor. For details please refer to the AM1810 processor specifications.
GND	N/A	System Digital Ground.

Signal / Group	Type	Description
EMA_*	I/O	EMIF-A pins. These pins are direct connects to the corresponding EMA_* pins on the AM1810 processor. Alternatively, these pins can be configured as GPIOs for modules that do not have NAND memory present. For details please refer to the AM1810 processor specifications. Note that pins 197, 198, 199 and 200 have 1.00K Ohm resistors in series with the signals on the module.
UPP_*	I/O	Universal Parallel Port pins. These pins are direct connects to the corresponding UPP_* pins on the AM1810 processor. The UPP_* function pins are multiplexed with other functions. These include RMII, VP_DIN, MMCSD1, and GPIO. For details please refer to the AM1810 processor specifications.
RMII_*	I/O	Reduced Media Independent Interface pins. These pins are direct connects to the corresponding RMII_* pins on the AM1810 processor. The RMII_* function pins are multiplexed with other functions. These include UPP and VP_DIN. For details please refer to the AM1810 processor specifications.
LCD_*	I/O	Liquid Crystal Display pins. These pins are direct connects to the corresponding LCD_* pins on the AM1810 processor. The LCD_* function pins are multiplexed with other functions. These include VP_DOUT, UPP, MMCSD1, and GPIO. For details please refer to the AM1810 processor specifications.
VP_*	I/O	Video Port In/Out. These pins are direct connects to the corresponding VP_* pins on the AM1810 processor. The VP_* function pins are multiplexed with other functions. These include UPP, MMCSD1, and GPIO. For details please refer to the AM1810 processor specifications.
RESET_OUT	I/O	Reset Output pin. This pin is a direct connect to the RESET_OUT pin on the AM1810 processor. This pin can also be configured as a GPIO. For details please refer to the AM1810 processor specifications.
USB0_*, USB1_*	I/O	Universal Serial Bus 0 / 1 pins. These pins are direct connects to the corresponding USB_* pins on the AM1810 processor. For details please refer to the AM1810 processor specifications.

DEBUG INTERFACE

Below is the pin-out for the Hirose 31 pin header (DF9-31P-1V(32)) that interfaces with an available adapter board, CL part number 80-000286, to debug the AM1810.

Debug Interface Connector Description (J2)

Table 3 AM1810 Hirose Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	-	GND	2	O	OMAP EMU1
3	-	GND	4	O	OMAP EMU0
5	-	GND	6	I	OMAP TCK
7	-	GND	8	O	OMAP RTCK
9	-	GND	10	O	OMAP TDO
11	-	GND	12	-	OMAP VCC / 3.3V
13	-	GND	14	I	OMAP TDI
15	-	GND	16	I	OMAP TRST
17	-	GND	18	I	OMAP TMS
19	-	GND	20	-	GND
21	-	GND	22	NC	FPGA VREF / VCCAUX
23	-	GND	24	NC	FPGA TMS
25	-	GND	26	NC	FPGA TCK
27	-	GND	28	NC	FPGA TDO
29	-	GND	30	NC	FPGA TDI
31	-	GND			

ELECTRICAL CHARACTERISTICS

Table 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V33	Voltage supply, 3.3 volt input.		3.2	3.3	3.4	Volts
I33	Quiescent Current draw, 3.3 volt input			230	TBS	mA
I33-max	Max current draw, positive 3.3 volt input.			300	TBS	mA
FCPU	CPU internal clock Frequency (PLL output)		25	375	375	MHz
FEMIF	EMIF bus frequency		-	100	-	MHz
	1. Power utilization of the MitySOM-1810 is heavily dependant on end-user application. Major factors include: ARM CPU PLL configuration, and external DDR2 RAM utilization.					

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 5: Standard Model Numbers

Model	ARM Speed	NOR Flash	NAND Flash	RAM	Operating Temp
1810-DX-225-RC	375 MHz	8MB	256MB	128MB	0°C to 70° C
1810-DX-225-RI	375 MHz	8MB	256MB	128MB	-40°C to 85° C

MECHANICAL INTERFACE

A mechanical outline of the MitySOM-1810 is illustrated in Figure 2, below.

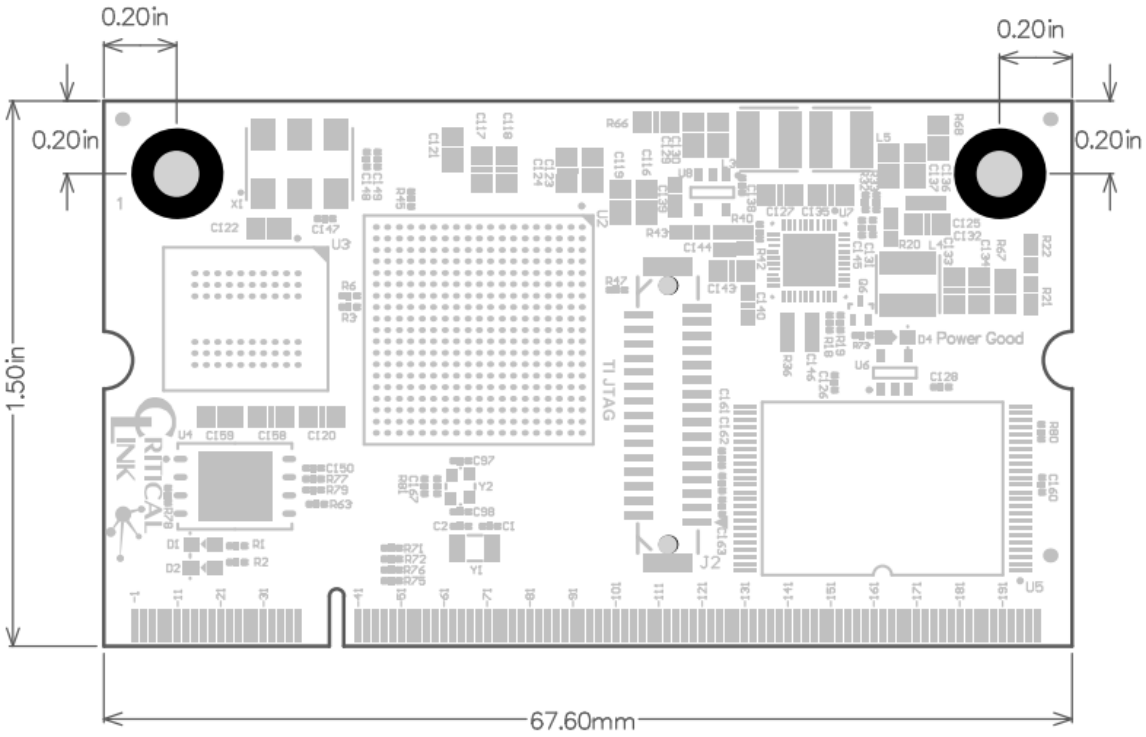

Figure 2 MitySOM-1810 Mechanical Outline

REVISION HISTORY

Date	Change Description
7-NOV-2010	Preliminary Draft, product overview
20-NOV-2010	Updates after initial review.
7-JAN-2011	Add SO-DIMM pinout table.
12-JUL-2011	Update NAND to indicate 8 bit data width. Update block diagram accordingly.
11-DEC-2012	Update Debug Header information, added MIL-STD-810F and Up To notation for RAM and NAND
27-MAR-2013	Added AM1810 processor pins with notes about on module resistors for specific pins as well as the OSCIN frequency.
5-MAR-2014	Update MitySOM product name.