

CMLDM7003  
CMLDM7003G\*  
CMLDM7003J

**SURFACE MOUNT SILICON  
DUAL N-CHANNEL  
ENHANCEMENT-MODE  
MOSFETS**



**SOT-563 CASE**

\* Device is **Halogen Free** by design



[www.centrasemi.com](http://www.centrasemi.com)

**DESCRIPTION:**

These CENTRAL SEMICONDUCTOR devices are dual N-Channel enhancement-mode MOSFETs, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7003 utilizes the USA pinout configuration, while the CMLDM7003J utilizes the Japanese pinout configuration. These devices offer low  $r_{DS(ON)}$  and ESD protection up to 2kV.

**MARKING CODES: CMLDM7003: C30  
CMLDM7003G\*: C3G  
CMLDM7003J: C3J**

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage  
Drain-Gate Voltage  
Gate-Source Voltage  
Continuous Drain Current  
Maximum Pulsed Drain Current  
Power Dissipation (Note 1)  
Power Dissipation (Note 2)  
Power Dissipation (Note 3)  
Operating and Storage Junction Temperature  
Thermal Resistance

SYMBOL		UNITS
$V_{DS}$	50	V
$V_{DG}$	50	V
$V_{GS}$	12	V
$I_D$	280	mA
$I_{DM}$	1.5	A
$P_D$	350	mW
$P_D$	300	mW
$P_D$	150	mW
$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
$\theta_{JA}$	357	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS PER TRANSISTOR:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=5.0\text{V}$			100	nA
$I_{GSSF}, I_{GSSR}$	$V_{GS}=10\text{V}$			2.0	$\mu\text{A}$
$I_{GSSF}, I_{GSSR}$	$V_{GS}=12\text{V}$			2.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=50\text{V}, V_{GS}=0$			50	nA
$BV_{DSS}$	$V_{GS}=0, I_D=10\mu\text{A}$	50			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.49		1.0	V
$V_{SD}$	$V_{GS}=0, I_S=115\text{mA}$			1.4	V
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=50\text{mA}$		1.6	3.0	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=50\text{mA}$		1.3	2.5	$\Omega$
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		1.1	2.0	$\Omega$
$g_{FS}$	$V_{DS}=10\text{V}, I_D=200\text{mA}$	200			mS
$C_{rss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			5.0	pF
$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			50	pF
$C_{oss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			25	pF
$Q_g(\text{tot})$	$V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$		0.764		nC
$Q_{gs}$	$V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$		0.148		nC
$Q_{gd}$	$V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$		0.156		nC

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm<sup>2</sup>

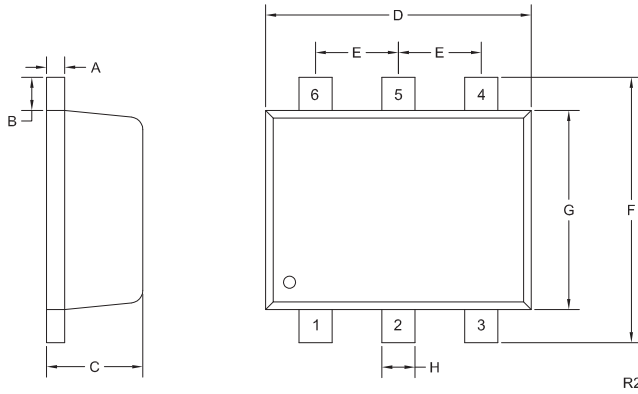
R9 (8-June 2015)

CMLDM7003  
 CMLDM7003G\*  
 CMLDM7003J

**SURFACE MOUNT SILICON  
 DUAL N-CHANNEL  
 ENHANCEMENT-MODE  
 MOSFETS**



**SOT-563 CASE - MECHANICAL OUTLINE**

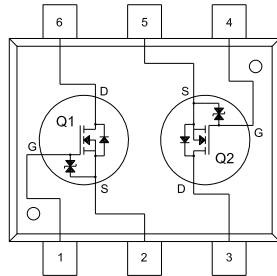


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0027	0.007	0.07	0.18
B	0.008		0.20	
C	0.017	0.024	0.45	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.059	0.067	1.50	1.70
G	0.043	0.051	1.10	1.30
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R2)

**PIN CONFIGURATIONS**

**CMLDM7003 (USA Pinout)  
 CMLDM7003G\***



**LEAD CODE:**

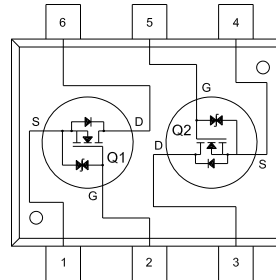
- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

**MARKING CODES:**

CMLDM7003: C30  
 CMLDM7003G\*: C3G

\* Device is *Halogen Free* by design

**CMLDM7003J (Japanese Pinout)**



**LEAD CODE:**

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

**MARKING CODE: C3J**

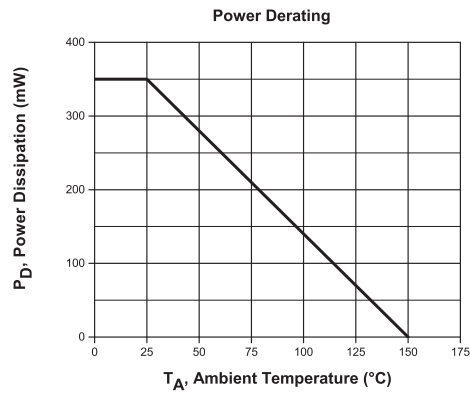
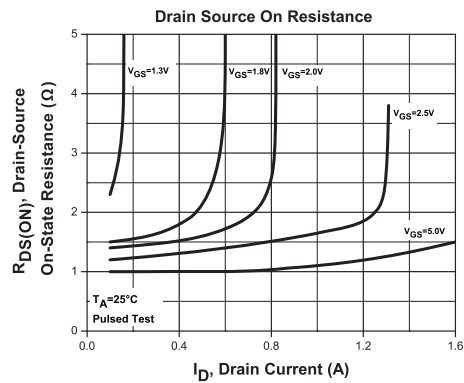
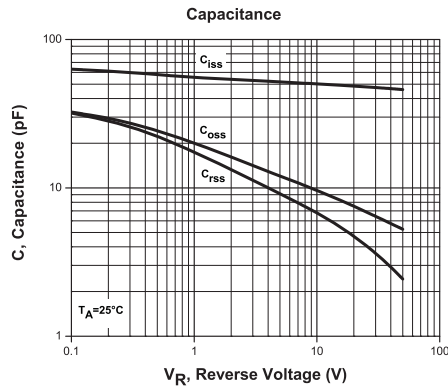
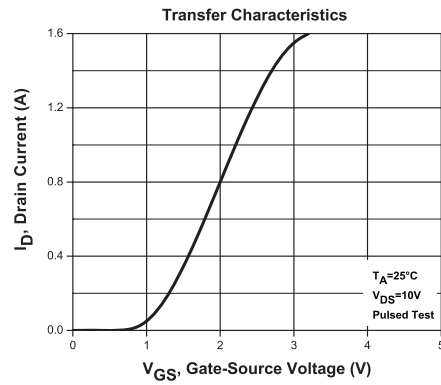
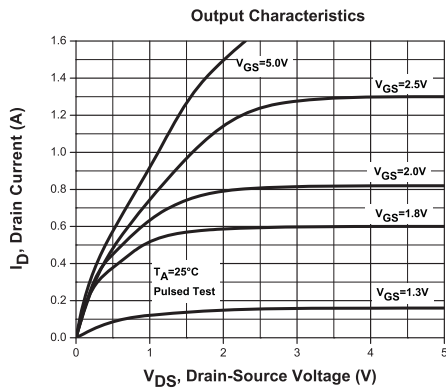
R9 (8-June 2015)

CMLDM7003  
 CMLDM7003G\*  
 CMLDM7003J

SURFACE MOUNT SILICON  
 DUAL N-CHANNEL  
 ENHANCEMENT-MODE  
 MOSFETS



TYPICAL ELECTRICAL CHARACTERISTICS



R9 (8-June 2015)

## OUTSTANDING SUPPORT AND SUPERIOR SERVICES



---

### PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

---

### DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2<sup>nd</sup> day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

---

### REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

---

### CONTACT US

#### Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.  
145 Adams Avenue  
Hauppauge, NY 11788 USA  
Main Tel: (631) 435-1110  
Main Fax: (631) 435-1824  
Support Team Fax: (631) 435-3388  
[www.centrasemi.com](http://www.centrasemi.com)

**Worldwide Field Representatives:**  
[www.centrasemi.com/wwreps](http://www.centrasemi.com/wwreps)

**Worldwide Distributors:**  
[www.centrasemi.com/wwdistributors](http://www.centrasemi.com/wwdistributors)

---

For the latest version of Central Semiconductor's **LIMITATIONS AND DAMAGES DISCLAIMER**, which is part of Central's Standard Terms and Conditions of sale, visit: [www.centrasemi.com/terms](http://www.centrasemi.com/terms)