2N5060 THRU 2N5064

SILICON CONTROLLED RECTIFIERS
0.8 AMP, 30 THRU 200 VOLT

TO-92 CASE

Central Semiconductor Corp.

www.centralsemi.com

The CENTRAL SEMICONDUCTOR 2N5060 series devices are epoxy molded SCRs designed for control systems and sensing circuit applications.

MARKING: FULL PART NUMBER

MAXIMUM RATINGS: (T_A=25°C unless otherwise noted)

	SYMBOL	2N5060	2N5061	2N5062	2N5063	2N5064	UNITS
Peak Repetitive Off-State Voltage	V_{DRM}, V_{RRM}	30	60	100	150	200	V
RMS On-State Current (Note 1; T_C=80°C)	$I_{T(RMS)}$			0.8			A
Average On-State Current (Note 1; T_C=67°C)	$I_{T(AV)}$			0.51			A
Average On-State Current (Note 1; T_C=102°C)	$I_{T(AV)}$			0.255			A
Peak One Cycle Surge Current (60Hz)	I_{TSM}			10			A
I^2t Value for Fusing (t=8.3ms)	I^2t			0.4			A^2s
Peak Forward Gate Power (tp≤1.0μs)	P_{GM}			0.1			W
Average Forward Gate Power (t=8.3ms)	$P_{G(AV)}$			0.01			W
Peak Forward Gate Current (tp≤1.0μs)	I_{GM}			1.0			A
Peak Reverse Gate Voltage (tp≤1.0μs)	V_{RGM}			5.0			V
Operating Junction Temperature	T_J			-40 to +125			°C
Storage Temperature	T_{stg}			-40 to +150			°C
Thermal Resistance (Note 2)	Θ_{JC}			75			°C/W
Thermal Resistance	Θ_{JA}			200			°C/W

Notes: 1) 180° Conduction Angles
2) Measured with the “flat side down” on a heatsink and held in position by a metal clamp over the curved surface.

ELECTRICAL CHARACTERISTICS: (T_C=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DRM}, I_{RRM}	V_D=Rated V_{DRM}, R_{GK}=1.0kΩ			10	μA
I_{DRM}, I_{RRM}	V_D=Rated V_{DRM}, R_{GK}=1.0kΩ, T_C=110°C			50	μA
I_{GT}	V_D=7.0V, R_L=100Ω			200	μA
I_{GT}	V_D=7.0V, R_L=100Ω, T_C=-40°C			350	μA
I_H	Initiating Current, I_T=20mA, R_{GK}=1.0kΩ			5.0	mA
I_H	Initiating Current, I_T=20mA, R_{GK}=1.0kΩ, T_C=-40°C			10	mA
V_{GT}	V_D=7.0V, R_L=100Ω			0.8	V
V_{GT}	V_D=7.0V, R_L=100Ω, T_C=-40°C			1.2	V
V_{GD}	V_D=Rated V_{DRM}, R_L=100Ω, T_C=110°C	0.1			V
V_{TM}	I_{TM}=1.2A, T_A=25°C			1.7	V
dv/dt	V_D=Rated V_{DRM}, R_{GK}=1.0kΩ		30		V/μs

R5 (7-May 2015)

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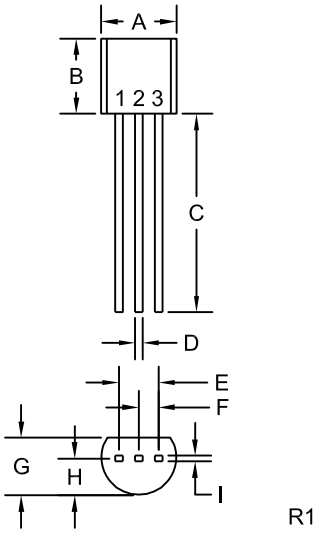
ELECTRICAL CHARACTERISTICS - Continued: (T_C=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	2N5060 2N5061 TYP	2N5062 2N5063 2N5064 TYP	UNITS
t_d	V_D=Rated V_{DRM}, I_{GT}=1.0mA,	3.0	3.0	μs
t_r	Forward Current=1.0A, di/dt=6.0A/μs	0.2	0.2	μs
t_q	Forward Current=1.0A, tp=50μs, 0.1% Duty Cycle, di/dt=6.0A/μs, dv/dt=20V/μs, I_{GT}=1.0mA	10	30	μs

TO-92 CASE - MECHANICAL OUTLINE



R1

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A (DIA)	0.175	0.205	4.45	5.21
B	0.170	0.210	4.32	5.33
C	0.500	-	12.70	-
D	0.016	0.022	0.41	0.56
E	0.100		2.54	
F	0.050		1.27	
G	0.125	0.165	3.18	4.19
H	0.080	0.105	2.03	2.67
I	0.015		0.38	

TO-92 (REV: R1)

LEAD CODE:
1) Cathode
2) Gate
3) Anode

MARKING:
FULL PART NUMBER

OUTSTANDING SUPPORT AND SUPERIOR SERVICES

PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centralsemi.com

Worldwide Field Representatives:
www.centralsemi.com/wwreps

Worldwide Distributors:
www.centralsemi.com/wwdistributors