



# +2.5V Low-Power Precision Voltage Reference

**REF43**

## 1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at [www.analog.com/REF43](http://www.analog.com/REF43)

## 2.0 Part Number. The complete part number(s) of this specification follow:

| Part Number | Description   |
|-------------|---|
| REF43-803J  | +2.5V Low-Power Precision Voltage Reference                   |
| REF43-803L  | +2.5V Low-Power Precision Voltage Reference                   |
| REF43-803RC | +2.5V Low-Power Precision Voltage Reference                   |
| REF43-803Z  | +2.5V Low-Power Precision Voltage Reference                   |
| REF43R803J  | Radiation Tested, +2.5V Low-Power Precision Voltage Reference |
| REF43R803L  | Radiation Tested, +2.5V Low-Power Precision Voltage Reference |
| REF43R803RC | Radiation Tested, +2.5V Low-Power Precision Voltage Reference |
| REF43R803Z  | Radiation Tested, +2.5V Low-Power Precision Voltage Reference |

## 2.1 Case Outline

| Letter | Descriptive designator <sup>1</sup> | Case Outline (Lead Finish per MIL-PRF-38535) |
|--------|-------------------------------------|--|
| J      | MACY1-X8                            | 8-Lead Can                                   |
| L      | GDFP1-F10                           | 10-lead cerpac                               |
| RC     | CQCC1-N20                           | 20-Terminal leadless chip carrier            |
| Z      | GDIP1-T8                            | 8-Lead ceramic dual-in-line package (CERDIP) |

<sup>1</sup> See MIL-STD-1835

## 3.0 Absolute Maximum Ratings. (T<sub>A</sub> = 25°C, unless otherwise noted)

|  |                |
|--|----------------|
| Supply voltage .....                         | 40V            |
| Power dissipation.....                       | 500mW          |
| Output short circuit duration .....          | Indefinite     |
| Storage Temperature range.....               | -65° to +150°C |
| Operating temperature range .....            | -55° to +125°C |
| Lead temperature (soldering, 60 sec) .....   | +300°C         |
| Junction Temperature (T <sub>J</sub> ) ..... | +175°C         |

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## 3.1 Thermal Characteristics:

| Package Type       | Junction-to-Case<br>( $\Theta_{JC}$ ) | Junction-to-Ambient<br>( $\Theta_{JA}$ ) | Units    |
|--------------------|---------------------------------------|--|----------|
| J (TO-99 Package)  | 45                                    | 150                                      | °C/W Max |
| L (CERPAC Package) | 22                                    | 141                                      | °C/W Max |
| RC (LCC Package)   | 35                                    | 110                                      | °C/W Max |
| Z (CERDIP Package) | 26                                    | 120                                      | °C/W Max |

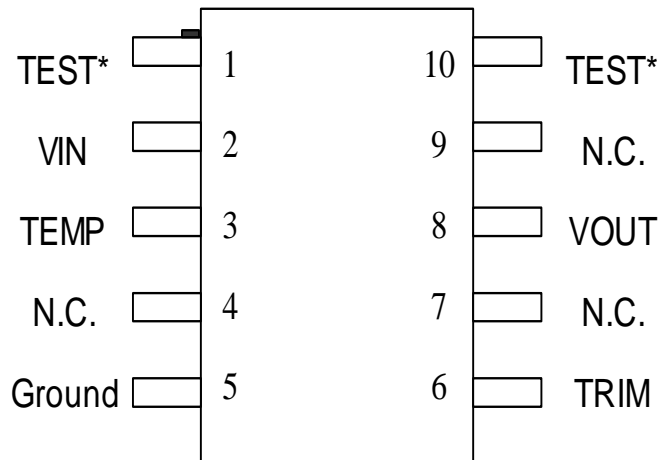
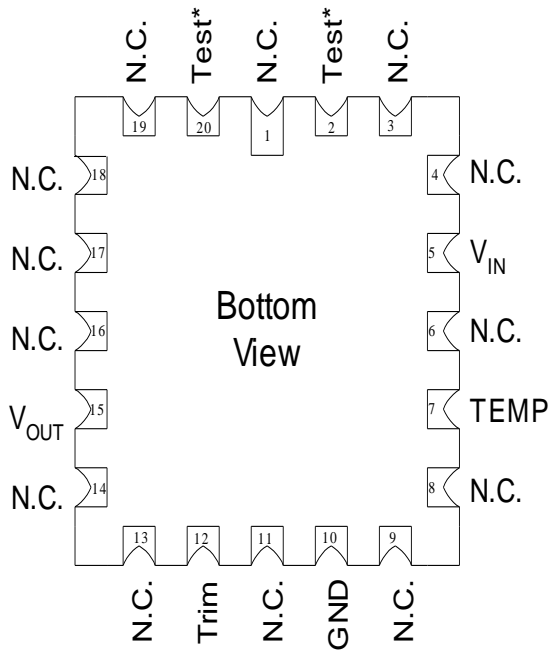
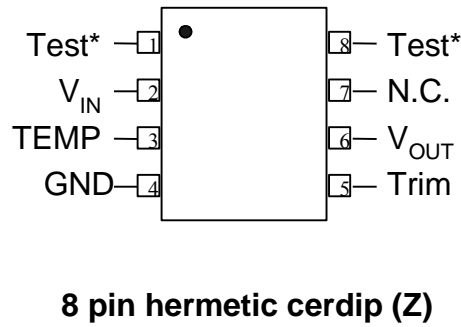
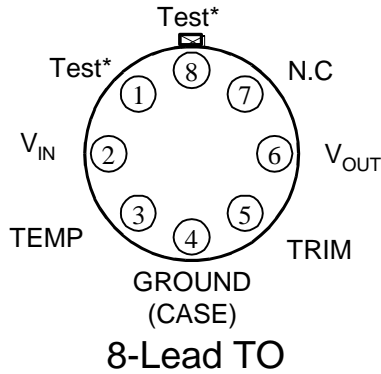


Figure 1 - Terminal connections.

\* Reserved for factory testing. Make no electrical connection to these pins.

## 4.0 Electrical Table: See notes at end of table

| Table I   |                             |                               |         |            |           |           |        |        |
|---|-----------------------------|-------------------------------|---------|------------|-----------|-----------|--------|--------|
| Parameter   | Symbol                      | Conditions <sup>1/</sup>      | Package | Sub-group  | Limit Min | Limit Max | Units  |        |
| Output voltage  | V <sub>O</sub>              | ALL                           | ALL     | 1          | 2.4975    | 2.5025    | V      |        |
|   |                             |                               |         | 2, 3       | 2.4950    | 2.5050    |        |        |
|   |                             |                               |         | M, D, L, R | ALL       | 1         |        | 2.4900 |
| Output voltage temperature co-efficient <sup>3/</sup> | TC <sub>V<sub>O</sub></sub> | ALL                           | ALL     | 8          |           | 15        | ppm/°C |        |
| Temperature voltage output <sup>4/</sup>              | V <sub>T</sub>              | ALL                           | ALL     | 1          | 0.54      | 0.58      | V      |        |
|   |                             |                               |         | 2          | 0.72      | 0.78      |        |        |
|   |                             |                               |         | 3          | 0.38      | 0.43      |        |        |
| Load regulation                                       | LD <sub>REG</sub>           | I <sub>L</sub> = 0mA to 10mA  | ALL     | J, Z       | 1         | 20        | ppm/mA |        |
|   |                             |                               |         | J, Z, RC   | 2, 3      | 40        |        |        |
|   |                             |                               |         | L, RC      | 1         | 28        |        |        |
|   |                             |                               |         | L          | 2, 3      | 50        |        |        |
|   |                             |                               |         | M, D, L, R | J, Z, RC  | 1         |        | 60     |
|   |                             |                               |         | L          | 1         | 70        |        |        |
| Line regulation                                       | LN <sub>REG</sub>           | V <sub>IN</sub> = 4.5V to 40V | ALL     | 1          | 2         | ppm/V     |        |        |
|   |                             |                               |         | 2, 3       | 3         |           |        |        |
|   |                             |                               |         | M, D, L, R | ALL       |           | 1      | 100    |
| Short circuit current <sup>4/</sup>                   | I <sub>SC</sub>             | V <sub>O</sub> = 0V           | ALL     | 1          | 100       | mA        |        |        |
|   |                             |                               |         | 2, 3       | 120       |           |        |        |
| Supply current  | I <sub>SY</sub>             | ALL                           | ALL     | 1          | 450       | μA        |        |        |
|   |                             |                               |         | 2, 3       | 600       |           |        |        |
|   |                             |                               |         | M, D, L, R | ALL       |           | 1      | 450    |
| Output adjustment range <sup>4/</sup>                 | ΔV <sub>TRIM</sub>          | ALL                           | ALL     | 1          | ±3        |           | %      |        |
| Load current <sup>2/</sup>                            | I <sub>L</sub>              | ALL                           | ALL     | 1, 2, 3    | 10        |           | mA     |        |
| Wideband output noise                                 | enRMS                       | ALL                           | ALL     | 7          |           | 10        | μVRMS  |        |

## TABLE I NOTES:

- <sup>1</sup> V<sub>IN</sub> = 5V, unless otherwise specified. NOTE: Output decoupling is not generally required or recommended on the REF43. In applications that require output decoupling, care will need to be taken when choosing the capacitor due to the ESR of the capacitor. If capacitors with very low ESR are chosen it may be necessary to add some additional resistance in series with the capacitor to limit the initial charge current when power is applied to the REF43. Adding series resistance when low ESR capacitors are used will help with the stability of the REF43 when power is applied over the entire temperature range. Contact ADI Aerospace applications for more detailed application information.
- <sup>2</sup> Guaranteed by Load regulation test.
- <sup>3</sup> Output voltage temperature coefficient is measured by the box method. The tempco is defined as the slope of the diagonal of a box drawn around the output voltage plotted against temperature. V<sub>OUT</sub> is measured at T<sub>MIN</sub> and T<sub>MAX</sub>. The lowest of these readings is subtracted from the highest reading and the resulting difference is divided by (T<sub>MAX</sub> - T<sub>MIN</sub>).
- <sup>4</sup> Not tested post-irradiation.

**4.1 Electrical Test Requirements:**

| <b>Table II</b>                         |   |
|---|---|
| Test Requirements                       | Subgroups (in accordance with MIL-PRF-38535, Table III) |
| Interim Electrical Parameters           | 1   |
| Final Electrical Parameters             | 1, 2, 3, 8 <u>1/</u> <u>2/</u>                          |
| Group A Test Requirements               | 1, 2, 3, 7, 8   |
| Group C end-point electrical parameters | 1 <u>2/</u>   |
| Group D end-point electrical parameters | 1   |
| Group E end-point electrical parameters | 1   |

1/ PDA applies to subgroup 1. Delta's excluded from PDA.  
 2/ See table III for delta measurement parameters. See Table I for test conditions.

**4.2 Table III. Lifetest / Burn-in delta limits.**

| <b>Table III</b> |                  |                   |             |       |
|------------------|------------------|-------------------|-------------|-------|
| TEST TITLE       | BURN-IN ENDPOINT | LIFETEST ENDPOINT | DELTA LIMIT | UNITS |
| VO               | 2.50 ±0.0025     | 2.50 ±0.005       | ±0.0025     | V     |
| ISY              | 450              | 495               | ±45         | µA    |

**5.0 Life Test/Burn-In Circuit:**

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

| Rev | Description of Change  | Date           |
|-----|--|----------------|
| A   | Initiate   | 26-May-00      |
| B   | Add subgroup 8 to table II, Add L package, update table III  | Mar. 27, 2001  |
| C   | Update web address. Table II – delete subgroup 7 from final electrical parameters and add subgroup 7 to Group A Test Requirements. | Feb. 14, 2002  |
| D   | Update web address. Delete burn-in circuit.  | May 29, 2003   |
| E   | Changed CERPAC Load Regulation limit from 20ppm/mA to 28ppm/mA. Add package column on electrical table                             | Feb. 03, 2005  |
| F   | Update Table I Load Regulation specs   | April 27, 2006 |
| G   | Update Table I Load Regulation specs.  | Feb. 13, 2007  |
| H   | Update header/footer and add to 1.0 Scope description.   | Feb. 21, 2008  |
| I   | Add temperature junction (T <sub>j</sub> )...+175°C to 3.0 Absolute Max. Ratings.  | April 4, 2008  |
| J   | Correct typo in Section 2 part numbers to be “R803” parts.   | Sep. 5, 2008   |
| K   | Add application note on output capacitive load sensitivity when using low ESR capacitors.  | Oct. 5, 2012   |
| L   | Correct typo on Theta JC/JA symbol   | Oct. 15, 2012  |
| M   | Change Load Regulation limit for RC package for Sub Group 1  | March 30, 2016 |