Low Noise Amplifier, 0.4 GHz to 10 GHz

Data Sheet

HMC8412CHIPS

FEATURES

- **Low noise figure: 1.5 dB typical**
- **Single positive supply (self biased)**
- **High gain: ≤15 dB typical**
- **High OIP3: 32 dBm typical**
- **V_{DD}: 5 V at I_{DQ} = 60 mA**
- **50 Ω matched input and output**
- **Die size: 0.945 mm × 1.545 mm × 0.102 mm**

APPLICATIONS

- **Test instrumentation**
- **Military and space**
- **Telecommunications infrastructure**
- **Software defined radios**
- **Electronic warfare**
- **Radar applications**

FUNCTIONAL BLOCK DIAGRAM

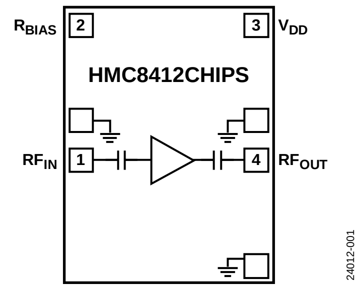

Figure 1.

GENERAL DESCRIPTION

The HMC8412CHIPS is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise amplifier that operates from 0.4 GHz to 10 GHz. The HMC8412CHIPS provides ≤15 dB of typical gain, ≤19 dBm typical output power at 1 dB gain compression (OP1dB), and a typical output third-order intercept (OIP3) of 32 dBm.

The HMC8412CHIPS requires 60 mA from a 5 V supply on V_{DD}. The HMC8412CHIPS also features inputs and outputs (I/Os) that are internally matched to 50 Ω and facilitates integration into multichip modules (MCMs). In addition, the bias choke to the HMC8412CHIPS and the dc blocking capacitors on the RF_{IN} and RF_{OUT} pads are integrated, creating a small form factor solution.

Rev. 0 **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

8/2020—Revision 0: Initial Version

SPECIFICATIONS

0.4 GHz TO 8 GHz FREQUENCY RANGE

V_{DD} = 5 V, supply current (I_{DQ}) = 60 mA, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.4		8	GHz	
GAIN (S21)	13	15		dB	
Gain Variation over Temperature		0.01		dB/°C	
NOISE FIGURE		1.5		dB	
RETURN LOSS					
Input (S11)		17		dB	
Output (S22)		14		dB	
OUTPUT					
OP1dB	17	19		dBm	
Saturated Output Power (P_{SAT})		20		dBm	
OIP3		32		dBm	Measurement taken at output power (P_{OUT}) per tone = 0 dBm
Output Second-Order Intercept (OIP2)		38		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
POWER ADDED EFFICIENCY (PAE)		29		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		60		mA	
V_{DD}	3	5	6	V	

8 GHz TO 10 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 60 mA, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8		10	GHz	
GAIN (S21)	13	14.5		dB	
Gain Variation over Temperature		0.018		dB/°C	
NOISE FIGURE		1.7		dB	
RETURN LOSS					
Input (S11)		20		dB	
Output (S22)		15		dB	
OUTPUT					
OP1dB	11.5	14.5		dBm	
P_{SAT}		19		dBm	
OIP3		32		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		43		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		15		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		60		mA	
V_{DD}	3	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD}	7 V
RF Input Power	25 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 12.2 mW/°C Above 85°C)	1.1 W
Temperature	
Channel	175°C
Storage Range	−65°C to +150°C
Operating Range	−55°C to +85°C
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 60 mA)	113.4°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the printed circuit board (PCB) thermal design is required.

θ_{JC} is the junction-to-case thermal resistance, channel to bottom of die using die attach epoxy.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
C-4-5	94.6	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

ESD Ratings for HMC8412CHIPS

Table 5. HMC8412CHIPS, 4-Pad Die

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

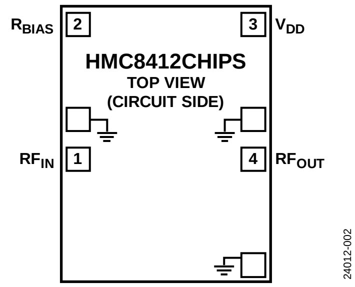

Figure 2. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RF_{IN}	RF Input. The RF_{IN} pad is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
	GND	Ground. The GND pads must be connected to the RF and dc ground. See Figure 6 for the interface schematic.
2	R_{BIAS}	Bias Resistor. See Figure 3 for the interface schematic.
3	V_{DD}	Drain Bias Voltage for the Amplifier. See Figure 5 for the interface schematic.
4	RF_{OUT}	RF Output. The RF_{OUT} pad is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.

INTERFACE SCHEMATICS

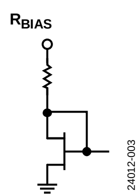

Figure 3. R_{BIAS} Interface Schematic

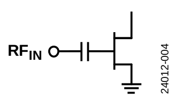

Figure 4. RF_{IN} Interface Schematic

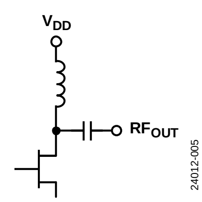

Figure 5. RF_{OUT} and V_{DD} Interface Schematic

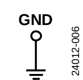

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

SMALL SIGNAL RESPONSE

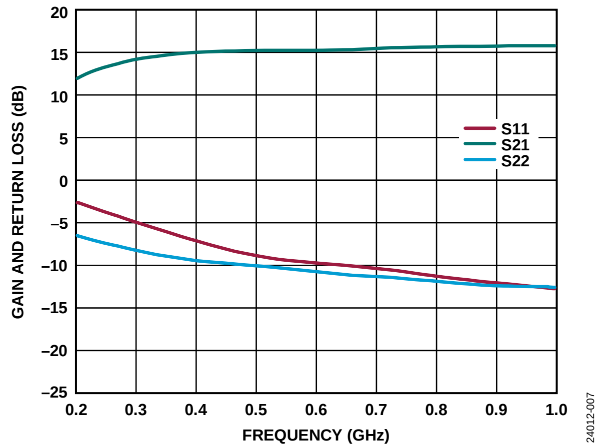

Figure 7. Gain and Return Loss vs. Frequency, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

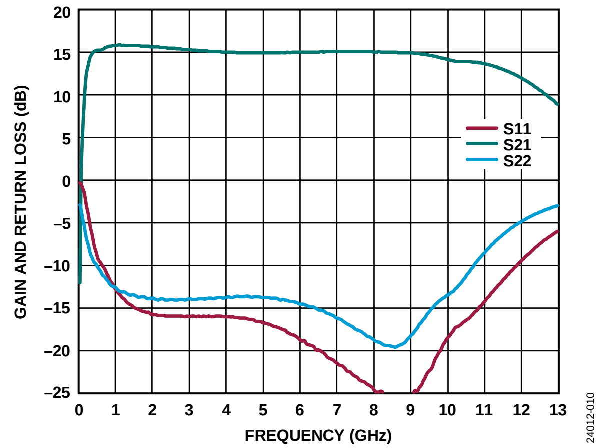

Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 60 mA

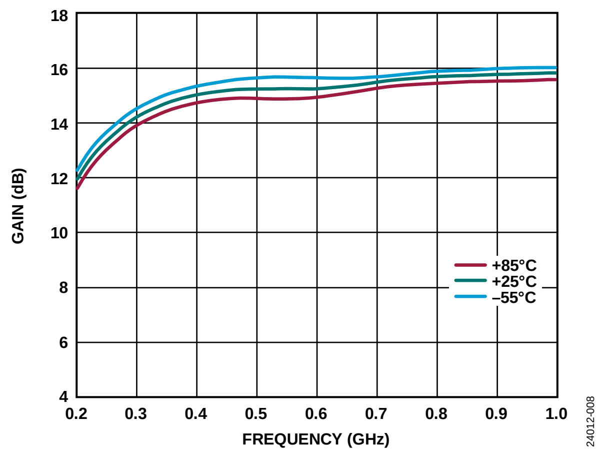

Figure 8. Gain vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

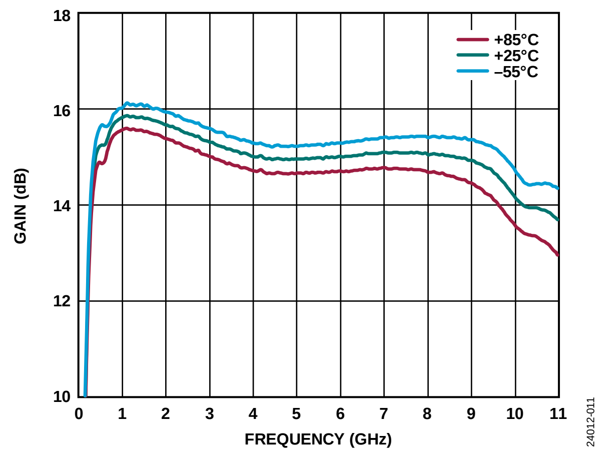

Figure 11. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

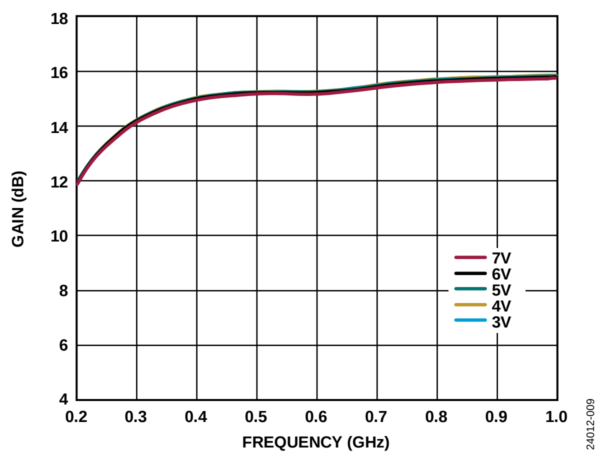

Figure 9. Gain vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

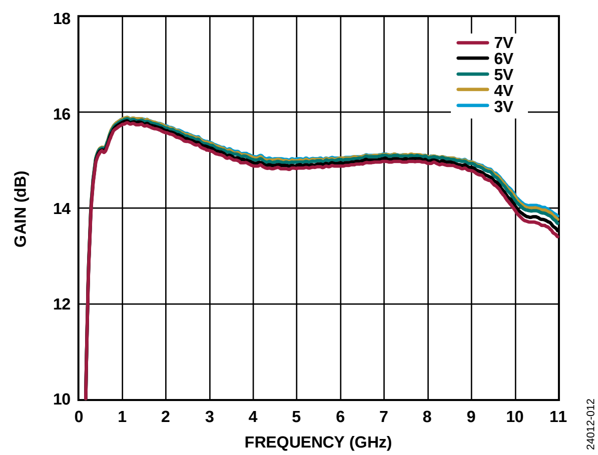

Figure 12. Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

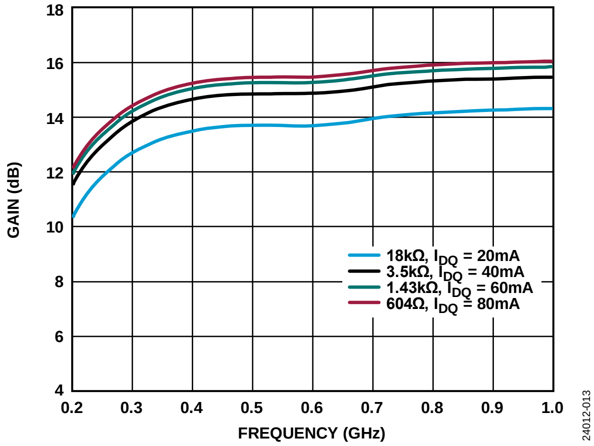

Figure 13. Gain vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

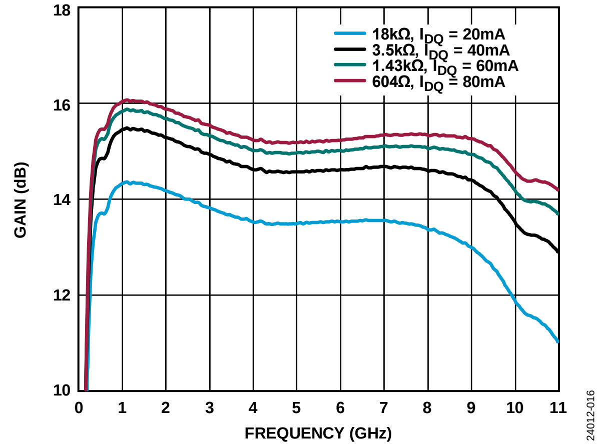

Figure 16. Gain vs. Frequency for Various Supply Currents, V_{DD} = 5 V

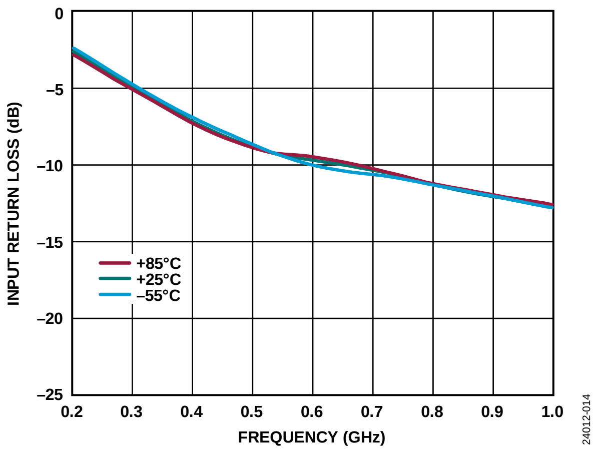

Figure 14. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

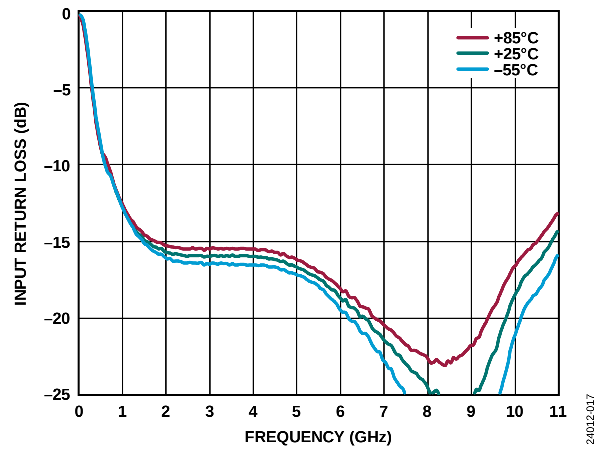

Figure 17. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

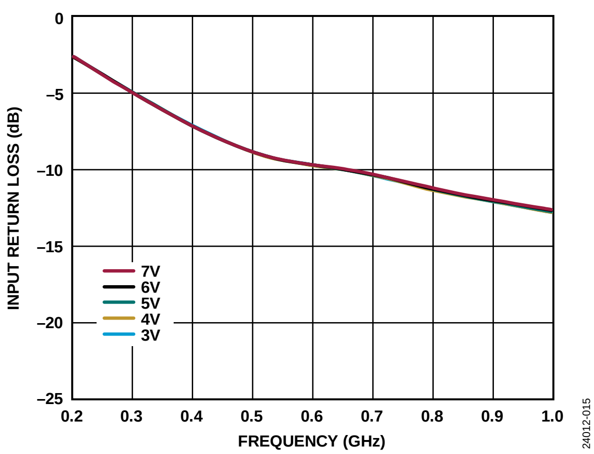

Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

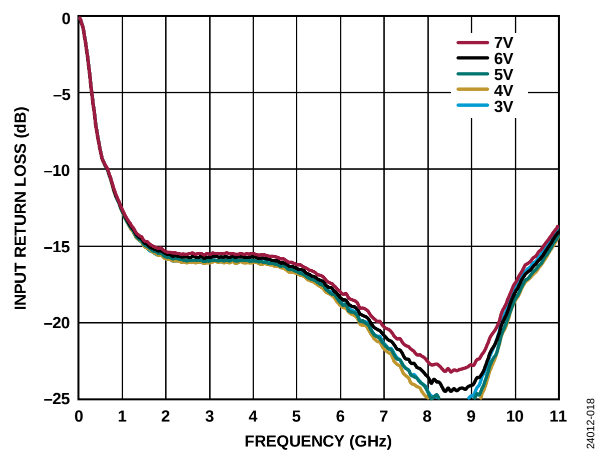

Figure 18. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

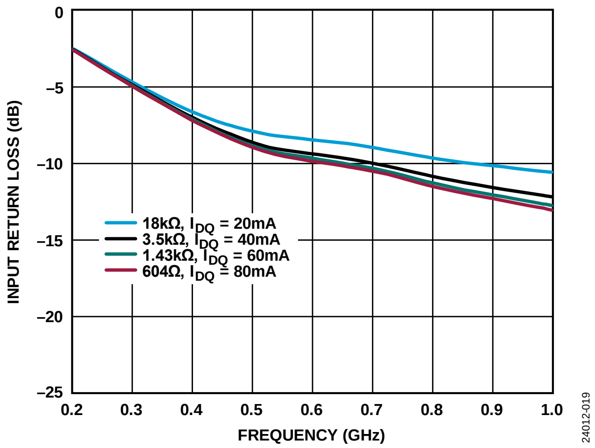

Figure 19. Input Return Loss vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

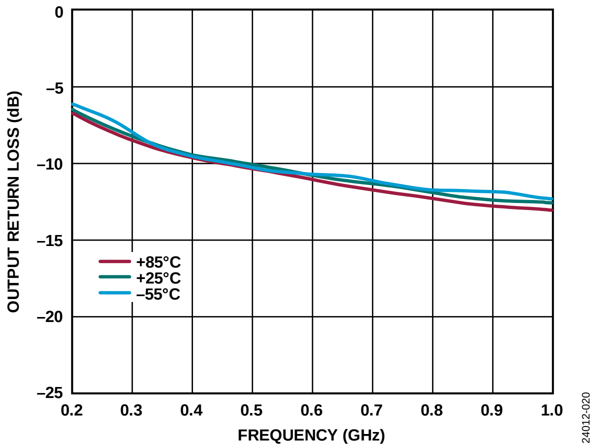

Figure 20. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

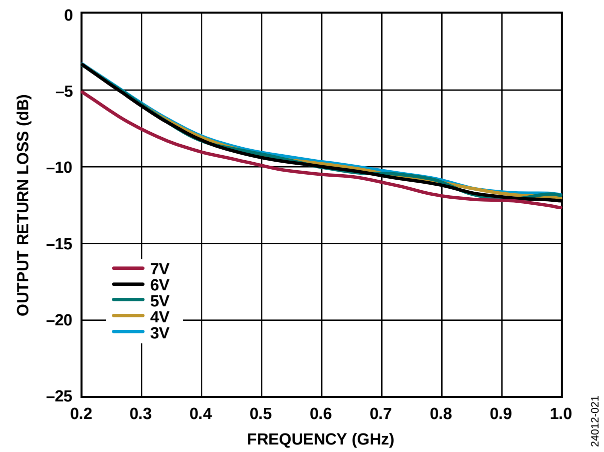

Figure 21. Output Return Loss vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

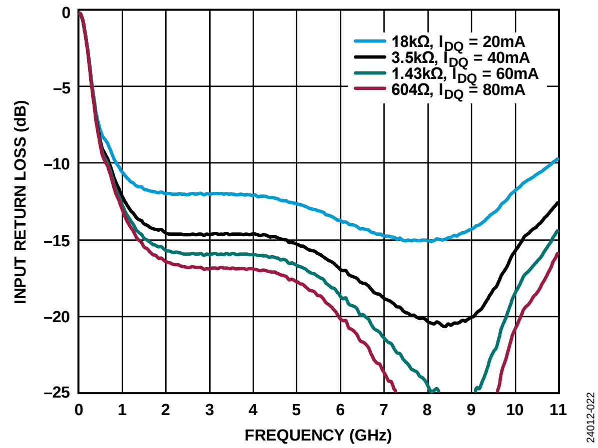

Figure 22. Input Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 5 V

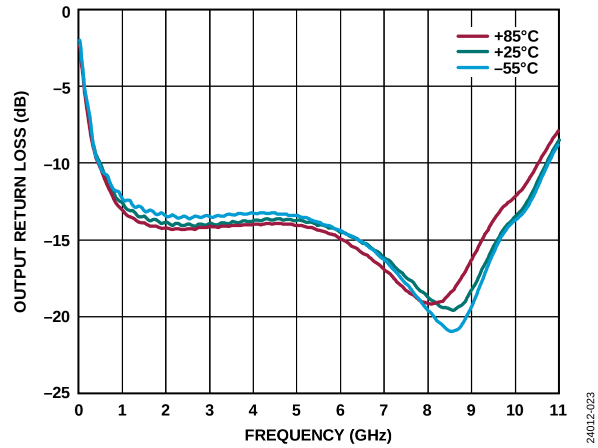

Figure 23. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

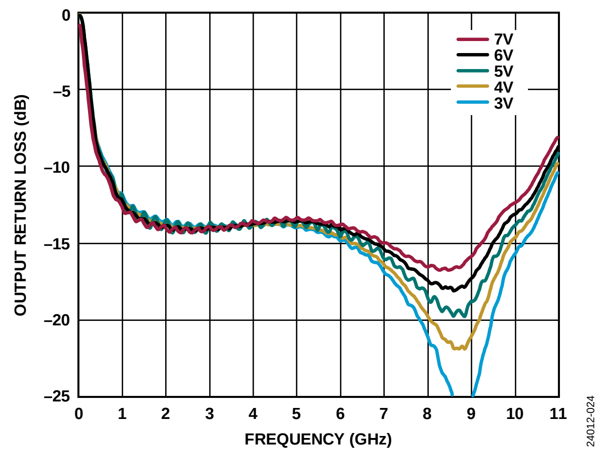

Figure 24. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

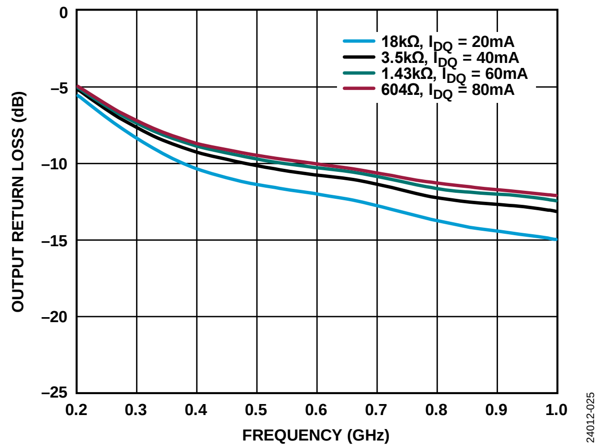

Figure 25. Output Return Loss vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

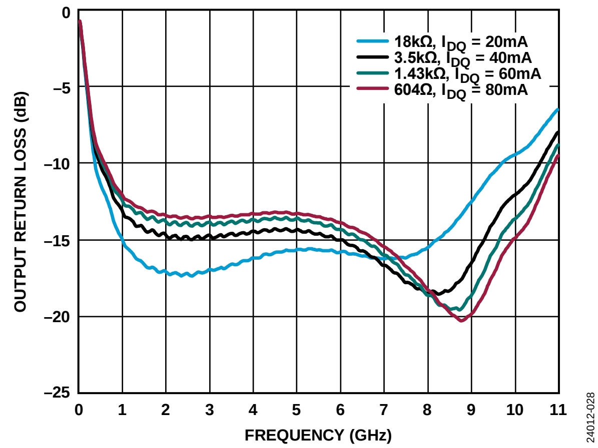

Figure 28. Output Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 5 V

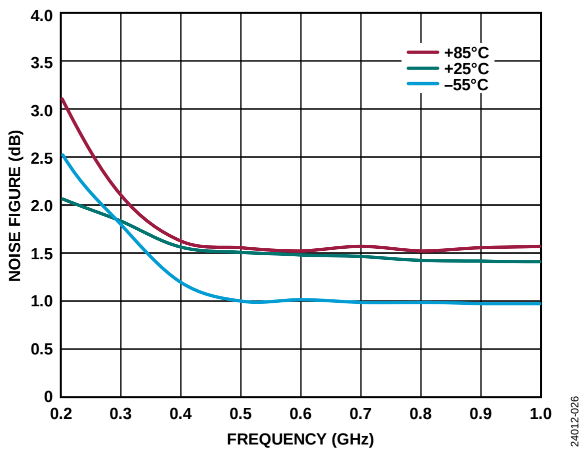

Figure 26. Noise Figure vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

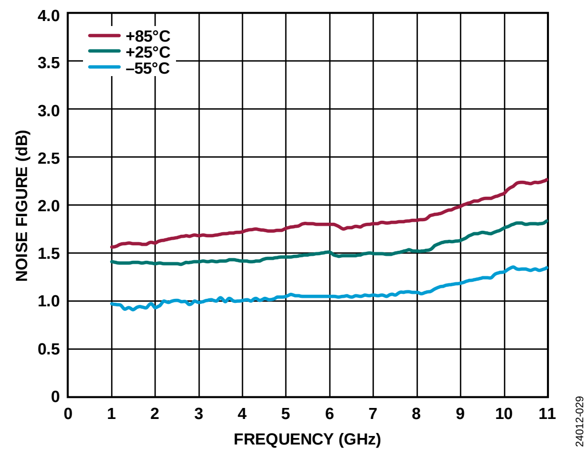

Figure 29. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

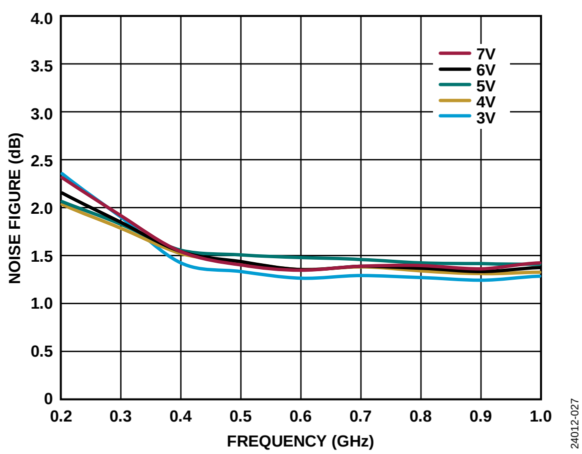

Figure 27. Noise Figure vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

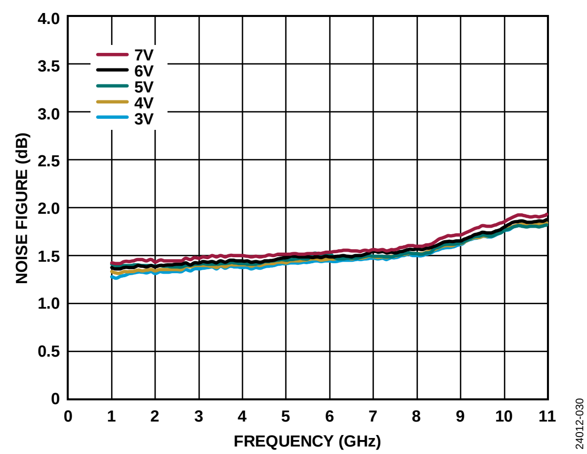

Figure 30. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

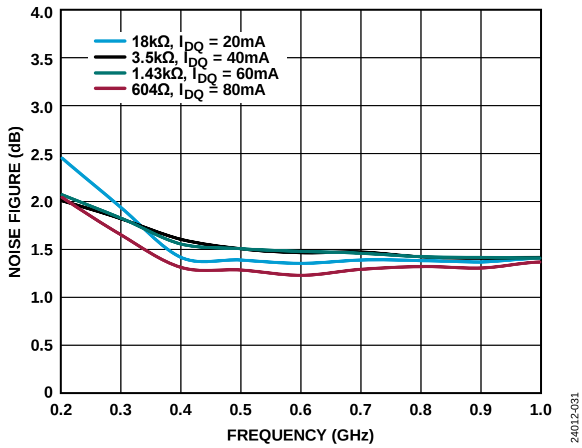

Figure 31. Noise Figure vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

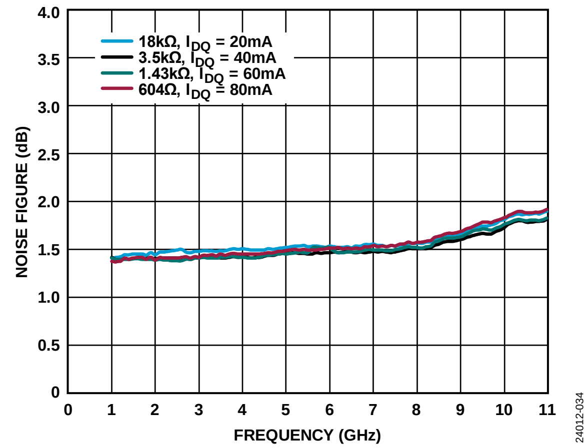

Figure 34. Noise Figure vs. Frequency for Various Supply Currents, V_{DD} = 5 V

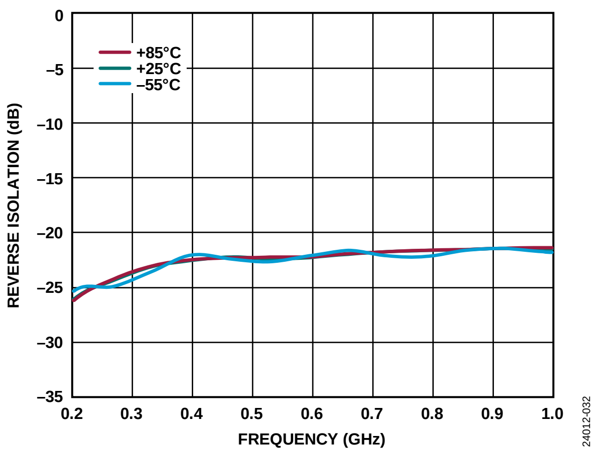

Figure 32. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

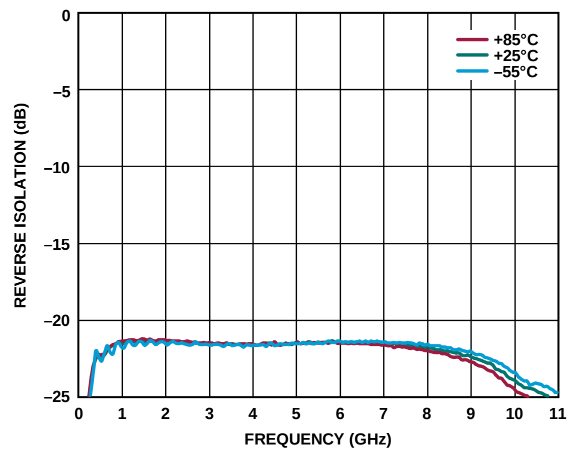

Figure 35. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

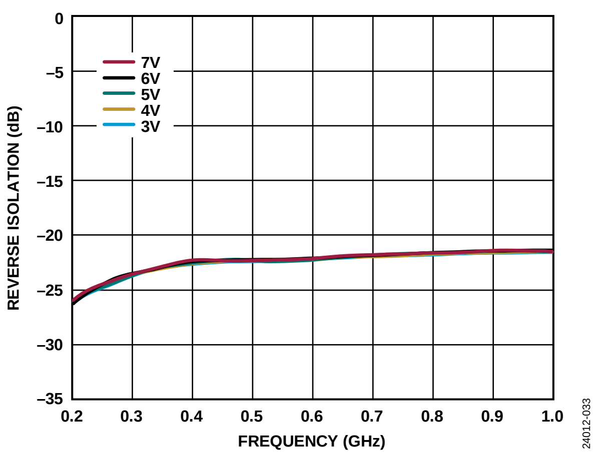

Figure 33. Reverse Isolation vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

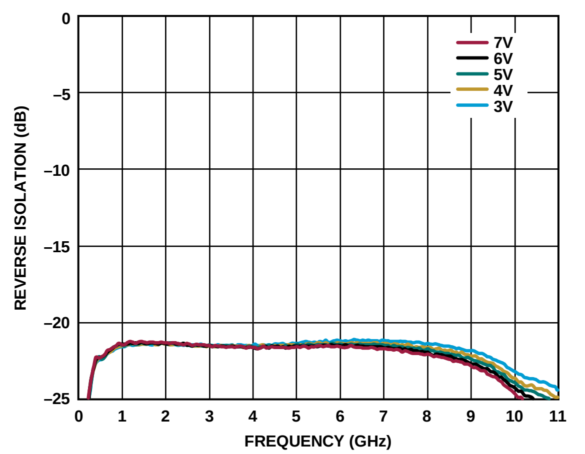

Figure 36. Reverse Isolation vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

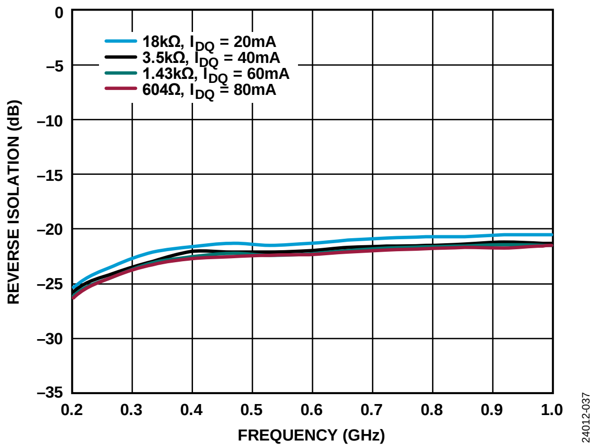

Figure 37. Reverse Isolation vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

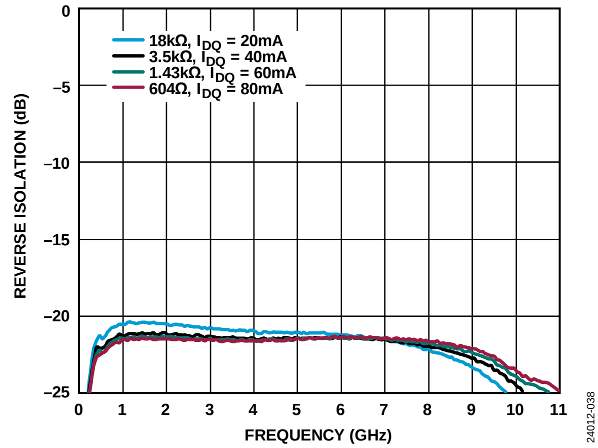

Figure 38. Reverse Isolation vs. Frequency for Various Supply Currents, V_{DD} = 5 V

LARGE SIGNAL RESPONSE

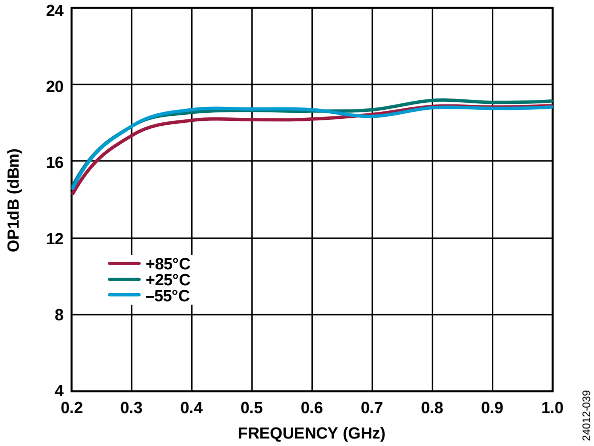

Figure 39. OP1dB vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

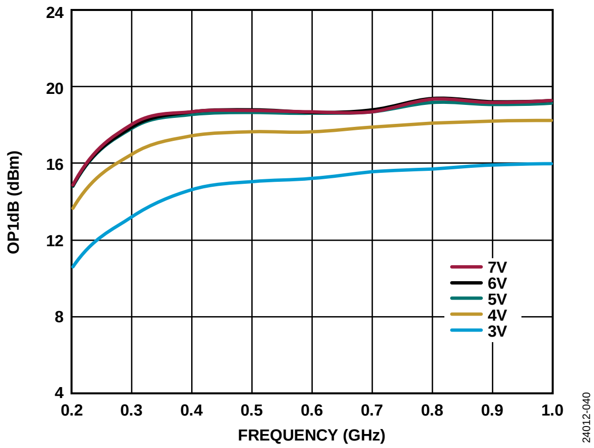

Figure 40. OP1dB vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

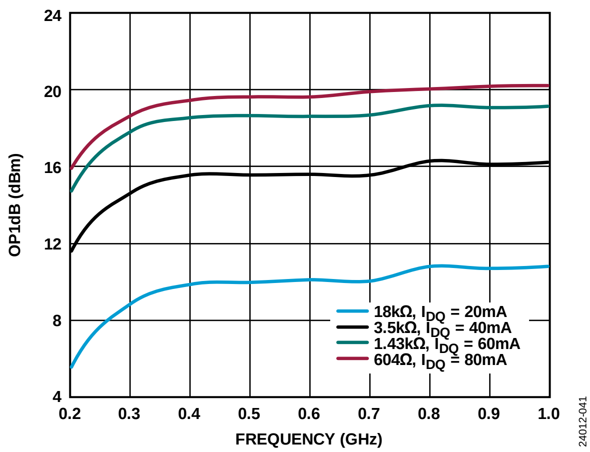

Figure 41. OP1dB vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

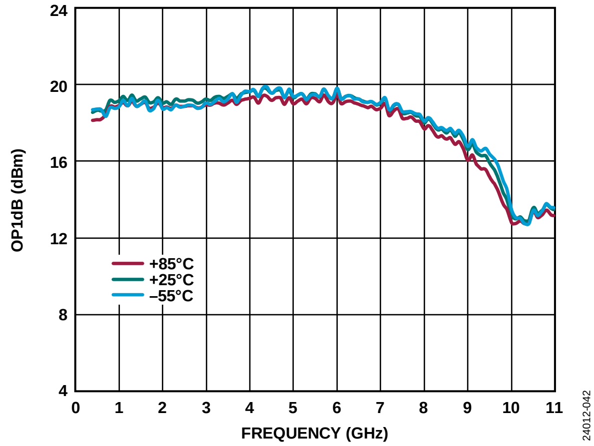

Figure 42. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

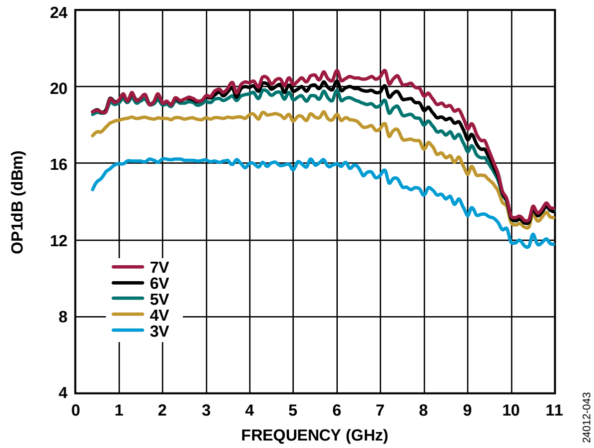

Figure 43. OP1dB vs. Frequency at Various Supply Voltages, I_{DQ} = 60 mA

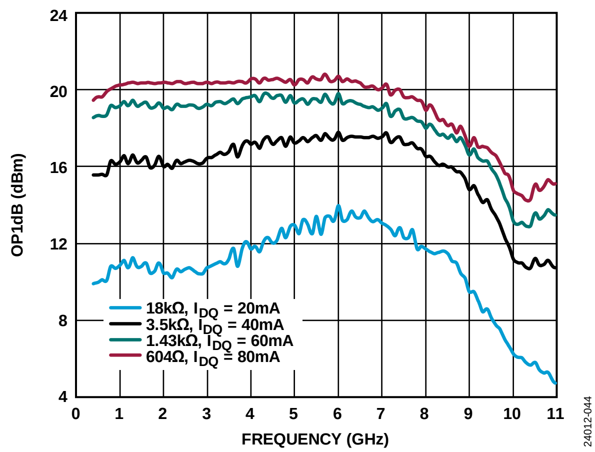

Figure 44. OP1dB vs. Frequency for Various Supply Currents, V_{DD} = 5 V

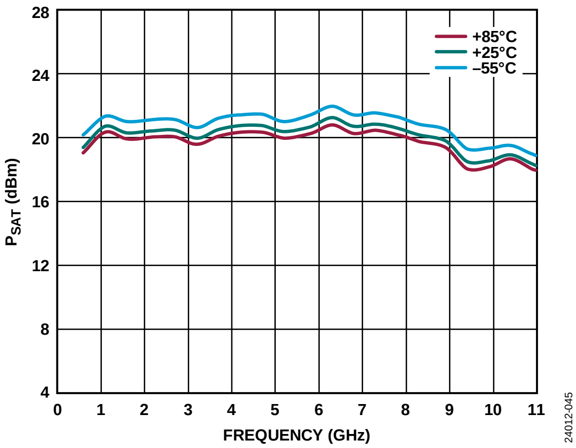

Figure 45. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

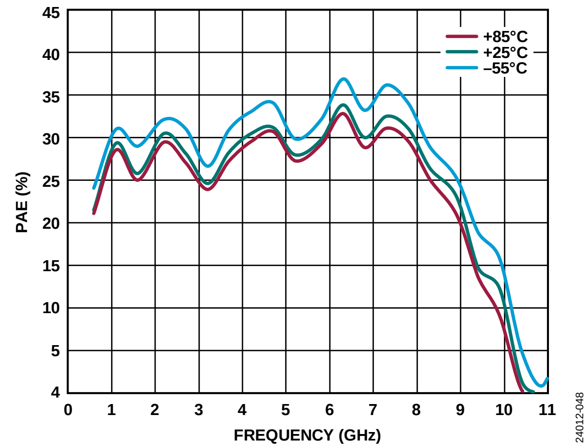

Figure 48. PAE vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA

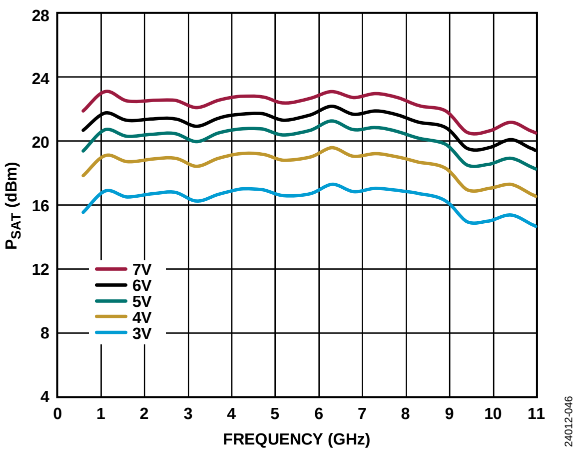

Figure 46. P_{SAT} vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

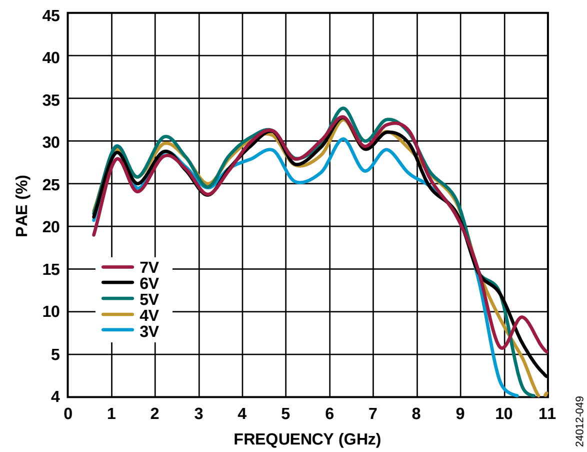

Figure 49. PAE vs. Frequency at Various Supply Voltages, I_{DQ} = 60 mA

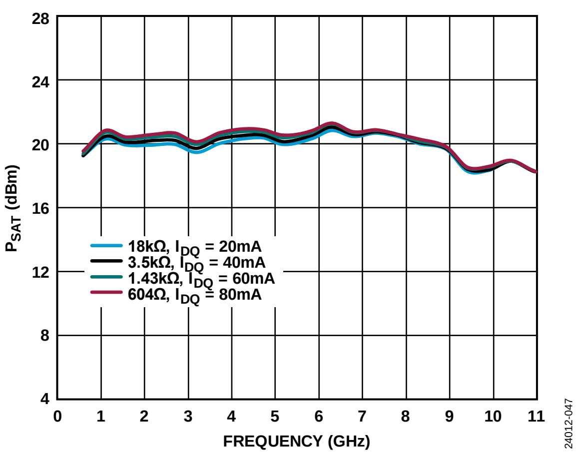

Figure 47. P_{SAT} vs. Frequency for Various Supply Currents, V_{DD} = 5 V

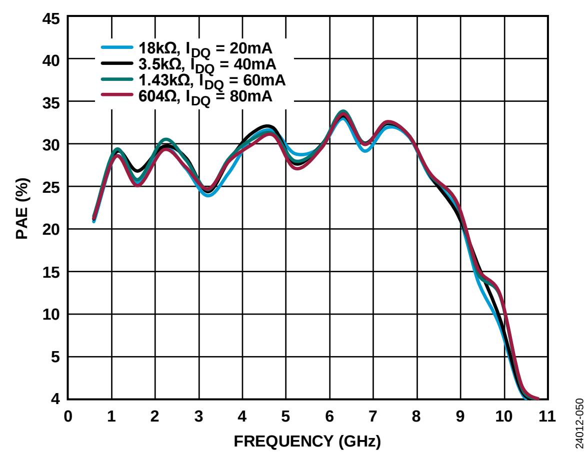

Figure 50. PAE vs. Frequency for Various Supply Currents, V_{DD} = 5 V

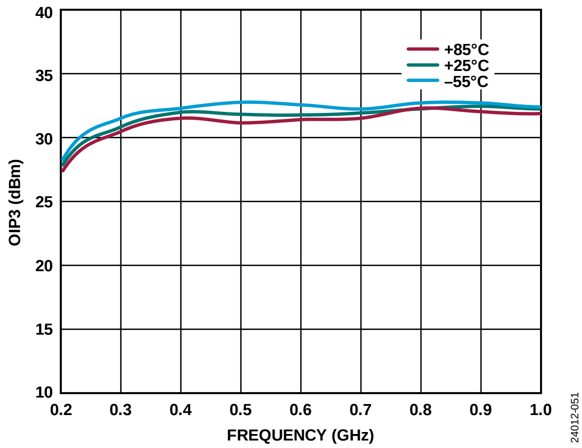

Figure 51. OIP3 vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, P_{OUT} = 0 dBm per Tone

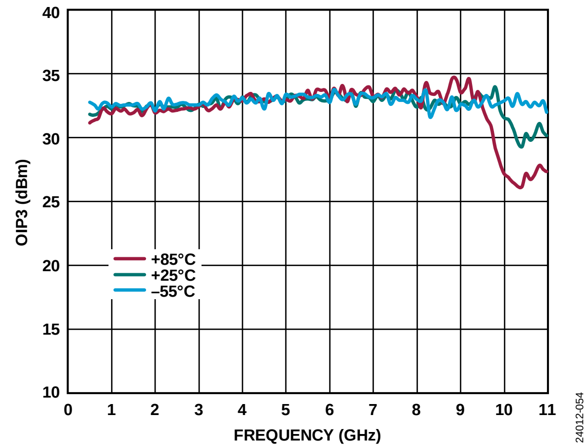

Figure 54. OIP3 vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA, P_{OUT} = 0 dBm per Tone

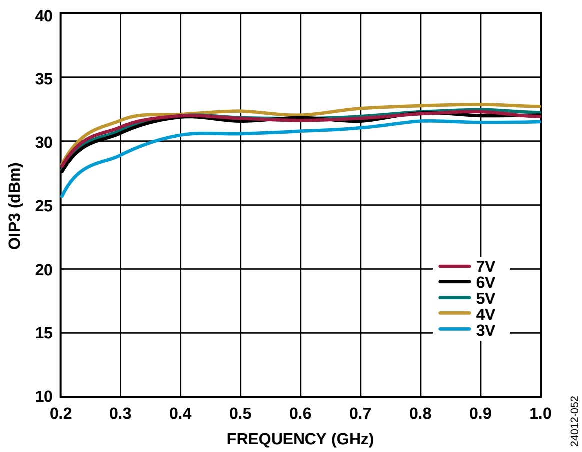

Figure 52. OIP3 vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

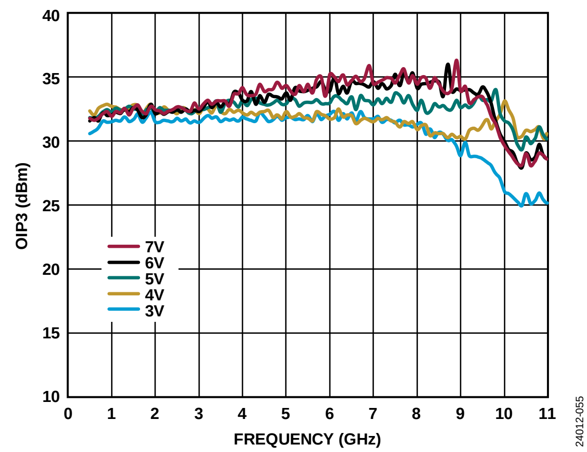

Figure 55. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

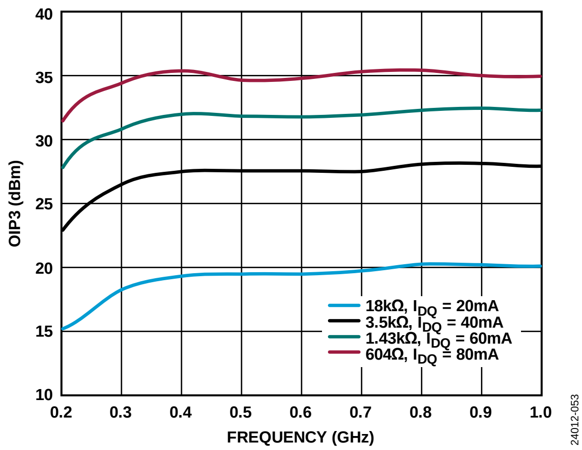

Figure 53. OIP3 vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

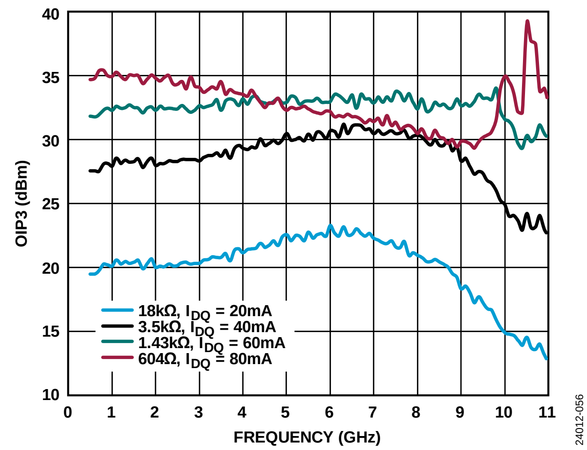

Figure 56. OIP3 vs. Frequency for Various Supply Currents, V_{DD} = 5 V

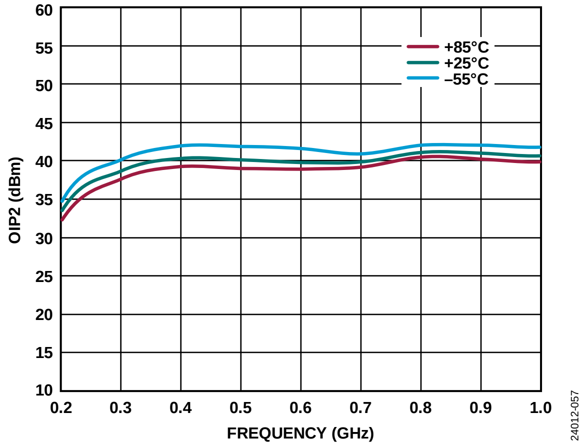

Figure 57. OIP2 vs. Frequency for Various Temperatures, 200 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, P_{OUT} = 0 dBm per Tone

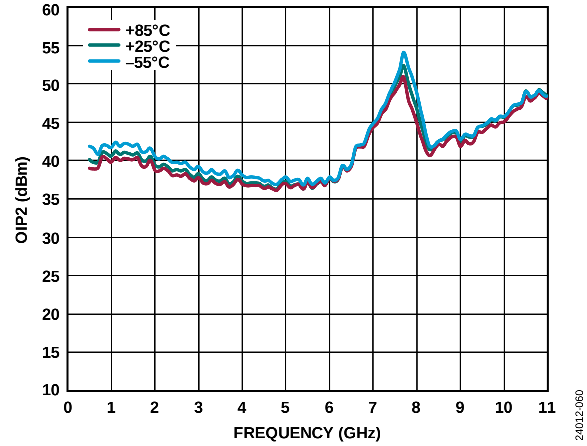

Figure 60. OIP2 vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 60 mA, P_{OUT} = 0 dBm per Tone

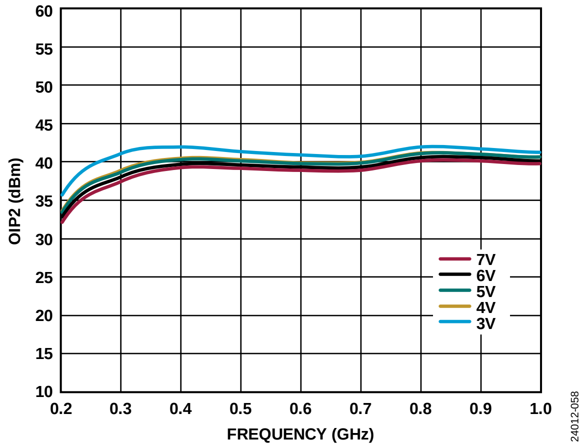

Figure 58. OIP2 vs. Frequency for Various Supply Voltages, 200 MHz to 1 GHz, I_{DQ} = 60 mA

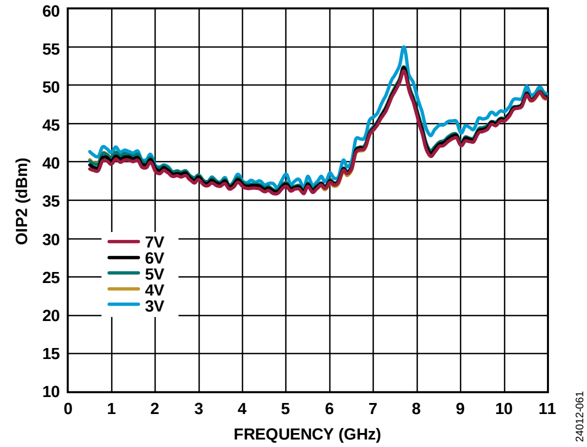

Figure 61. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA

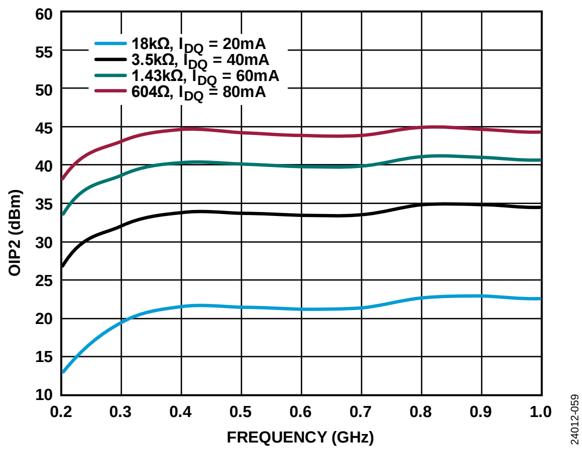

Figure 59. OIP2 vs. Frequency for Various Supply Currents, 200 MHz to 1 GHz, V_{DD} = 5 V

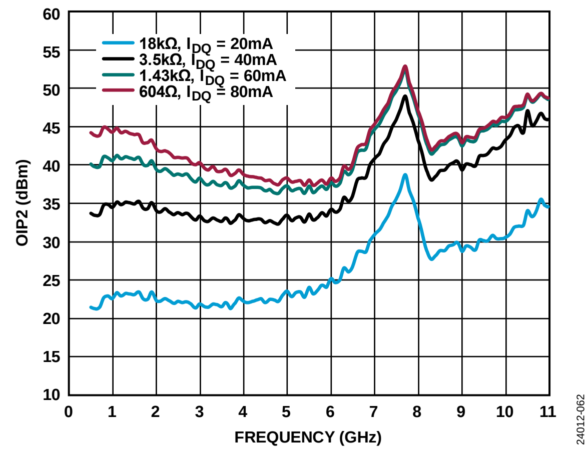

Figure 62. OIP2 vs. Frequency for Various Supply Currents, V_{DD} = 5 V

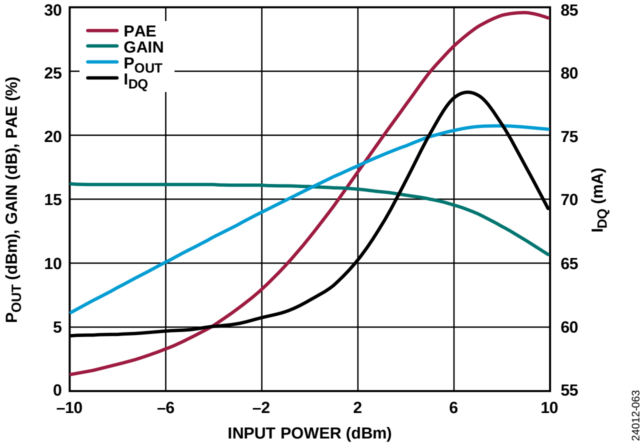

Figure 63. P_{OUT}, Gain, PAE, and I_{DQ} vs. Input Power, Power Compression at 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

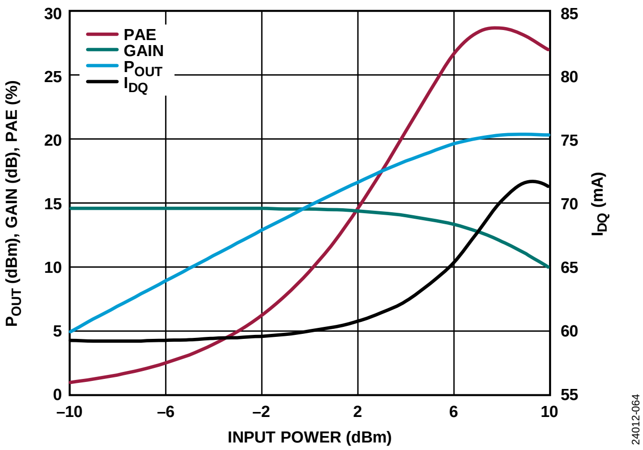

Figure 64. P_{OUT}, Gain, PAE, and I_{DQ} vs. Input Power, Power Compression at 5 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

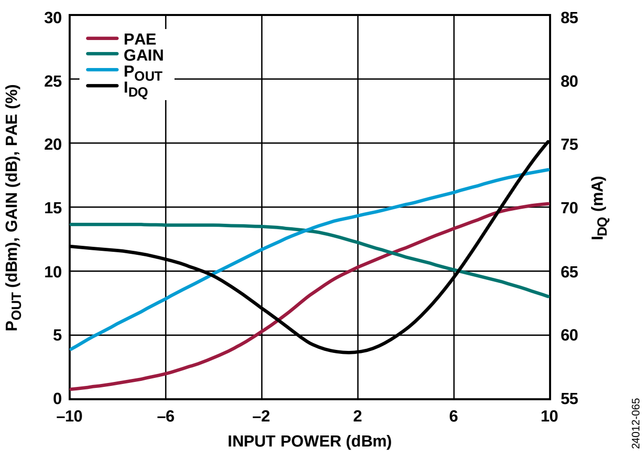

Figure 65. P_{OUT}, Gain, PAE, and I_{DQ} vs. Input Power, Power Compression at 10 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA

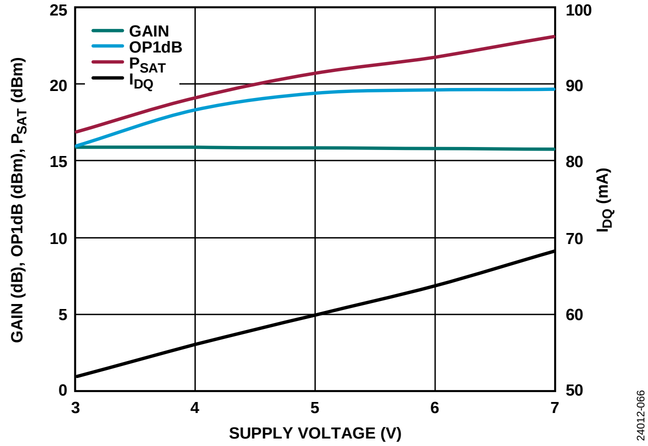

Figure 66. Gain, OP1dB, P_{SAT}, and I_{DQ} vs. Supply Voltage, Power Compression at 1 GHz, R_{BIAS} = 1.43 kΩ

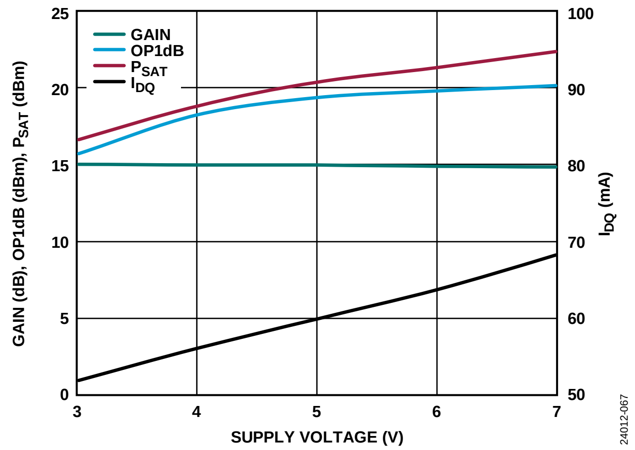

Figure 67. Gain, OP1dB, P_{SAT}, and I_{DQ} vs. Supply Voltage, Power Compression at 5 GHz, R_{BIAS} = 1.43 kΩ

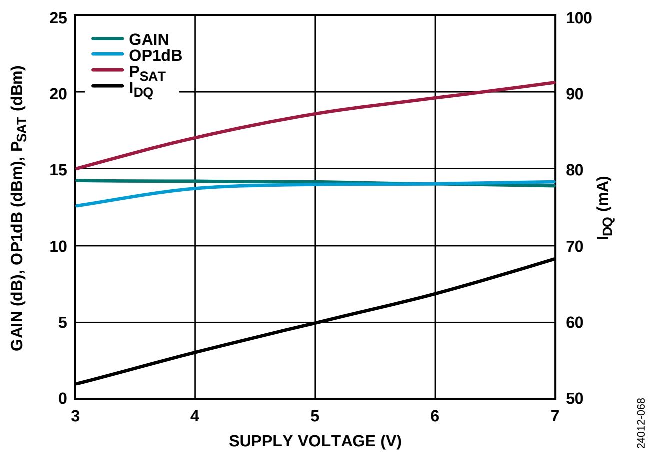

Figure 68. Gain, OP1dB, P_{SAT}, and I_{DQ} vs. Supply Voltage, Power Compression at 10 GHz, R_{BIAS} = 1.43 kΩ

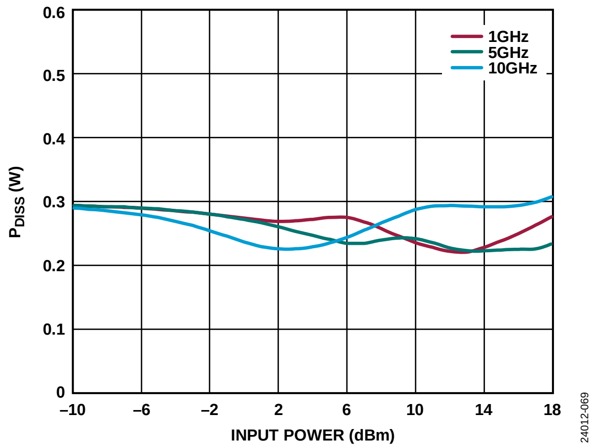

Figure 69. P_{DISS} vs. Input Power at T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 60 mA

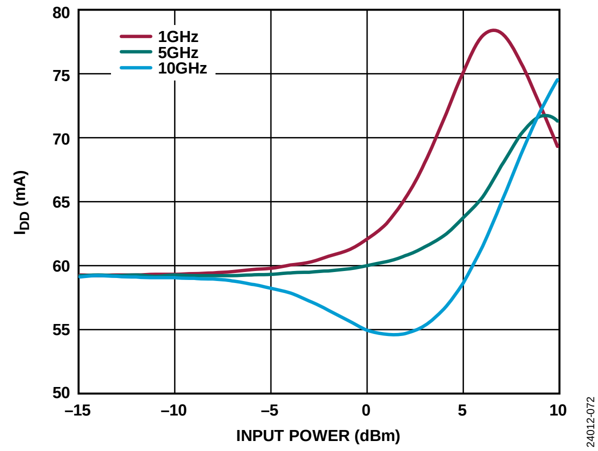

Figure 71. Drain Current (I_{DD}) vs. Input Power for Various Frequencies, V_{DD} = 5 V, R_{BIAS} = 1.43 kΩ

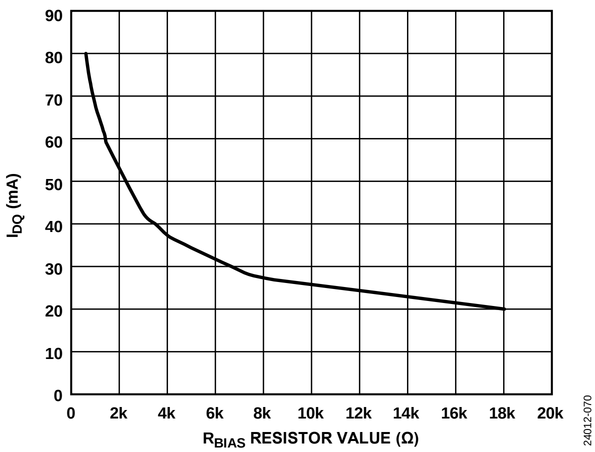

Figure 70. I_{DQ} vs. R_{BIAS} Resistor Value, V_{DD} = 5 V

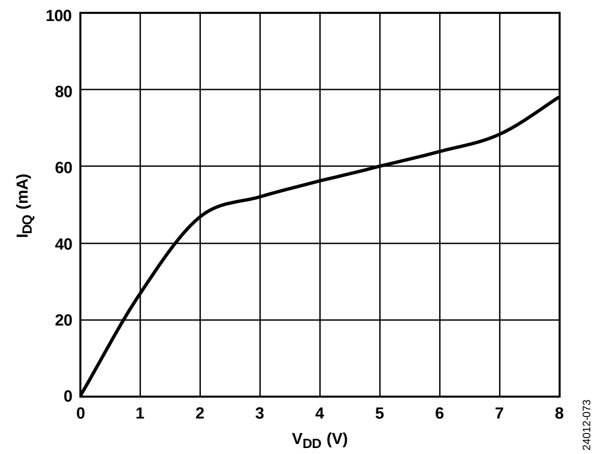

Figure 72. I_{DQ} vs. V_{DD}, R_{BIAS} = 1.43 kΩ

THEORY OF OPERATION

The HMC8412CHIPS is a GaAs, MMIC, pHEMT, low noise wideband amplifier with integrated ac-coupling capacitors and a bias inductor. A simplified block diagram is shown in Figure 73.

The HMC8412CHIPS has ac-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 0.4 GHz to 10 GHz frequency range. No external matching components are required. To adjust the drain bias current, connect an external resistor between the R_{BIAS} and V_{DD} pads.

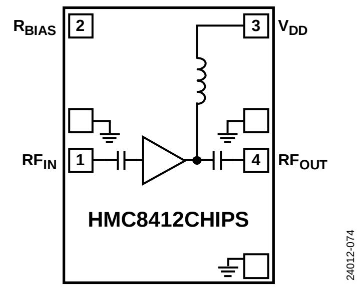

Figure 73. Simplified Block Diagram

APPLICATIONS INFORMATION

The basic connections for operating the HMC8412CHIPS over the specified frequency range are shown in Figure 74. No external biasing inductor is required, allowing the 5 V supply to be connected to the V_{DD} pad. The 4.7 µF, 0.01 µF, and 100 pF power supply decoupling capacitors are recommended. The power supply decoupling capacitors shown in Figure 74 represent the configuration used to characterize and qualify the HMC8412CHIPS. It is possible to reduce the number of capacitors, but this reduction varies from system to system. It is recommended to first remove the largest capacitors that are farthest from the device when reducing the number of capacitors.

To set I_{DQ}, connect a resistor, R1, between the R_{BIAS} and V_{DD} pads (see Figure 74). A default value of 1.43 kΩ is recommended, which results in a nominal I_{DQ} of 60 mA. Table 7 shows how the I_{DQ} varies vs. the bias resistor value. The R_{BIAS} pad also draws a current that varies with the value of R_{BIAS} (see Table 7). Do not leave the R_{BIAS} pad open.

TYPICAL APPLICATION CIRCUIT

Figure 74 shows the typical application circuit of the HMC8412CHIPS.

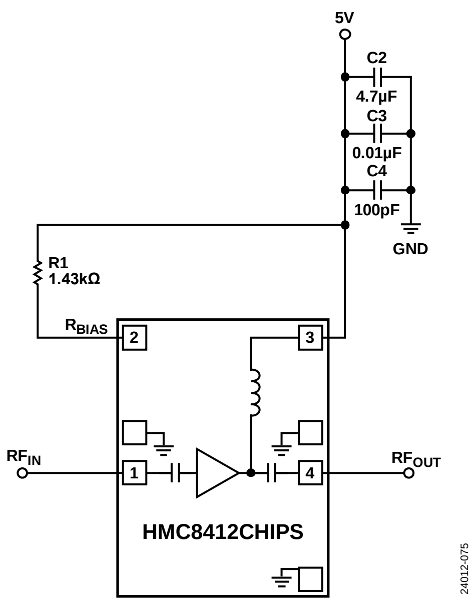

Figure 74. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

During Power-Up

To power up, follow this bias sequence:

1. Set V_{DD} to 5 V.
2. Apply the RF signal.

During Power-Down

To power down, follow this bias sequence:

1. Turn off the RF signal.
2. Set V_{DD} to 0 V.

Table 7. Recommended Bias Resistor Values

R_{BIAS} (Ω)	Total Current (mA)	I_{DQ} (mA)	R_{BIAS} Current (mA)
604	82.83	80	2.93
802	75.98	75	2.68
1000	70.96	70	2.36
1210	66.95	65	2.05
1430	62.08	60	1.98
1800	57.13	55	1.73
2500	51.68	50	1.48
3010	43.74	45	1.24
3500	41.15	40	1.05
4990	35.35	35	0.85
6650	30.55	30	0.65
8450	27.37	25	0.47
18000	20.35	20	0.25

ASSEMBLY DIAGRAM

Figure 75 shows the assembly diagram of the HMC8412CHIPS.

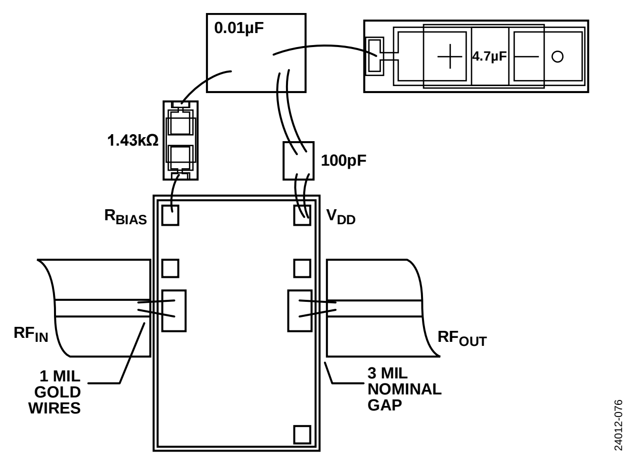

Figure 75. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETER WAVE GaAS MMICs

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section).

To bring RF to and from the HMC8412CHIPS, implement 50 Ω transmission lines using a microstrip or coplanar waveguide on 0.127 mm (5 mil) thick alumina, thin film substrates (see Figure 76). When using 0.254 mm (10 mil) thick alumina, raise the die to ensure that the die and substrate surfaces are coplanar. Raise the die 0.150 mm (6 mil) to ensure that the surface of the die is coplanar with the surface of the substrate. To make the die coplanar with the surface of the substrate, attach the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick, molybdenum (Mo) heat spreader (moly tab), which then attaches to the ground plane (see Figure 76 and Figure 77).

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

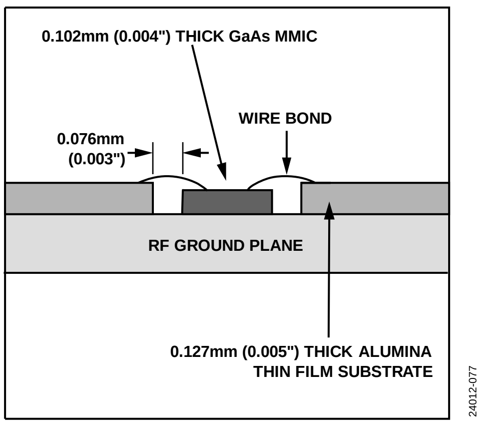

Figure 76. High Frequency Input Matching

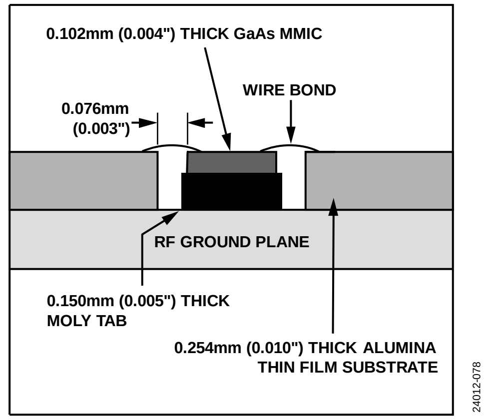

Figure 77. High Frequency Output Matching

HANDLING PRECAUTIONS

To avoid permanent damage to the die, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle-based or gel-based ESD protective containers, and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chip in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While applying bias, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers.

OUTLINE DIMENSIONS

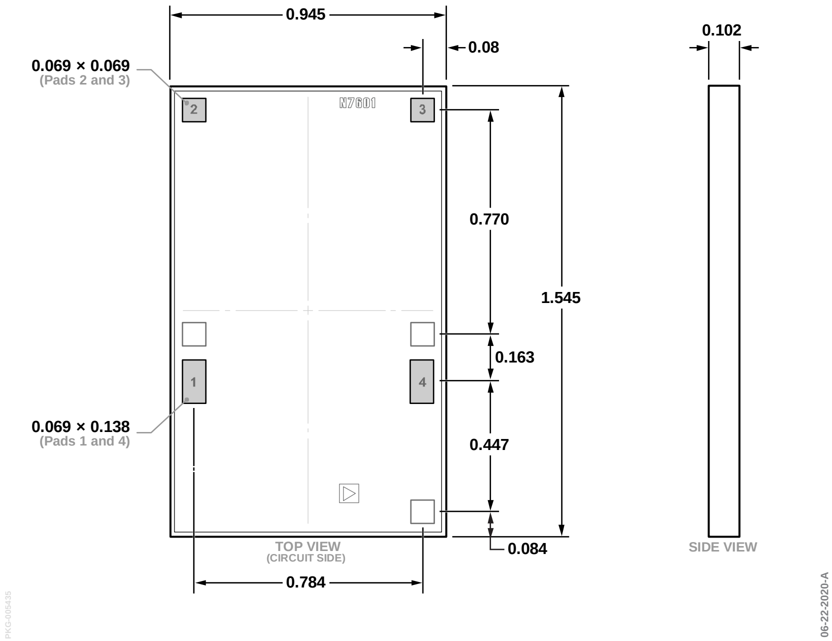

Figure 78. 4-Pad Bare Die [CHIP]
(C-4-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC8412CHIPS	−55°C to +85°C	4-Pad Bare Die [CHIP]	C-4-5
HMC8412CHIPS-SX	−55°C to +85°C	4-Pad Bare Die [CHIP]	C-4-5

[1] The HMC8412CHIPS and HMC8412CHIPS-SX are RoHS compliant parts.