HMC593LP3 / 593LP3E

v03.0309

GaAs PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.3 - 3.8 GHz

Typical Applications

The HMC593LP3(E) is ideal for:

- Wireless Infrastructure
- Fixed Wireless
- WiMAX WiBro / 4G
- Tower Mounted Amplifiers

Features

Noise Figure: 1.2 dB

Output IP3: +29 dBm

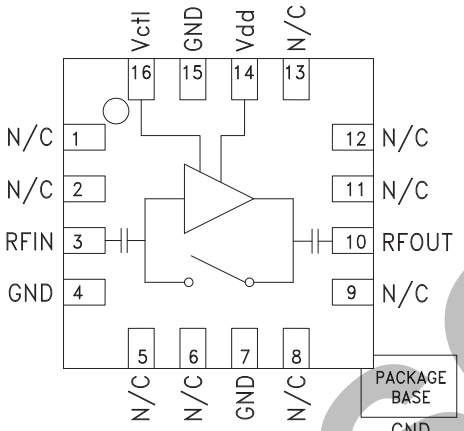
Gain: 19 dB

Low Loss LNA Bypass Path

Single Supply: +3V or +5V

50 Ohm Matched Output

Functional Diagram



General Description

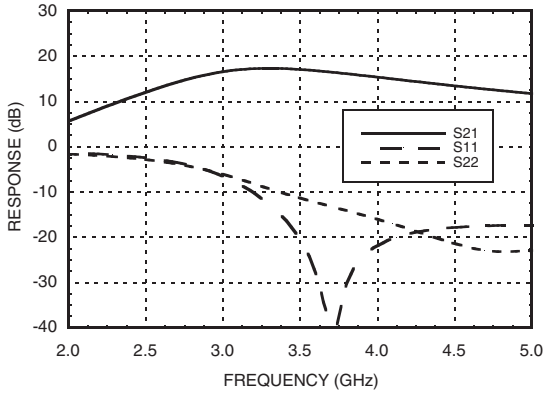
The HMC593LP3(E) is a versatile, high dynamic range GaAs MMIC Low Noise Amplifier that integrates a low loss LNA bypass mode on the IC. The amplifier is ideal for WiBro & WiMAX receivers operating between 3.3 and 3.8 GHz and provides 1.2 dB noise figure, 19 dB of gain and +29 dBm IP3 from a single supply of +5V @ 40mA. Input and output return losses are 23 and 13 dB respectively with no external matching components required. A single control line (0/Vdd) is used to switch between LNA mode and a low 2 dB loss bypass mode reducing the current consumption to 10 µA.

Electrical Specifications, T_A = +25° C

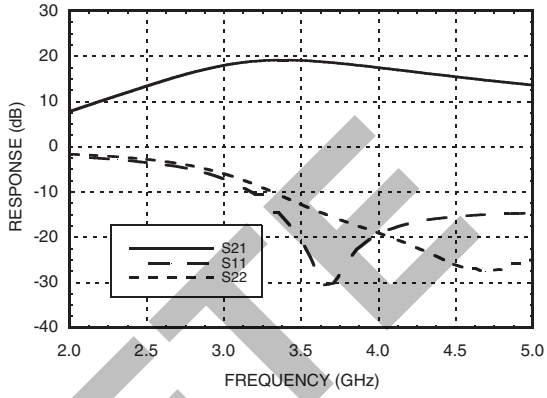
Parameter	Vdd = +3V						Vdd = +5V						Units
	LNA Mode			Bypass Mode			LNA Mode			Bypass Mode			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	3.3 - 3.8												GHz
Gain	14	17		-3	-2		16	19		-3	-2		dB
Gain Variation Over Temperature		0.011			0.002			0.011			0.002		dB / °C
Noise Figure		1.4	1.8					1.2	1.6				dB
Input Return Loss		23			30			23			30		dB
Output Return Loss		12			25			13			25		dB
Reverse Isolation		39						36					dB
Power for 1dB Compression (P1dB)*	10	13			30		13	16			30		dBm
Saturated Output Power (Psat)		13.5						17					dBm
Third Order Intercept (IP3)* (-20 dBm Input Power per tone, 1 MHz tone spacing)		22						29					dBm
Supply Current (Idd)		20	25		0.01			40	50		0.01		mA
Switching Speed: LNA Mode to Bypass Mode		428						428					ns
Switching Speed: Bypass Mode to LNA Mode					343						343		ns

* P1dB and IP3 for LNA Mode are referenced to RFOUT while P1dB for Bypass Mode is referenced to RFIN.

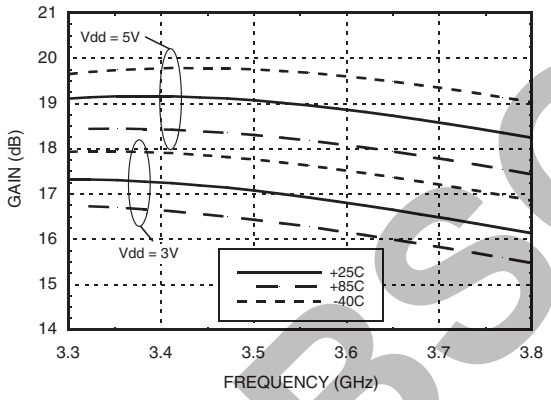
LNA Broadband Gain & Return Loss @ Vdd= 3V



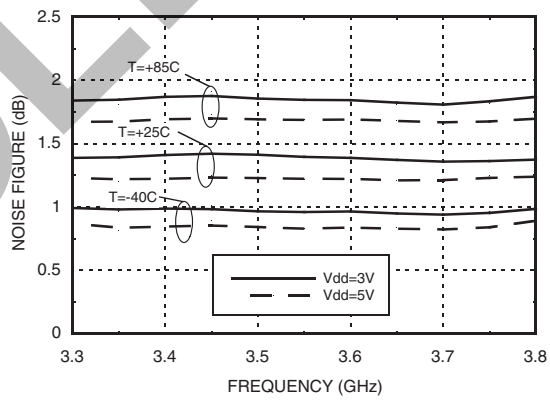
LNA Broadband Gain & Return Loss @ Vdd= 5V



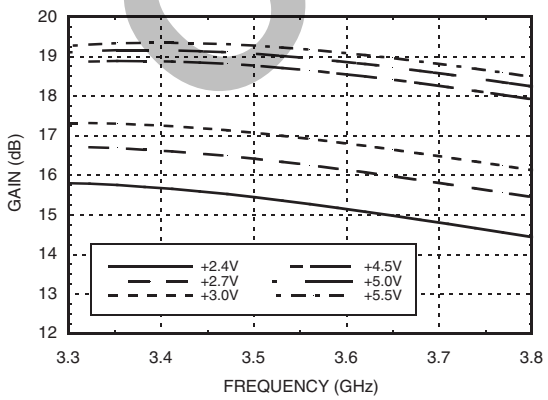
LNA Gain vs. Temperature



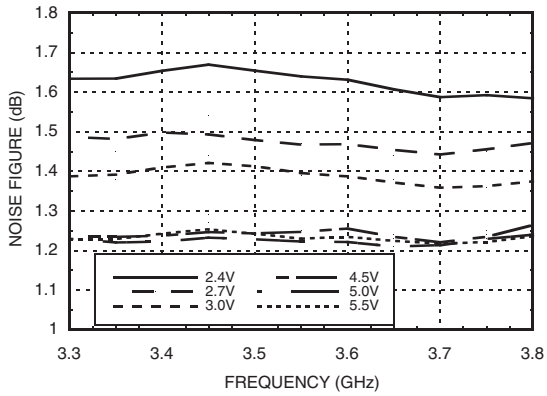
LNA Noise Figure vs. Temperature



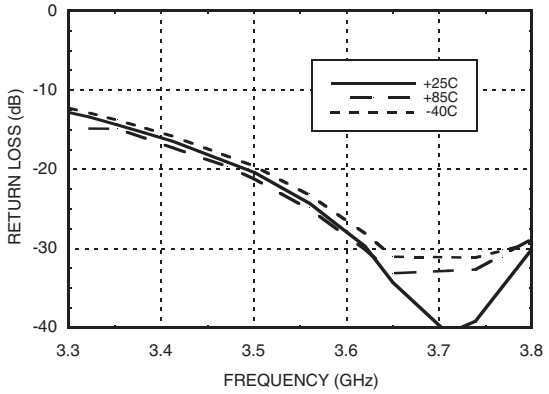
LNA Gain vs. Vdd



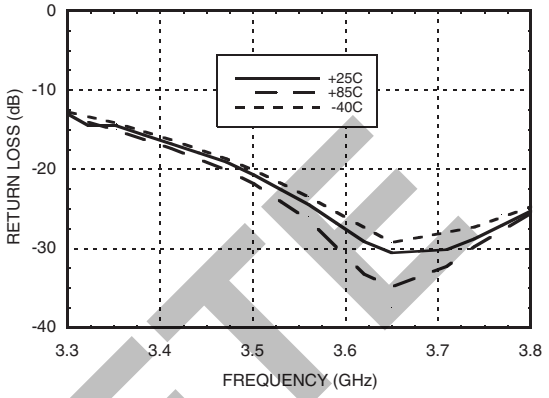
LNA Noise Figure vs. Vdd



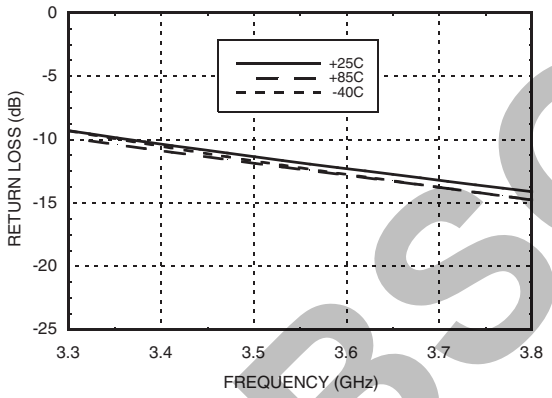
LNA Input Return Loss vs. Temperature @ Vdd= 3V



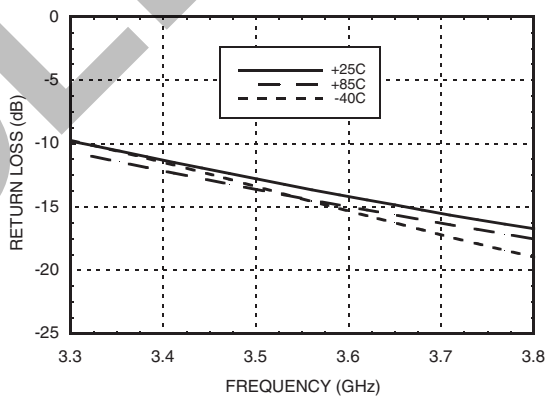
LNA Input Return Loss vs. Temperature @ Vdd= 5V



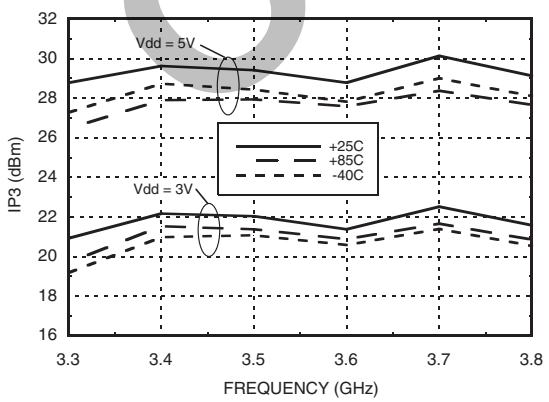
LNA Output Return Loss vs. Temperature @ Vdd= 3V



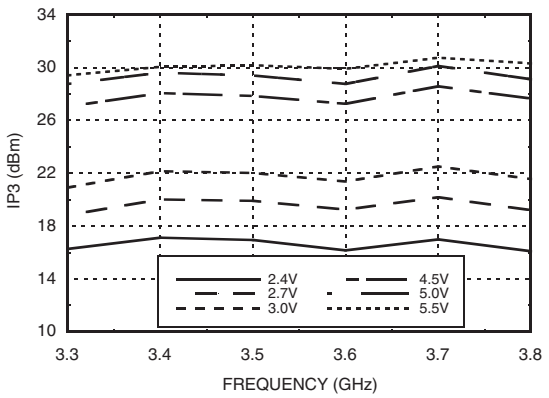
LNA Output Return Loss vs. Temperature @ Vdd= 5V



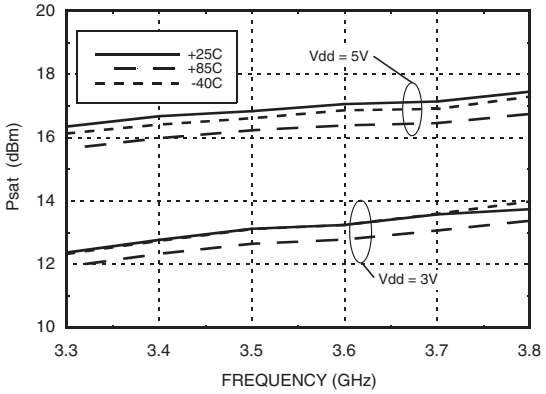
LNA Output IP3 vs. Temperature



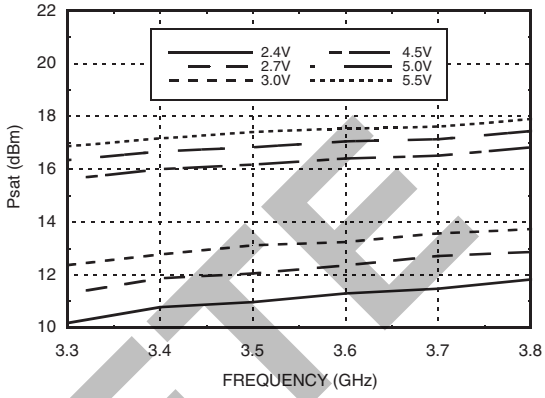
LNA Output IP3 vs. Vdd



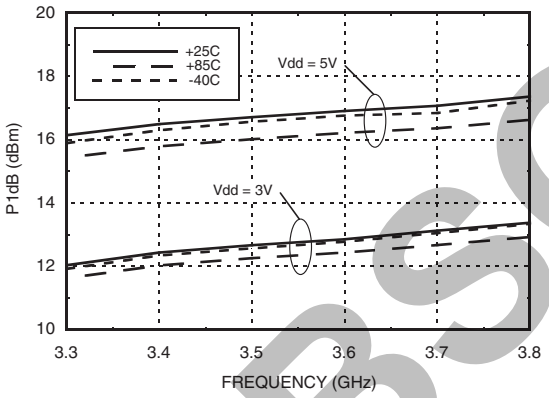
LNA Psat vs. Temperature



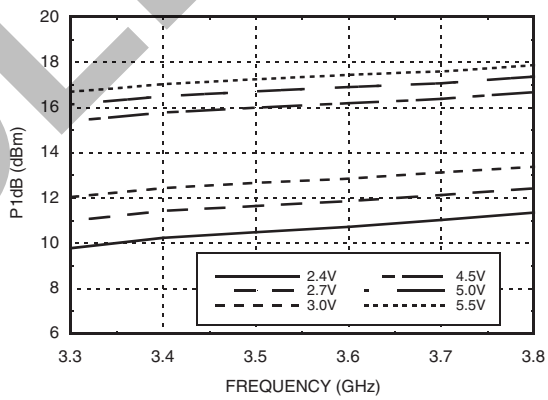
LNA Psat vs. Vdd



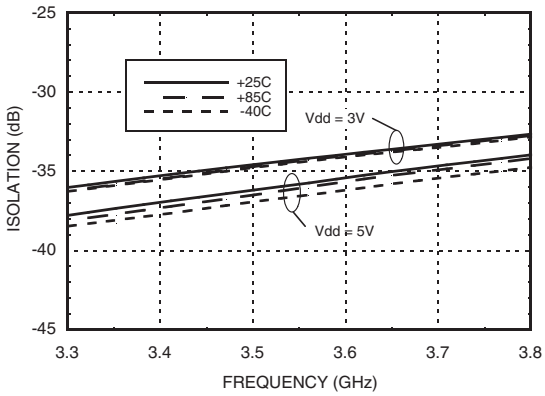
LNA Output P1dB vs. Temperature



LNA Output P1dB vs. Vdd

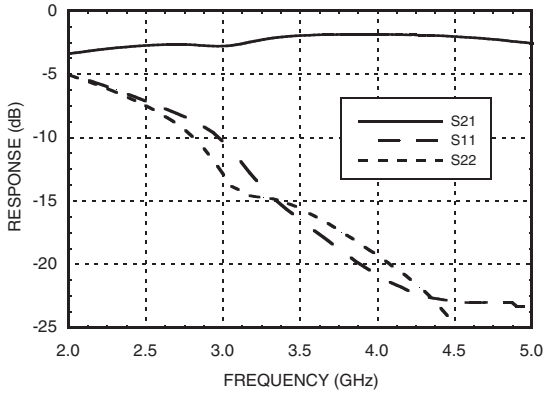


LNA Reverse Isolation vs. Temperature

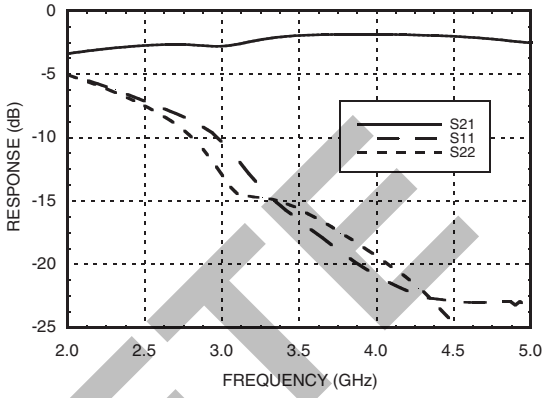


GaAs PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.3 - 3.8 GHz

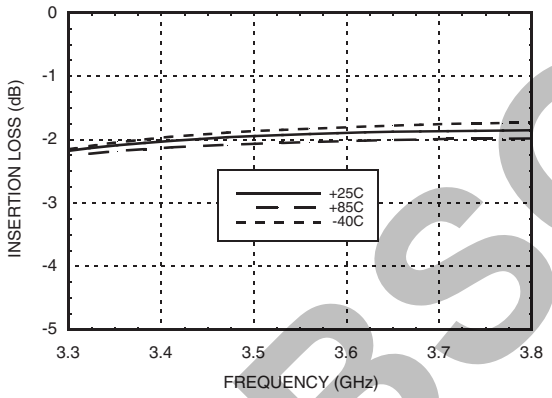
Bypass Mode Broadband Gain & Return Loss [1]



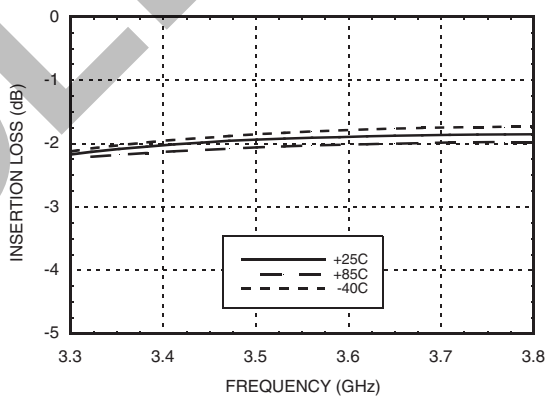
Bypass Mode Broadband Gain & Return Loss [2]



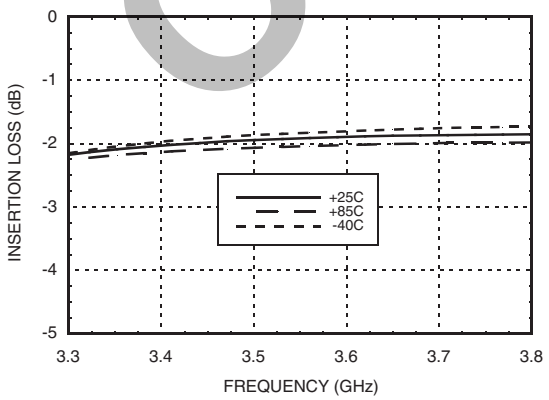
Bypass Mode Insertion Loss vs. Temperature [1]



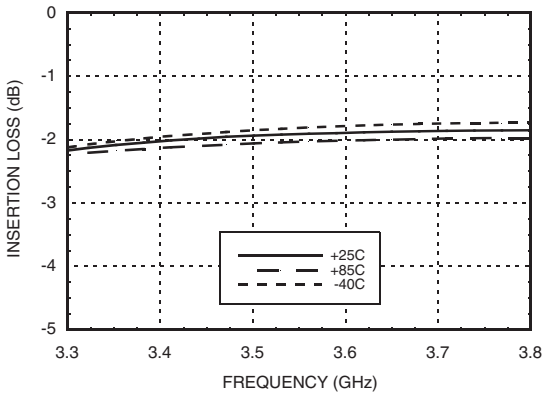
Bypass Mode Insertion Loss vs. Temperature [2]



Bypass Mode, Input IP3 vs. Temperature



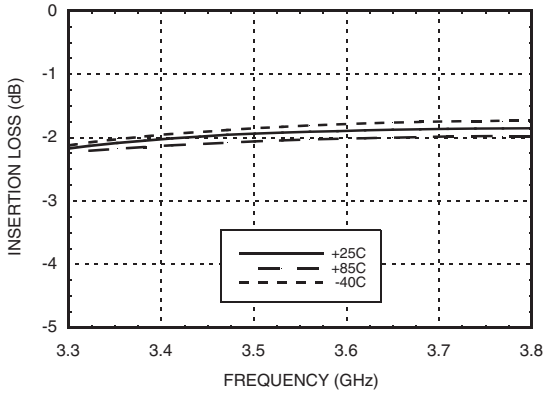
Bypass Mode, P1dB vs. Temperature



[1] Vdd = 3V [2] Vdd = 5V

GaAs PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.3 - 3.8 GHz

Bypass Mode, Psat vs. Temperature



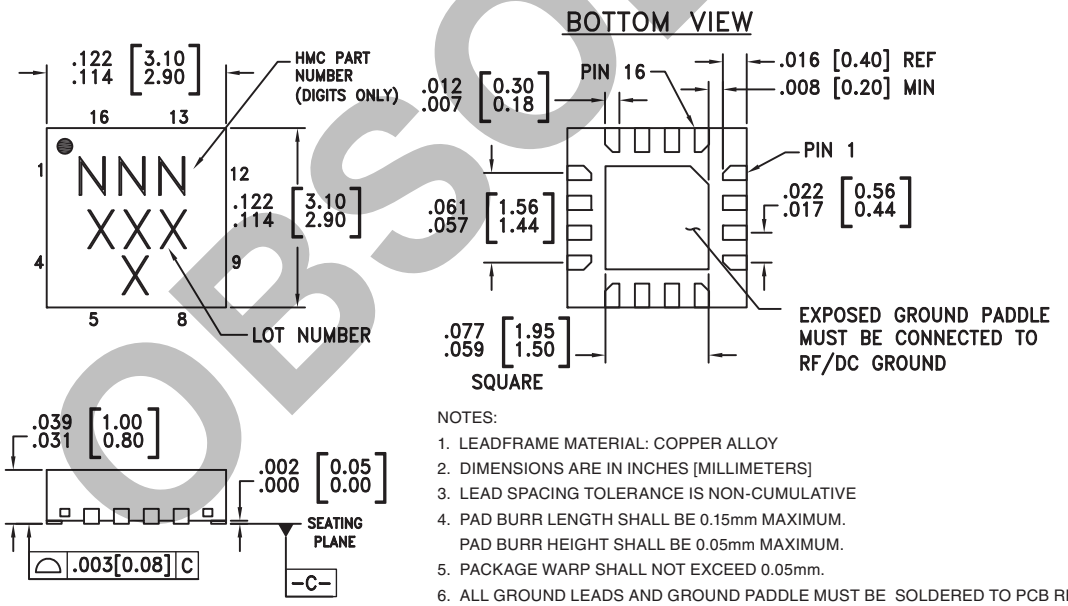
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+2.4	9
+2.7	12
+3.0	16
+4.5	33
+5.0	39
+5.5	44

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+8 V
RF Input Power (RFIN) (Vdd = +5.0 Vdc) LNA Mode / Bypass Mode	+15 dBm / +30 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 13 mW/°C above 85 °C)	850 mW
Thermal Resistance (channel to ground paddle)	76.9 °C/W
Storage Temperature	-65 to +150° C
Operating Temperature	-40 to +85° C
ESD Sensitivity (HBM)	Class 1A

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC593LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	593 XXXX
HMC593LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	593 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

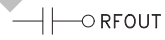
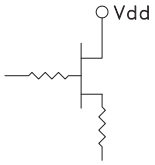
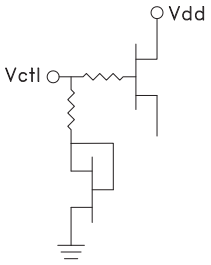
GaAs PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.3 - 3.8 GHz

Truth Table

LNA Mode	Vctl= Vdd
Bypass Mode	Vctl= 0V

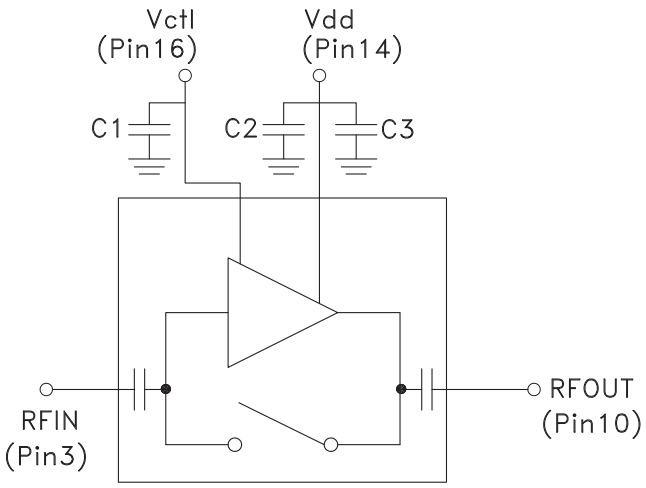
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Pin Descriptions

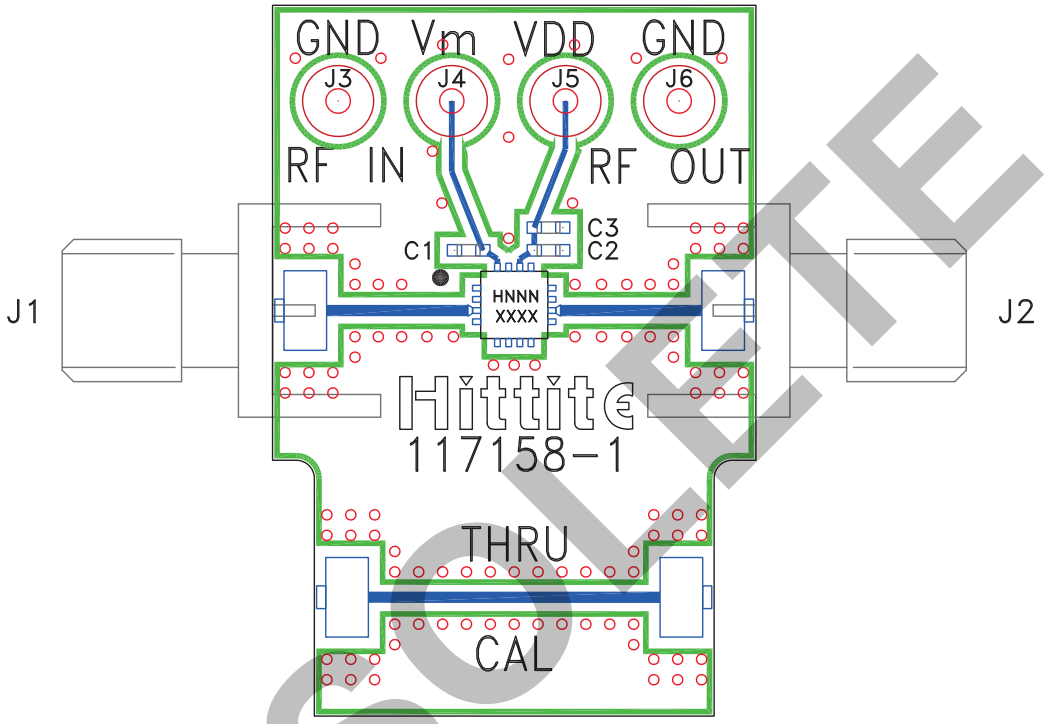
Pin Number	Function	Description	Interface Schematic
1, 2, 5, 6, 8, 9, 11 - 13	N/C	No connection necessary. These pins may be connected to RF/DC ground.	
3	RFIN	This pin is AC coupled and matched to 50 Ohms.	
4, 7, 15	GND	These pins must be connected to RF/DC ground.	
10	RFOUT	This pin is AC coupled and matched to 50 Ohms.	
14	Vdd	Power supply voltage. Bypass capacitors are required. See application circuit.	
16	Vctl	LNA/Bypass Mode Control Voltage. See truth table.	

Application Circuit

Component	Value
C1, C2	100pF
C3	10KpF



Evaluation PCB



List of Materials for Evaluation PCB 117160 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J6	DC Pin
C1, C2	100 pF Capacitor, 0402 Pkg.
C3	10 KpF Capacitor, 0402 Pkg.
U1	HMC593LP3 / HMC593LP3E Amplifier
PCB [2]	117158 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.