25 MBPS Quad-Channel Digital Isolator

ADuM7442S

1.0 Scope

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

This data specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at http://www.analog.com/ADuM7442

2.0 Part Number

The complete part number(s) of this specification follows:

Specific Part Number	Description
ADuM7442R703F	25 MBPS Quad-Channel Digital Isolator

3.0 Case Outline

The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline Letter	Descriptive Designator	Terminals	Lead Finish	Package style
X	CDFP4-F16	16 lead	Hot Solder Dip	Bottom Brazed Flat Pack

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

Package: X			
Pin Number	**Terminal Symbol**	**Pin Type**	**Pin Description**
1	VDD1A	Power	Supply Voltage A for Isolator Side 1. 1/, 2/
2	GND1	Power	Ground 1. Ground reference for Isolator Side 1. 3/, 6/
3	VIA	Digital Input	Logic Input A
4	VIB	Digital Input	Logic Input B
5	VOC	Digital Output	Logic Output C
6	VOD	Digital Output	Logic Output D
7	VDD1B	Power	Supply Voltage B for Isolator Side 1. 1/, 2/
8	GND1	Power	Ground 1. Ground reference for Isolator Side 1. 3/ 6/
9	GND2	Power	Ground 2. Ground reference for Isolator Side 2. 4/
10	VDD2B	Power	Supply Voltage B for Isolator Side 2. 2/, 5/
11	VID	Digital Input	Logic Input D.
12	VIC	Digital Input	Logic Input C.
13	VOB	Digital Output	Logic Output B.
14	VOA	Digital Output	Logic Output A.
15	GND2	Power	Ground 2. Ground reference for Isolator Side 2. 4/
16	VDD2A	Power	Supply Voltage A for Isolator Side 2. 2/, 5/
Lid		Power	Metal Lid electrically connected to ground. (GND1)

Figure 1 – Terminal Connections

1/ Pin 1 must be connected externally to Pin 7.
2/ Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between VDD1A (Pin 1) and GND1 (Pin 2), between VDD1B (Pin 7) and GND1 (Pin 8), between VDD2B (Pin 10) and GND2 (Pin 9), and between VDD2A (Pin 16) and GND2 (Pin 15)
3/ Pin 2 and Pin 8 are internally connected, and connecting both to GND1 is recommended.
4/ Pin 9 and Pin 15 are internally connected, and connecting both to GND2 is recommended.
5/ Pin 10 must be connected externally to Pin 16.
6/ Internally connected to Metal Lid.

4.0 Specifications

4.1. Absolute Maximum Ratings 1/

Supply voltage (V_{DD1} , V_{DD2}) ..... -0.5V to 7.0V
Input voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}) ..... -0.5V to V_{DDI} + 0.5V 2/ 3/
Output voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD}) ..... -0.5V to V_{DDO} + 0.5V 2/ 3/
Storage temperature range ..... -65°C to +150°C
Output current per pin (I_{O1}, I_{O2}) ..... -10mA to +10mA
Junction temperature maximum (T_J) ..... +150°C
Lead temperature (soldering, 60 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 60 °C/W 4/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 98 °C/W 4/

4.2. Recommended Operating Conditions

Supply voltage (V_{DDI}) ..... +3.3 V to +5.0 V
Ambient operating temperature range (T_A)..... -55°C to +125°C

4.3. Nominal Operating Performance Characteristics 5/

Jitter 2ns
Refresh Rate
V_{DD1}=V_{DD2} = 5V ..... 1.2 Mbps
V_{DD1}=V_{DD2} = 3.3V ..... 1.1 Mbps
V_{DD1}= 5V, V_{DD2} = 3.3V ..... 1.2 Mbps
V_{DD1}= 3.3V, V_{DD2} = 5.0V ..... 1.1 Mbps
Common Mode Transient Immunity |CM| .....15 kV/µs 6/
Capacitance (Input-to-Output) 10pF 7/
Input Capacitance 6pF 8/

Radiation Features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)….100 k rads(Si)

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
2/ VDDI and VDDO refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
3/ See Figure 2 for maximum rated current values for various temperatures.
4/ Measurement taken under absolute worst case condition and represent data taken with thermal camera for highest power density location. See MIL-STD-1835 for average Θ_{JC} number.
5/ All typical specifications are at TA = 25°C, VDD1 All typical specifications are at TA = 25°C, 3.6 V ≤ VDD1 ≤ 5. V, 3.3 V ≤ VDD2 ≤ 5.0 V, unless otherwise noted. Switching specifications are tested with CL = 15 pF and CMOS signal levels, unless otherwise noted.
6/ |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining VO > 0.8 VDD, VIx = VDDx, VCM = 200 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.
7/ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.
8/ Input capacitance is from any input data pin to ground.

TABLE IA – ELECTRICAL PERFORMANCE CHARACTERISTICS - 5V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate	DR	Within PWD Limit	9,10,11		25	Mbps
		M,D,P,L,R	9		25	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9,10,11	29	50	ns
		M,D,P,L,R	9	29	50	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	9,10,11		5	ns
		M,D,P,L,R	9		5	ns
Pulse Width	PW	Within PWD limit	9,10,11	40		ns
		M,D,P,L,R	9	40		ns
Propagation Delay Skew 2/, 3/, 4/	t_{PSK}		9,10,11		10	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11		30	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		4	ns
		M,D,P,L,R	9		4	ns
Channel Matching Opposing-Direction	t_{PSKOD}		9,10,11		6	ns
		M,D,P,L,R	9		6	ns
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4, 5		20	mA
			6		22	mA
		M,D,P,L,R	4		20	mA
	$I_{DD2(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4, 5		20	mA
			6		22	mA
		M,D,P,L,R	4		20	mA
Quiescent Supply Current	$I_{DD1(Q)}$		1,2,3		3.8	mA
		M,D,P,L,R	1		3.8	mA
	$I_{DD2(Q)}$		2		2.92	mA
			1,3		3.4	mA
		M,D,P,L,R	1		3.4	mA
DC CHARACTERISTICS						
Logic High Input Threshold	VIH	7/	1,2,3	0.7 V_{DDx}		V
		M,D,P,L,R	1	0.7 V_{DDx}		V
Logic low Input Threshold	VIL	7/	1,2,3		0.3 V_{DDx}	V
		M,D,P,L,R	1		0.3 V_{DDx}	V
Logic High Output Voltages	VOH	I_{Ox} = –20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} – 0.1		V
		M,D,P,L,R	1	V_{DDx} – 0.1		V
		I_{Ox} = –4 mA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} – 0.4		V
		M,D,P,L,R	1	V_{DDx} – 0.4		V
Logic Low Output Voltages	VOL	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.1	V
		M,D,P,L,R	1		0.1	V
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.4	V
		M,D,P,L,R	1		0.4	V
Input Leakage Current per Channel	I_{IH}	V_{Ix} = V_{DDx} 5/, 6/,7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA
	I_{IL}	V_{Ix} = 0V 5/, 6/,7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA
AC CHARACTERISTICS						
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	4		2.5	ns
			5		3	
			6		2	

TABLE IA NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, and T_A min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. V_{DDx} nom = 5 V, V_{DDx} max = 5.5V, V_{DDx} min = 4.5V

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

5/ V_{Ix} refer to the voltage input signals of a given channel (A, B, C, or D).

6/ I_{Ox} refer to the output current of a given channel (A, B, C, or D).

7/ V_{DDx} refers to the power supply on either side of a given channel (A, B, C, or D).

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS – 3.3V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate	DR	Within PWD Limit	9,10,11		25	Mbps
		M,D,P,L,R	9		25	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9,10,11	29	66	ns
		M,D,P,L,R	9	29	66	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - tP_{HL} \rvert$	9,11		5	ns
			10		9	
		M,D,P,L,R	9		5	ns
Pulse Width	PW	Within PWD limit	9,10,11	40		ns
		M,D,P,L,R	9	40		ns
Propagation Delay Skew 2/, 3/, 4/	t_{PSK}		9,10,11		10	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11		43	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		5	ns
		M,D,P,L,R	9		5	ns
Channel Matching Opposing-Direction	t_{PSKOD}		9,10,11		7	ns
		M,D,P,L,R	9		7	ns
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4		13	mA
			5,6		14	
		M,D,P,L,R	4		13	mA
	$I_{DD2(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4,5		13	mA
			6		15	
		M,D,P,L,R	4		13	mA
Quiescent Supply Current	$I_{DD1(Q)}$		1,2,3		2.4	mA
		M,D,P,L,R	1		2.4	mA
	$I_{DD2(Q)}$		1,2		2.3	mA
			3		2.4	mA
		M,D,P,L,R	1		2.3	mA
DC CHARACTERISTICS						
Logic High Input Threshold	VIH	7/	1,2,3	0.7 V_{DDx}		V
		M,D,P,L,R	1	0.7 V_{DDx}		V
Logic low Input Threshold	VIL	7/	1,2,3		0.3 V_{DDx}	V
		M,D,P,L,R	1		0.3 V_{DDx}	V
Logic High Output Voltages	VOH	I_{Ox} = –20 µA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} – 0.1		V
		M,D,P,L,R	1	V_{DDx} – 0.1		V
		I_{Ox} = –4 µA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} – 0.4		V
		M,D,P,L,R	1	V_{DDx} – 0.4		V
Logic Low Output Voltages	VOL	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.1	V
		M,D,P,L,R	1		0.1	V
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.4	V
		M,D,P,L,R	1		0.4	V
Input Leakage Current per Channel	I_{IH}	V_{Ix} = V_{DDx} 5/, 6/,7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA
	I_{IL}	V_{Ix} = 0V 5/, 6/,7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
AC CHARACTERISTICS						
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	4		3	ns
			5		4	
			6		2.5	

TABLE IB NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, and T_A min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. V_{DDx} nom = 3.3 V, V_{DDx} max = 3.6V, V_{DDx} min = 3V

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

5/ V_{Ix} refer to the voltage input signals of a given channel (A, B, C, or D).

6/ I_{Ox} refer to the output current of a given channel (A, B, C, or D).

7/ V_{DDx} refers to the power supply on either side of a given channel (A, B, C, or D).

TABLE IC – ELECTRICAL PERFORMANCE CHARACTERISTICS – MIXED 5 V/3.3 V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate	DR	Within PWD Limit	9,10,11		25	Mbps
		M,D,P,L,R	9		25	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9,11	30	55	ns
			10	30	57	
		M,D,P,L,R	9	30	55	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - tP_{HL} \rvert$	9,11		5	ns
			10		7	
		M,D,P,L,R	9		5	ns
Pulse Width	PW	Within PWD limit	9,10,11	40		ns
		M,D,P,L,R	9	40		ns
Propagation Delay Skew 2/, 3/, 4/	t_{PSK}		9,10,11		10	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11		40	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		5	ns
		M,D,P,L,R	9		5	ns
Channel Matching Opposing-Direction	t_{PSKOD}		9,10		9	ns
			11		12	ns
		M,D,P,L,R	9		9	ns
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4,5,6		20	mA
		M,D,P,L,R	4		20	mA
	$I_{DD2(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4,5		12	mA
			6		15	
		M,D,P,L,R	4		12	mA
Quiescent Supply Current	$I_{DD1(Q)}$		1,2,3		3.8	mA
		M,D,P,L,R	1		3.8	mA
	$I_{DD2(Q)}$		1,2		2.3	mA
			3		2.4	mA
		M,D,P,L,R	1		2.3	mA
DC CHARACTERISTICS						
Logic High Input Threshold	VIH	7/	1,2,3	0.7 V_{DDx}		V
		M,D,P,L,R	1	0.7 V_{DDx}		V
Logic low Input Threshold	VIL	7/	1,2,3		0.3 V_{DDx}	V
		M,D,P,L,R	1		0.3 V_{DDx}	V
Logic High Output Voltages	VOH	I_{Ox} = −20 µA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} − 0.1		V
		M,D,P,L,R	1	V_{DDx} − 0.1		V
		I_{Ox} = −4 µA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} − 0.4		V
		M,D,P,L,R	1	V_{DDx} − 0.4		V
Logic Low Output Voltages	VOL	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.1	V
		M,D,P,L,R	1		0.1	V
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.4	V
		M,D,P,L,R	1		0.4	V
Input Leakage Current per Channel	I_{IH}	V_{Ix} = V_{DDx} 5/, 6/,7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA
	I_{IL}	V_{Ix} = 0V 5/, 6/,7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
AC CHARACTERISTICS						
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	4		3	ns
			5		4	
			6		2.5	

TABLE IC NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, and T_A min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. V_{DD1} nom = 5 V, V_{DD1} max = 5.5V, V_{DD1} min = 4.5V / V_{DD2} nom = 3.3 V, V_{DD2} max = 3.6V, V_{DD2} min = 3V

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

5/ V_{Ix} refer to the voltage input signals of a given channel (A, B, C, or D).

6/ I_{Ox} refer to the output current of a given channel (A, B, C, or D).

7/ V_{DDx} refers to the power supply on either side of a given channel (A, B, C, or D).

TABLE ID – ELECTRICAL PERFORMANCE CHARACTERISTICS – MIXED 3.3 V/5 V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate	DR	Within PWD Limit	9,10,11		25	Mbps
		M,D,P,L,R	9		25	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9,10,11	31	60	ns
		M,D,P,L,R	9	31	60	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - tP_{HL} \rvert$	9, 11		5	ns
			10		7	
		M,D,P,L,R	9		5	ns
Pulse Width	PW	Within PWD limit	9,10,11	40		ns
		M,D,P,L,R	9	40		ns
Propagation Delay Skew 2/,3/,4/	t_{PSK}		9,10,11		10	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11		33	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		5	ns
		M,D,P,L,R	9		5	ns
Channel Matching Opposing-Direction	t_{PSKOD}		9,10,11		9	ns
		M,D,P,L,R	9		9	ns
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4,5		13	mA
			6		14.5	mA
		M,D,P,L,R	4		13	mA
	$I_{DD2(D)}$	F = 2MBPS, 10MBPS, 25MBPS	4,5		20	mA
			6		22	mA
		M,D,P,L,R	4		20	mA
Quiescent Supply Current	$I_{DD1(Q)}$		1,2,3		2.4	mA
		M,D,P,L,R	1		2.4	mA
	$I_{DD2(Q)}$		2		2.92	mA
			1,3		3.5	mA
		M,D,P,L,R	1		3.5	mA
DC CHARACTERISTICS						
Logic High Input Threshold	VIH	Z/	1,2,3	0.7 V_{DDx}		V
		M,D,P,L,R	1	0.7 V_{DDx}		V
Logic low Input Threshold	VIL	Z/	1,2,3		0.3 V_{DDx}	V
		M,D,P,L,R	1		0.3 V_{DDx}	V
Logic High Output Voltages	VOH	I_{Ox} = −20 µA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} – 0.1		V
		M,D,P,L,R	1	V_{DDx} – 0.1		V
		I_{Ox} = −4 µA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} – 0.4		V
		M,D,P,L,R	1	V_{DDx} – 0.4		V
Logic Low Output Voltages	VOL	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.1	V
		M,D,P,L,R	1		0.1	V
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.4	V
		M,D,P,L,R	1		0.4	V

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
Input Leakage Current per Channel	I_{IH}	$V_{Ix} = V_{DDx}$ 5/, 6/, 7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA
	I_{IL}	V_{Ix} = 0V 5/, 6/, 7/	1,2,3	-10	+10	µA
		M,D,P,L,R	1	-10	+10	µA
AC CHARACTERISTICS						
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	4		3.5	ns
			5		4.5	
			6		3	

TABLE ID NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, and T_A min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. V_{DD1} nom = 3.3 V, V_{DD1} max = 3.6V, V_{DD1} min = 3V / V_{DD2} nom = 5 V, V_{DD2} max = 5.5V, V_{DD2} min = 4.5V

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

5/ V_{Ix} refer to the voltage input signals of a given channel (A, B, C, or D).

6/ I_{Ox} refer to the output current of a given channel (A, B, C, or D).

7/ V_{DDx} refers to the power supply on either side of a given channel (A, B, C, or D).

TABLE IE – ELECTRICAL PERFORMANCE CHARACTERISTICS- INSULATION AND SAFETY-RELATED SPECIFICATIONS

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage 1/, 2/, 3/	Iso	200	Vpeak	1-minute duration
Maximum Continuous Working Voltage 1/, 2/, 3/	CWV	100	Vpeak	Continuous voltage magnitude imposed across the isolation barrier. AC Bipolar
Resistance (Input-to-Output) 4/	R_{I-O}	10^{12}	Ω	

TABLE IE NOTES:

1/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

2/ Parameter is not tested post irradiation

3/ Operation at this high voltage can lead to shortened isolation life. Continuous working voltage exceeding the rated value may cause permanent damage.

4/ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.

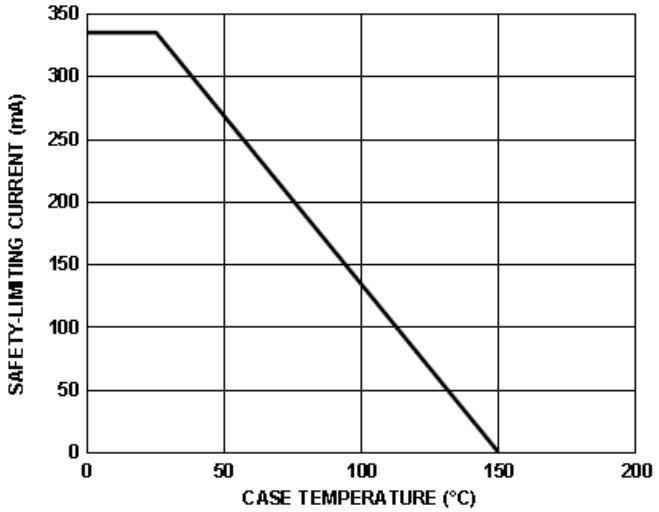

Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10
See note 3/ at the end of Section 4.0 Specifications

V_{Ix} Input[1/]	V_{DDI} State[2/]	V_{DDO} State[3/]	V_{Ox} Output[1/]	Description
H	Powered	Powered	H	Normal operation; data is high.
L	Powered	Powered	L	Normal operation; data is low.
X	Unpowered	Powered	H	Input unpowered. Outputs are in the default high state. Outputs return to input state within 1 µs of VDDI power restoration. See the pin function descriptions (Figure 1) for more details.
X	Powered	Unpowered	Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 µs of VDDO power restoration. See the pin function descriptions (Figure 1) for more details.

Figure 3 - Truth Table (Positive Logic)

1/ VIx and VOx refer to the input and output signals of a given channel (A, B, C, or D).
2/ VDDI refers to the power supply on the input side of a given channel (A, B, C, or D).
3/ VDDO refers to the power supply on the output side of a given channel (A, B, C, or D).

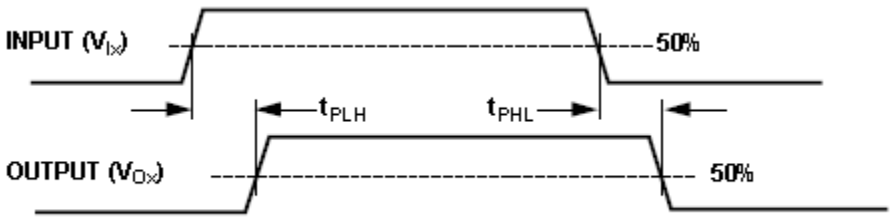

Figure 4. Propagation Delay Parameters

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	**Subgroups (in accordance with MIL-PRF-38535, Table III)**
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6, 9, 10, 11 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 4, 5, 6, 9, 10, 11 2/
Group D end-point electrical parameters	1, 2, 3, 4, 5, 6, 9, 10, 11
Group E end-point electrical parameters	1, 4, 9 3/

Table IIA Notes:
1/ PDA applies to Table I subgroup 1 and Table IIB delta parameters.
2/ See Table IIB for delta parameters
3/ Parameters noted in Table I are not tested post irradiation.

TABLE IIB – LIFE TEST/BURN-IN DELTA LIMITS (VDD1 = VDD2 = 3.0V and VDD1 = VDD2 = 5.5V, F=25MHz)

Table IIB			
Parameter	**Symbol**	**Delta**	**Units**
IDD1 Dynamic Supply Current VDD1=VDD2=5V, 25MBPS	$I_{DD1(D)}$	±1.0	mA
IDD2 Dynamic Supply Current VDD1=VDD2=5V, 25MBPS	$I_{DD2(D)}$	±0.5	mA
IDD1 Quiescent Supply Current VDD, VDD1=VDD2=5V	$I_{DD1(Q)}$	±0.2	mA
IDD2 Quiescent Supply Current VDD, VDD1=VDD2=5V	$I_{DD2(Q)}$	±0.1	mA
Input Current, VDD1=VDD2=5V, V_{Ix} = 0V	I_I	±0.5	µA
Input Current, VDD1=VDD2=5V, V_{Ix} = 5V	I_I	±0.5	µA
Logic High Output Voltages	VOH	±0.8	V
Logic Low Output Voltages	VOL	±7	mV

5.0 Burn-In Life Test, and Radiation

5.1. Burn-In Test Circuit, Life Test Circuit

5.1.1. The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition D of MIL –STD-883.

5.1.2. HTRB is not applicable for this drawing.

5.2. Radiation Exposure Circuit

5.2.1. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0 MIL-PRF-38535 QMLV Exceptions

6.1. Wafer Fabrication

Wafer fabrication occurs at MIL-PRF-38535 QML Class Q certified facility.

6.2. Wafer Lot Acceptance (WLA)

Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM inspection per MIL-STD-883 TM2018 is not applicable to the ADuM7442. The wafer fabrication process is manufactured using planarized metallization.

7.0 Application Notes

TYPICAL PERFORMANCE CHARACTERISTICS

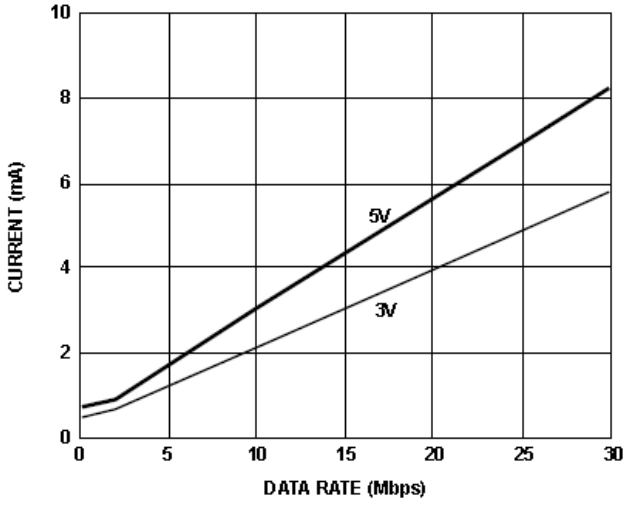

Figure 5. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

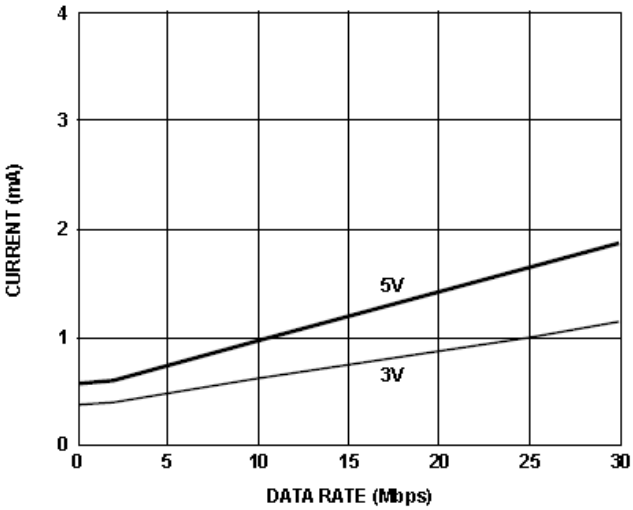

Figure 6. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

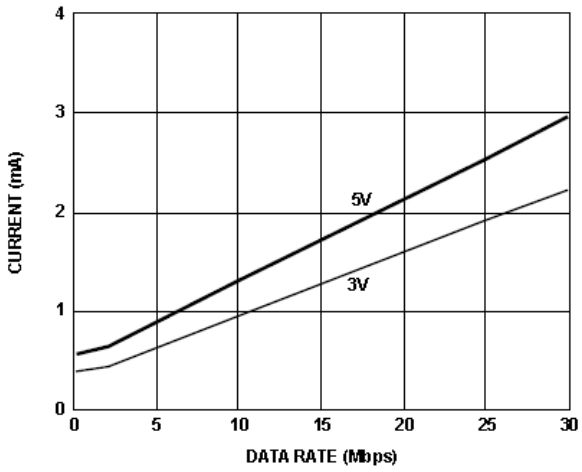

Figure 7. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

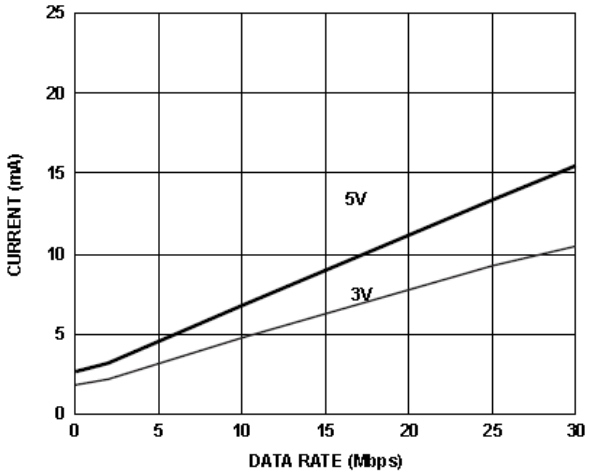

Figure 8. Typical ADuM7442 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

PC BOARD LAYOUT

The ADuM7442 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 9). A total of four bypass capacitors should be connected between Pin 1 and Pin 2 for V_{DD1A}, between Pin 7 and Pin 8 for V_{DD1B}, between Pin 9 and Pin 10 for V_{DD2B}, and between Pin 15 and Pin 16 for V_{DD2A}. Supply V_{DD1A} Pin 1 and V_{DD1B} Pin 7 should be connected together and supply V_{DD2B} Pin 10 and V_{DD2A} Pin 16 should be connected together. The capacitor values should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the power supply pin should not exceed 20 mm.

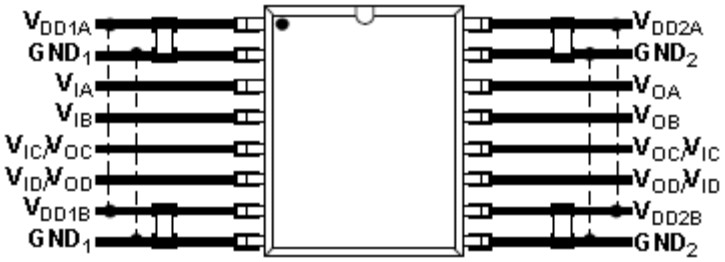

Figure 9. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, users should design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition. See Figure 4.

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM7442 component. Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM7442 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default high state by the watchdog timer circuit. The magnetic field immunity of the ADuM7442 is determined by the changing magnetic field, which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM7442 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta / dt) \sum \pi r_n^2; n = 1, 2, \ldots, N$$

where:

β is magnetic flux density (gauss).

rn is the radius of the nth turn in the receiving coil (cm).

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM7442 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 10.

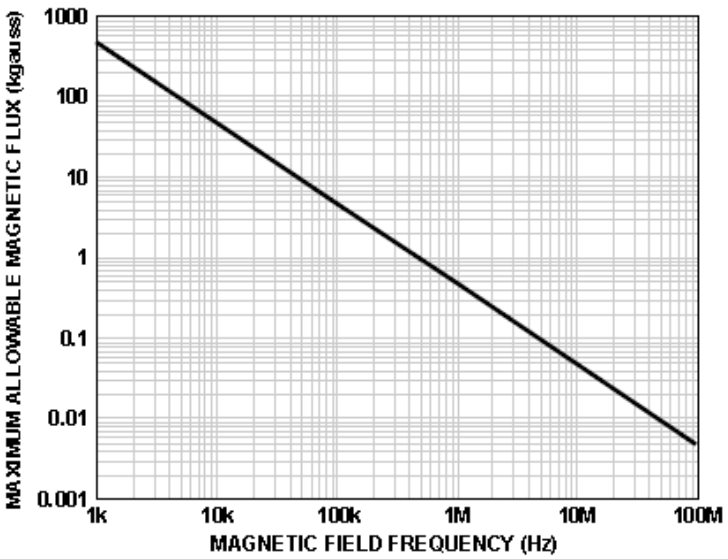

Figure 10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM7442 transformers. Figure 11 shows these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM7442 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted previously, a 1.2 kA current would have to be placed 5 mm away from the ADuM7442 to affect the operation of the component.

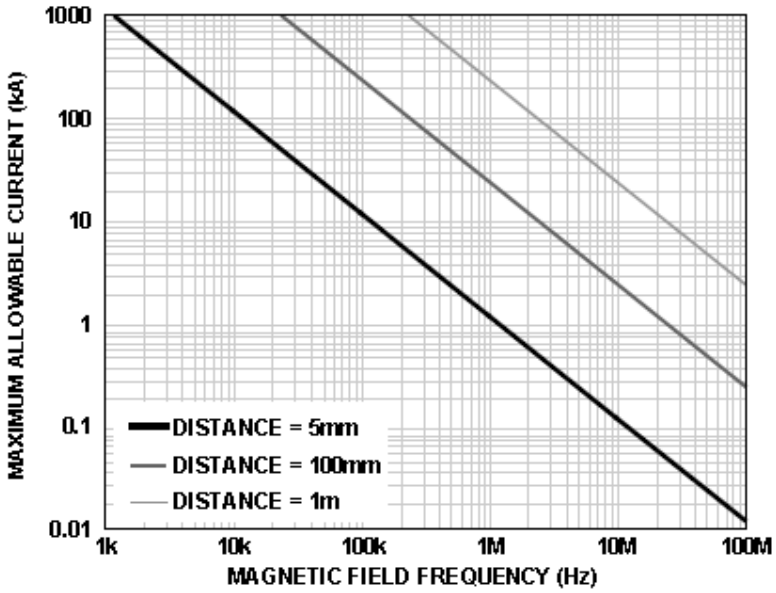

Figure 11. Maximum Allowable Current for Various Current-to-ADuM7442 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM7442 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$I_{DDI} = I_{DDI\,(Q)}$ $f \le 0.5\ f_r$

$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)}$ $f > 0.5\ f_r$

For each output channel, the supply current is given by

$I_{DDO} = I_{DDO\,(Q)}$ $f \le 0.5$ fr

$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10{-}3) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)}$ $f > 0.5$ fr

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.

f_r is the input stage refresh rate (Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel

corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 5 and Figure 6 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 7 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 8 show the total V_{DD1} and V_{DD2} supply current as a function of data rate for the ADuM7442.

8.0 Package Outline Dimensions

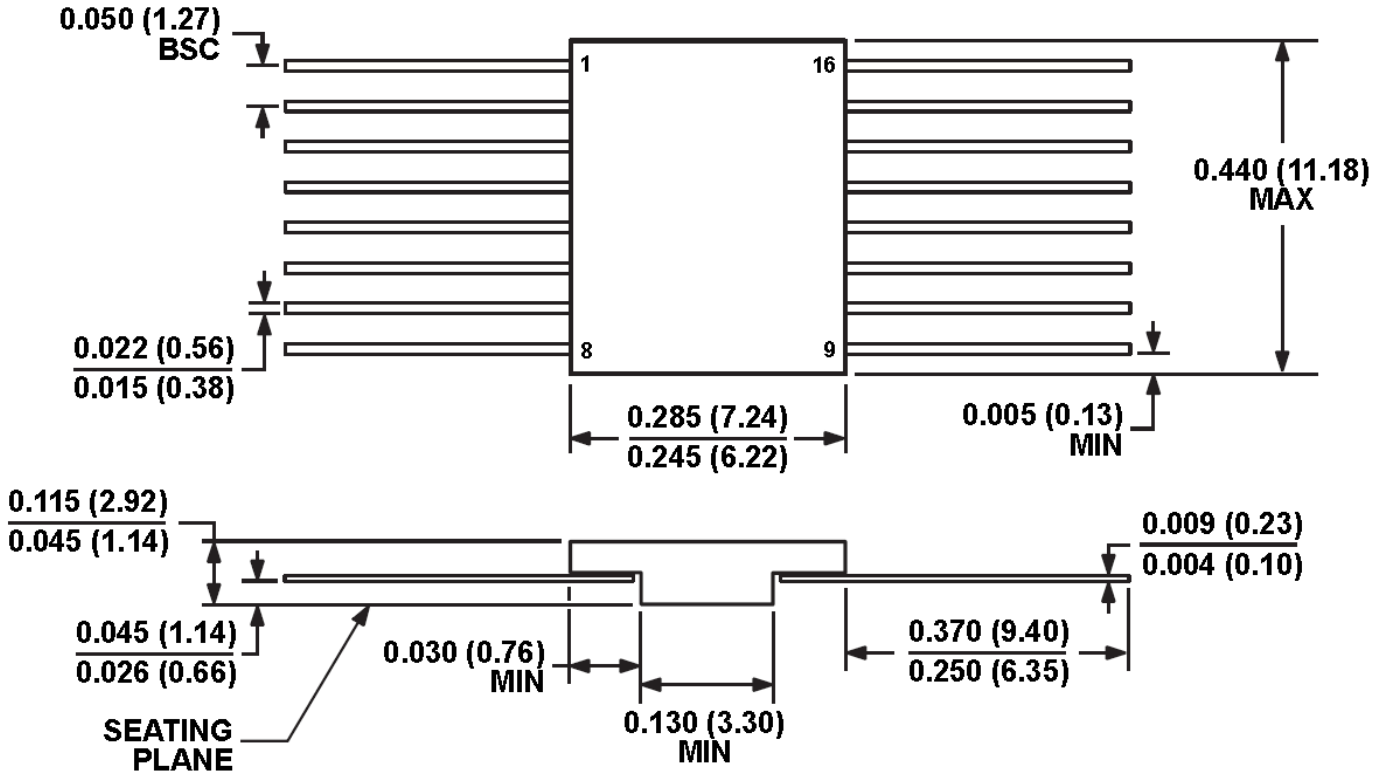

Figure 12. 16-Lead Bottom Brazed Flatpack
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuM7442R703F	−55°C to +125°C	16 Lead Bottom Brazed Flat Pack	CDFP4-F16

9.0 Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial Release	7/29/2016
B	Format compliance changes	8/10/2016
C	Add lead finish and specify terminal connection of metal lid	01/03/2018