Cyclone V Device Datasheet

2016.06.10

CV-51002

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for devices.

devices are offered in commercial and industrial grades. Commercial devices are offered in –C6 (fastest), –C7, and –C8 speed grades. Industrial grade devices are offered in the –I7 speed grade. Automotive devices are offered in the –A7 speed grade.

Related Information

Cyclone V Device Overview
Provides more information about the densities and packages of devices in the Cyclone V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of devices.

Operating Conditions

devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage tothe device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1: Absolute Maximum Ratings for Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.5	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO}	I/O power supply	–0.5	3.90	V
V_{CCA_FPLL}	Phase-locked loop (PLL) analog power supply	–0.5	3.25	V
V_{CCH_GXB}	Transceiver high voltage power	–0.5	3.25	V
V_{CCE_GXB}	Transceiver power	–0.5	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.5	1.50	V
V_I	DC input voltage	–0.5	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.5	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.5	3.90	V
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.5	3.25	V
$V_{CC\_AUX\_SHARED}$ (1)	HPS auxiliary power supply	–0.5	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

(1) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for SX C5, C6, D5, and D6 devices, and SE A5 and A6 devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 2: Maximum Allowed Overshoot During Transitions for Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for devices.

Recommended Operating Conditions

Table 3: Recommended Operating Conditions for Devices

This table lists the steady-state voltage values expected from devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum[2]	Typical	Maximum[2]	Unit
V_{CC}	Core voltage, periphery circuitry power supply, transceiver physical coding sublayer (PCS) power supply, and transceiver PCI Express® (PCIe®) hard IP digital power supply	Devices without internal scrubbing feature	1.07	1.1	1.13	V
		Devices with internal scrubbing feature (with SC suffix) [3]	1.12	1.15	1.18	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCPD}[4]	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

(2) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(3) The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local sales representatives.

(4) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Symbol	Description	Condition	Minimum[2]	Typical	Maximum[2]	Unit
V_{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CCA_FPLL}[5]	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCBAT}[6]	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	VCCIO	V

(2) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.
(5) PLL digital voltage is regulated from V_{CCA_FPLL}.
(6) If you do not use the design security feature in devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. power-on reset (POR) circuitry monitors V_{CCBAT}. devices do not exit POR if V_{CCBAT} is not powered up.

Symbol	Description	Condition	Minimum[2]	Typical	Maximum[2]	Unit
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
		Automotive	–40	—	125	°C
t_{RAMP}[7]	Power supply ramp time	Standard POR	200µs	—	100ms	—
		Fast POR	200µs	—	4ms	—

Transceiver Power Supply Operating Conditions

Table 4: Transceiver Power Supply Operating Conditions for GX, GT, SX, and ST Devices

Symbol	Description	Minimum[8]	Typical	Maximum[8]	Unit
V_{CCH_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V_{CCE_GXBL}[9][10]	Transmitter and receiver power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V
V_{CCL_GXBL}[9][10]	Clock network power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V

(2) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(7) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when `HPS_PORSEL` = 0 and t_{RAMP} specifications for fast POR when `HPS_PORSEL` = 1.

(8) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in GT and ST devices under this condition, refer to the Transceiver Protocol Configurations in Devices chapter.

(10) recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (GT and ST devices) and 6.144Gbps (GT and ST devices only). For more information about the maximum full duplex channels recommended in GT and ST devices for CPRI 6.144 Gbps, refer to the Transceiver Protocol Configurations in Devices chapter.

Related Information

- **PCIe Supported Configurations and Placement Guidelines**
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- **6.144-Gbps Support Capability in Cyclone V GT Devices**
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

HPS Power Supply Operating Conditions

Table 5: HPS Power Supply Operating Conditions for SX and ST Devices

This table lists the steady-state voltage and current values expected from system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Devices table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

Symbol	Description	Condition	Minimum(11)	Typical	Maximum(11)	Unit
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	—	1.07	1.1	1.13	V
V_{CCPD_HPS} (12)	HPS I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

(11) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(12) V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

Symbol	Description	Condition	Minimum[11]	Typical	Maximum[11]	Unit
V_{CCIO_HPS}	HPS I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V [13]	1.283	1.35	1.418	V
		1.2 V	1.14	1.2	1.26	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
$V_{CC\_AUX\_SHARED}$[14]	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 5
Provides the steady-state voltage values for the FPGA portion of the device.

[11] The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.
[13] V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.
[14] $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for SX C5, C6, D5, and D6 devices, and SE A5 and A6 devices.

DC Characteristics

Supply Current and Power Consumption

offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- **PowerPlay Early Power Estimator User Guide**
  Provides more information about power estimation tools.
- **PowerPlay Power Analysis chapter, Quartus Prime Handbook**
  Provides more information about power estimation tools.

I/O Pin Leakage Current

Table 6: I/O Pin Leakage Current for Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 7: Bus Hold Parameters for Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V <V_{IN} <V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 8: OCT Calibration Accuracy Specifications for Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–C6	–I7, –C7	–C8, –A7	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

OCT Without Calibration Resistance Tolerance Specifications

Table 9: OCT Without Calibration Resistance Tolerance Specifications for Devices

This table lists the OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	ResistanceTolerance			Unit
			–C6	–I7, –C7	–C8, –A7	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8, 1.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5	±25	±40	±40	%

Figure 1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 10: OCT Variation after Power-Up Calibration for Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of ±5% and a temperature range of 0°C to 85°C.

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Pin Capacitance

Table 11: Pin Capacitance for Devices

Symbol	Description	Maximum	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 12: Hot Socketing Specifications for Devices

Symbol	Description	Maximum	Unit
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300	µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8[15]	mA
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter (TX) pin	100	mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

(15) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Table 13: Internal Weak Pull-Up Resistor Values for Devices

Symbol	Description	Condition (V)[16]	Value[17]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Related Information

Cyclone V Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

(16) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(17) Valid with ±10% tolerances to cover changes over PVT.

Single-Ended I/O Standards

Table 14: Single-Ended I/O Standards for Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL}[18] (mA)	I_{OH}[18] (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

[18] To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	—	—	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 16: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[19] (mA)	I_{OH}[19] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8

(19) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[19] (mA)	I_{OH}[19] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO}+ 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Differential SSTL I/O Standards

Table 17: Differential SSTL I/O Standards for Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[20]	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})
SSTL-135	1.283	1.35	1.45	0.18	[20]	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})

[19] To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

[20] The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(20)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 18: Differential HSTL and HSUL I/O Standards for Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Differential I/O Standard Specifications

Table 19: Differential I/O Standard Specifications for Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for GX, GT, SX, and ST Devices table.														
2.5 V LVDS[24]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 700 Mbps	1.80	0.247	—	0.6	1.125	1.25	1.375
							1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS[25] [26]	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO)[27]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)[28]	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4

(21) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
(22) R_L range: $90 \leq R_L \leq 110\ \Omega$.
(23) This applies to default pre-emphasis setting only.
(24) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rate above 700 Mbps and 0.00 V to 1.85 V for data rate below 700 Mbps.
(25) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.
(26) For more information about BLVDS interface support in devices, refer to AN522: Implementing Bus LVDS Interface in Supported Device Families.
(27) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.
(28) For optimized mini-LVDS receiver performance, the receiver voltage input range must be within 0.300 V to 1.425 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL[29]	—	—	—	300	—	—	0.60	$D_{MAX} \leq$ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	$D_{MAX} >$ 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- **AN522: Implementing Bus LVDS Interface in Supported Altera Device Families**
  Provides more information about BLVDS interface support in Altera devices.
- **Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices** on page 24
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of core and periphery blocks.

[21] The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
[22] R_L range: $90 \leq R_L \leq 110\ \Omega$.
[23] This applies to default pre-emphasis setting only.
[29] For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Transceiver Performance Specifications

Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Table 20: Reference Clock Specifications for GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL[31], HCSL, and LVDS										
Input frequency from REFCLK input pins[32]	—	27	—	550	27	—	550	27	—	550	MHz
Rise time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz

(30) Transceiver Speed Grade 5 covers specifications for GT and ST devices.
(31) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(32) The reference clock frequency must be ≥ 307.2 MHz to be fully compliance to CPRI transmit jitter specification at 6.144 Gbps. For more information about CPRI 6.144 Gbps, refer to the Transceiver Protocol Configurations in Devices chapter.
(33) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	V_{CCE_GXBL} supply[34][35]			V_{CCE_GXBL} supply			V_{CCE_GXBL} supply			V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK phase noise[36]	10 Hz	—	—	–50	—	—	–50	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	—	—	–80	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	—	—	–110	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	—	—	–120	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	—	—	–120	—	—	–120	dBc/Hz
	≥1 MHz	—	—	–130	—	—	–130	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

(30) Transceiver Speed Grade 5 covers specifications for GT and ST devices.

(34) recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in GT and ST devices under this condition, refer to the Transceiver Protocol Configurations in Devices chapter.

(35) recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (GT and ST devices) and 6.144 Gbps (GT and ST devices only). For more information about the maximum full duplex channels recommended in GT and ST devices for CPRI 6.144 Gbps, refer to the Transceiver Protocol Configurations in Devices chapter.

(36) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12}.

Table 21: Transceiver Clocks Specifications for GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	100/ 125[37]	75	—	100/ 125[37]	75	—	100/ 125[37]	MHz

Table 22: Receiver Specifications for GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS										
Data rate[38]	—	614	—	5000/ 6144[35]	614	—	3125	614	—	2500	Mbps
Absolute V_{MAX} for a receiver pin[39]	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V

(37) The maximum supported clock frequency is 100 MHz if the PCIe hard IP block is enabled or 125 MHz if the PCIe hard IP block is not enabled.
(38) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
(39) The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins[40]	—	110	—	—	110	—	—	110	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
V_{ICM} (AC coupled)	2.5 V PCML, LVPECL, and LVDS	V_{CCE_GXBL} supply[34][35]			V_{CCE_GXBL} supply			V_{CCE_GXBL} supply			V
	1.5 V PCML	0.65[41]/0.8									V
t_{LTR}[42]	—	—	—	10	—	—	10	—	—	10	µs
t_{LTD}[43]	—	—	—	4	—	—	4	—	—	4	µs
t_{LTD_manual}[44]	—	—	—	4	—	—	4	—	—	4	µs

(40) The differential eye opening specification at the receiver input pins assumes that you have disabled the Receiver Equalization feature. If you enable the Receiver Equalization feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(41) The AC coupled V_{ICM} is 650 mV for PCIe mode only.

(42) t_{LTR} is the time required for the receive clock data recovery (CDR) to lock to the input reference clock frequency after coming out of reset.

(43) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(44) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{LTR\_LTD\_manual}$[45]	—	15	—	—	15	—	—	15	—	—	µs
Programmable ppm detector[46]	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000									ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3 [47] DC gain setting = 0 to 1	Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for GX, GT, SX, and ST Devices diagrams.									dB

Table 23: Transmitter Specifications for GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML										
Data rate	—	614	—	5000/ 6144[35]	614	—	3125	614	—	2500	Mbps
V_{OCM} (AC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω

(45) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.
(46) The rate matcher supports only up to ±300 parts per million (ppm).
(47) The software allows AC gain setting = 3 for design with data rate between 614 Mbps and 1.25 Gbps only.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	TX V_{CM} = 0.65 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	—	—	180	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew	×*N* PMA bonded mode	—	—	500	—	—	500	—	—	500	ps

Table 24: CMU PLL Specifications for GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported data range	—	614	—	5000/ 6144[35]	614	—	3125	614	—	2500	Mbps
fPLL supported data range	—	614	—	3125	614	—	3125	614	—	2500	Mbps

Table 25: Transceiver-FPGA Fabric Interface Specifications for GX, GT, SX, and ST Devices

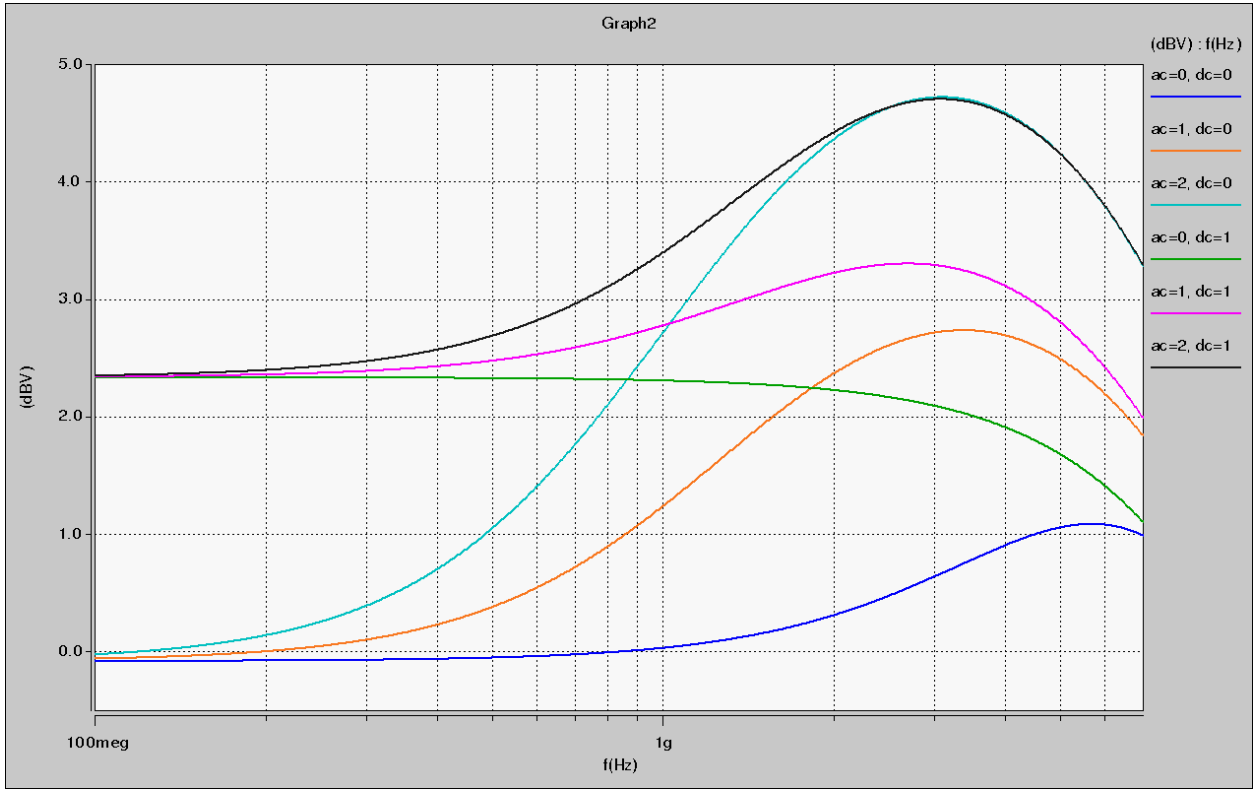
Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Interface speed (single-width mode)	—	25	—	187.5	25	—	187.5	25	—	163.84	MHz
Interface speed (double-width mode)	—	25	—	163.84	25	—	163.84	25	—	156.25	MHz

Related Information

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 31
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 32
- **PCIe Supported Configurations and Placement Guidelines**
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- **6.144-Gbps Support Capability in Cyclone V GT Devices**
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

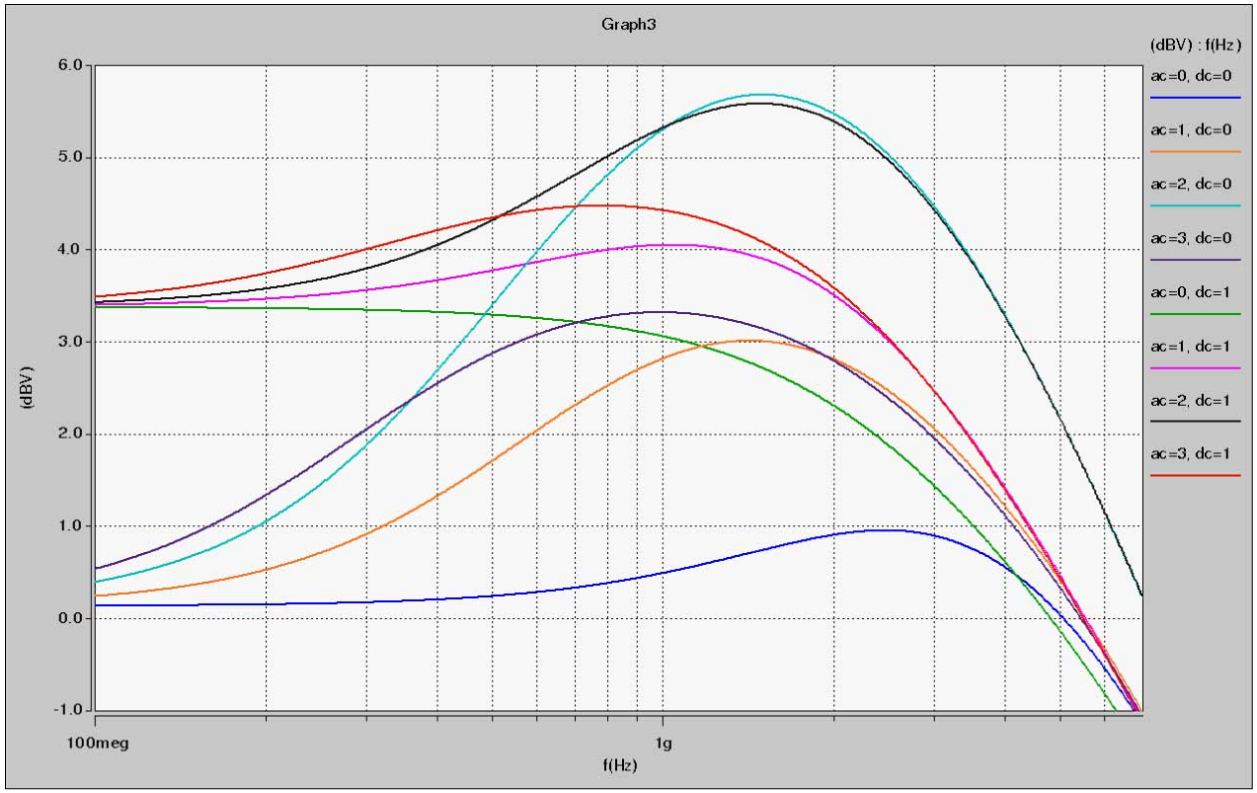
CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for GX, GT, SX, and ST Devices



CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for GX, GT, SX, and ST Devices



Typical TX V_{OD} Setting for Transceiver Channels with termination of 100 Ω

Table 26: Typical TX V_{OD} Setting for Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting[48]	V_{OD} Value (mV)	V_{OD} Setting[48]	V_{OD} Value (mV)
V_{OD} differential peak-to-peak typical	6[49]	120	34	680
	7[49]	140	35	700
	8[49]	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

[48] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Symbol	V_{OD} Setting[48]	V_{OD} Value (mV)	V_{OD} Setting[48]	V_{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

(48) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.
(49) Only valid for data rates ≤ 5 Gbps.

Exception for PCIe Gen2 design:

- V_{OD} setting = 50 and pre-emphasis setting = 22 are allowed for PCIe Gen2 design with transmit de-emphasis –6dB setting (`pipe_txdeemp` = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.
- V_{OD} setting = 50 and pre-emphasis setting = 12 are allowed for PCIe Gen2 design with transmit de-emphasis –3.5dB setting (`pipe_txdeemp` = 1'b1) using Altera PCIe Hard IP and PIPE IP cores.

For example, when V_{OD} = 800 mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the HSSI HSPICE models.

Table 27: Transmitter Pre-Emphasis Levels for Devices

1st Post Tap Pre-Emphasis Setting	V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB

1st Post Tap Pre-Emphasis Setting	V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices

Provides the Cyclone V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Sales Representative.

Table 28: Transceiver Compliance Specification for All Supported Protocol for GX, GT, SX, and ST Devices

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2(50)	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000

(50) For PCIe Gen2 sub-protocol, recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for GT and ST FPGA systems which ensure full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in GT and ST devices under this condition, refer to the Transceiver Protocol Configurations in Devices chapter.

Protocol	Sub-protocol	Data Rate (Mbps)
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII(51)	4,915.2
	CPRI E60LVII(51)	6,144
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970
VbyOne	VbyOne 3750	3,750

(51) For CPRI E48LVII and E60LVII, recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (GT and ST devices) and 6.144 Gbps (GT and ST devices only). For more information about the maximum full duplex channels recommended in GT and ST devices for CPRI 6.144 Gbps, refer to the Transceiver Protocol Configurations in Devices chapter.

Protocol	Sub-protocol	Data Rate (Mbps)
HiGig+	HIGIG 3750	3,750

Related Information

- **PCIe Supported Configurations and Placement Guidelines**
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- **6.144-Gbps Support Capability in Cyclone V GT Devices**
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

Core Performance Specifications

Clock Tree Specifications

Table 29: Clock Tree Specifications for Devices

Parameter	Performance			Unit
	–C6	–C7, –I7	–C8, –A7	
Global clock and Regional clock	550	550	460	MHz
Peripheral clock	155	155	155	MHz

PLL Specifications

Table 30: PLL Specifications for Devices

This table lists the PLL block specifications. PLL block does not include HPS PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–C6 speed grade	5	—	670[52]	MHz
		–C7, –I7 speed grades	5	—	622[52]	MHz
		–C8, –A7 speed grades	5	—	500[52]	MHz
f_{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	—	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	—	50	—	160	MHz
f_{VCO}[53]	PLL voltage-controlled oscillator (VCO) operating range	–C6, –C7, –I7 speed grades	600	—	1600	MHz
		–C8, –A7 speed grades	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	–C6, –C7, –I7 speed grades	—	—	550[54]	MHz
		–C8, –A7 speed grades	—	—	460[54]	MHz

(52) This specification is limited in the software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(53) The VCO frequency reported by the software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
(54) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OUT_EXT}	Output frequency for external clock output	–C6, –C7, –I7 speed grades	—	—	667[54]	MHz
		–C8, –A7 speed grades	—	—	533[54]	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High[55]	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ}[56][57]	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.15	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	±750	ps (p-p)

(55) High bandwidth PLL settings are not supported in external feedback mode.
(56) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.
(57) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTPJ_DC}[58]	Period jitter for dedicated clock output in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	300	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	30	mUI (p-p)
t_{FOUTPJ_DC}[58]	Period jitter for dedicated clock output in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	425[61], 300[59]	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	42.5[61], 30[59]	mUI (p-p)
t_{OUTCCJ_DC}[58]	Cycle-to-cycle jitter for dedicated clock output in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	300	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	30	mUI (p-p)
$t_{FOUTCCJ\_DC}$[58]	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	425[61], 300[59]	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	42.5[61], 30[59]	mUI (p-p)
t_{OUTPJ_IO}[58][60]	Period jitter for clock output on a regular I/O in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	650	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	65	mUI (p-p)
t_{FOUTPJ_IO}[58][60][61]	Period jitter for clock output on a regular I/O in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	650	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	65	mUI (p-p)
t_{OUTCCJ_IO}[58][60]	Cycle-to-cycle jitter for clock output on regular I/O in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	650	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	65	mUI (p-p)
$t_{FOUTCCJ\_IO}$[58][60][61]	Cycle-to-cycle jitter for clock output on regular I/O in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	650	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	65	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$[58][62]	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	300	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	30	mUI (p-p)

(58) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Devices table.

(59) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

(60) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Devices table.

(61) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	Bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 50
Provides more information about the external memory interface clock output jitter specifications.

(62) The cascaded PLL specification is only applicable with the following conditions:

- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

DSP Block Performance Specifications

Table 31: DSP Block Performance Specifications for Devices

Mode		Performance			Unit
		–C6	–C7, –I7	–C8, –A7	
Modes using One DSP Block	Independent 9 × 9 multiplication	340	300	260	MHz
	Independent 18 × 19 multiplication	287	250	200	MHz
	Independent 18 × 18 multiplication	287	250	200	MHz
	Independent 27 × 27 multiplication	250	200	160	MHz
	Independent 18 × 25 multiplication	310	250	200	MHz
	Independent 20 × 24 multiplication	310	250	200	MHz
	Two 18 × 19 multiplier adder mode	310	250	200	MHz
	18 × 18 multiplier added summed with 36-bit input	310	250	200	MHz
Modes using Two DSP Blocks	Complex 18 × 19 multiplication	310	250	200	MHz

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 32: Memory Block Performance Specifications for Devices

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–C6	–C7, –I7	–C8, –A7	
MLAB	Single port, all supported widths	0	1	420	350	300	MHz
	Simple dual-port, all supported widths	0	1	420	350	300	MHz
	Simple dual-port with read and write at the same address	0	1	340	290	240	MHz
	ROM, all supported width	0	1	420	350	300	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 33: High-Speed I/O Specifications for Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	437.5	5	—	420	5	—	320	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	320	5	—	320	5	—	275	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	840	(65)	—	740	(65)	—	640	Mbps

(63) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

(64) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(65) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol	Condition	–C6			–C7, –I7			–C8, –A7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks- f_{HSDR} (data rate) (67)	SERDES factor J = 4 to 10	(65)	—	640	(65)	—	640	(65)	—	550	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	(65)	—	170	(65)	—	170	(65)	—	170	Mbps
$t_{x\ Jitter}$ -True Differential I/O Standards(67)	Total Jitterfor Data Rate, 600 Mbps – 840 Mbps	—	—	350	—	—	380	—	—	500	ps
	Total Jitter for Data Rate < 600Mbps	—	—	0.21	—	—	0.23	—	—	0.30	UI
$t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Networks	Total Jitter for Data Rate < 640Mbps	—	—	500	—	—	500	—	—	500	ps

(66) The maximum ideal data rate is the SERDES factor (J) × PLL max output frequency (f_{out}), provided you can close the design timing and the signal integrity simulation is clean. You can estimate the achievable maximum data rate by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(67) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

Symbol	Condition	–C6			–C7, –I7			–C8, –A7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network	Total Jitter for Data Rate < 640Mbps	—	—	0.15	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} and t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	300	—	—	300	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
Receiver	f_{HSDR} (data rate)	SERDES factor J =4 to 10[64]	[65]	—	875[67]	[65]	—	840[67]	[65]	—	640[67]	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	[65]	—	[66]	[65]	—	[66]	[65]	—	[66]	Mbps
Sampling Window		—	—	—	350	—	—	350	—	—	350	ps

DLL Frequency Range Specifications

Table 34: DLL Frequency Range Specifications for Devices

Parameter	–C6	–C7, –I7	–C8	Unit
DLL operating frequency range	167 – 400	167 – 400	167 – 333	MHz

DQS Logic Block Specifications

Table 35: DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–C6	–C7, –I7	–C8	Unit
2	40	80	80	ps

Memory Output Clock Jitter Specifications

Table 36: Memory Output Clock Jitter Specifications for Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

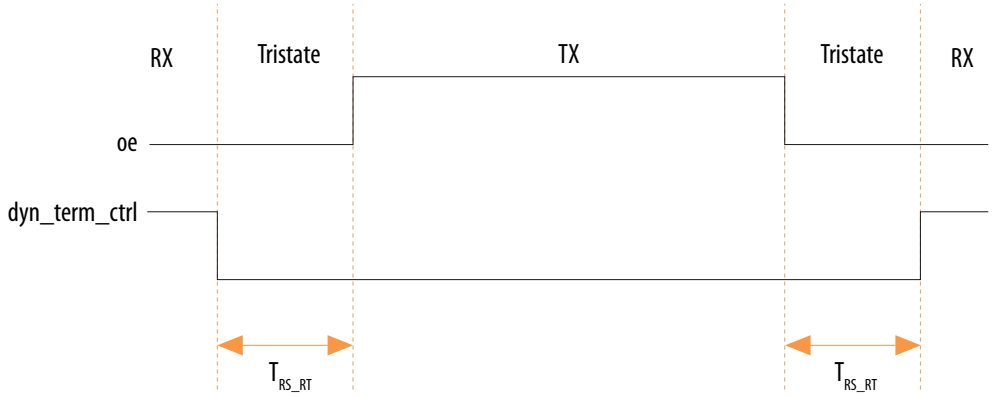
Parameter	Clock Network	Symbol	–C6		–C7, –I7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	–60	60	–70	70	–70	70	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	—	90	—	100	—	100	ps

OCT Calibration Block Specifications

Table 37: OCT Calibration Block Specifications for Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 4: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 38: Worst-Case DCD on I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	–C6		–C7, –I7		–C8, –A7		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

HPS Specifications

This section provides HPS specifications and timing for devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

HPS Clock Performance

Table 39: HPS Clock Performance for Devices

Symbol/Description	–C6	–C7, –I7	–A7	–C8	Unit
mpu_base_clk (microprocessor unit clock)	925	800	700	600	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	350	300	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	160	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 40: HPS PLL VCO Frequency Range for Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C7, –I7, –A7, –C8	320	1,600	MHz
	–C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 41: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

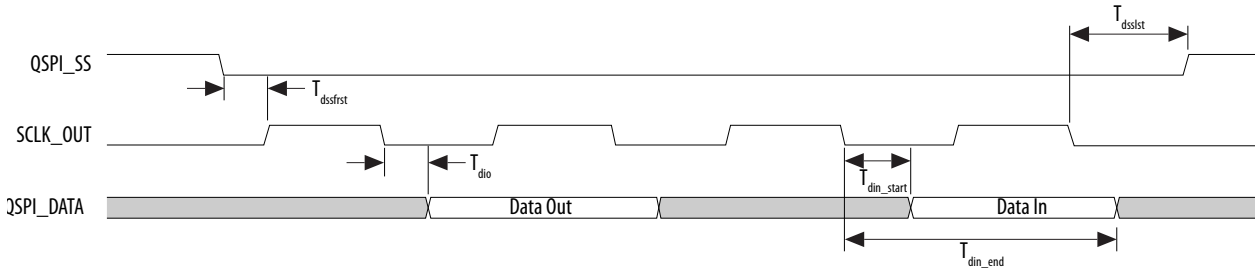
Table 42: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (68)	ns
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (68)	—	—	ns

(68) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the Quad SPI Flash Controller chapter in the Hard Processor System Technical Reference Manual.

Figure 5: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

Quad SPI Flash Controller Chapter, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about Rdelay.

SPI Timing Characteristics

Table 43: SPI Master Timing Requirements for Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 (69)	—	ns
T_{h}	SPI MISO hold time	1	—	ns
$T_{dutycycle}$	SPI_CLK duty cycle	45	55	%
$T_{dssfrst}$	Output delay SPI_SS valid before first clock edge	8	—	ns

(69) This value is based on `rx_sample_dly` = 1 and `spi_m_clk` = 120 MHz. `spi_m_clk` is the internal clock that is used by SPI Master to derive it's `SCLK_OUT`. These timings are based on `rx_sample_dly` of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct `rx_sample_dly` value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about `rx_sample_delay`, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

Symbol	Description	Min	Max	Unit
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	ns
T_{dio}	Master-out slave-in (MOSI) output delay	–1	1	ns

Figure 6: SPI Master Timing Diagram

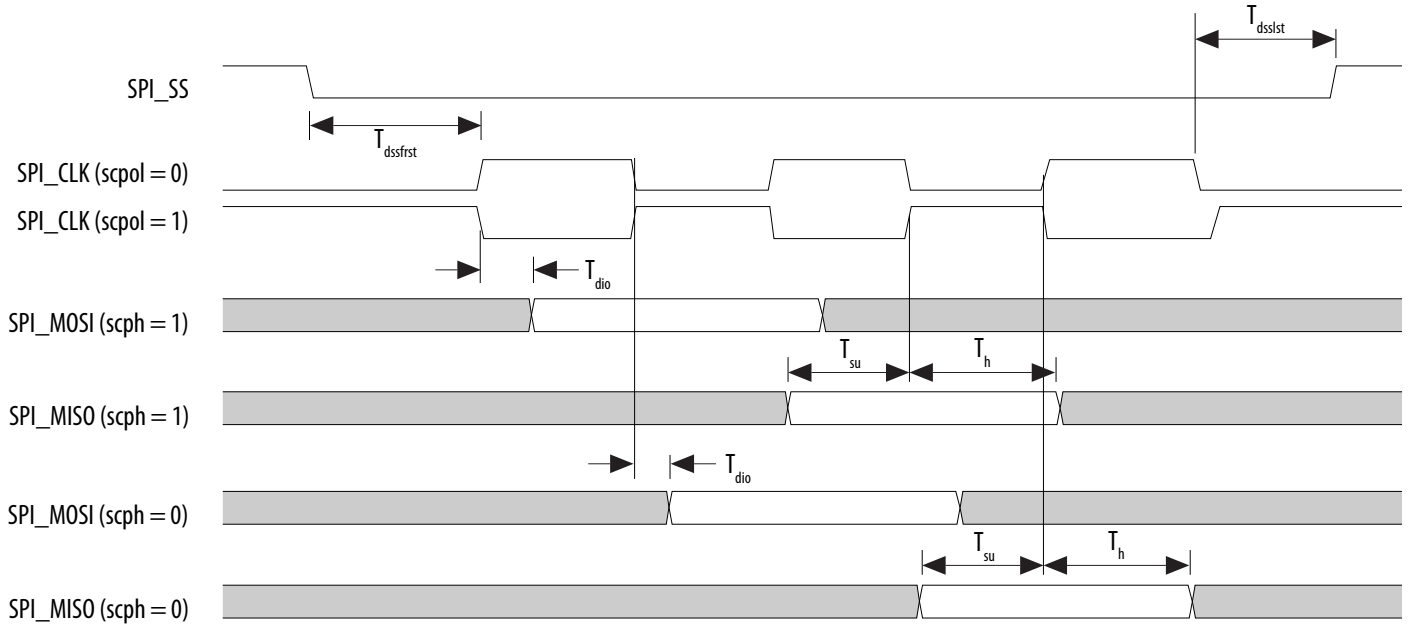


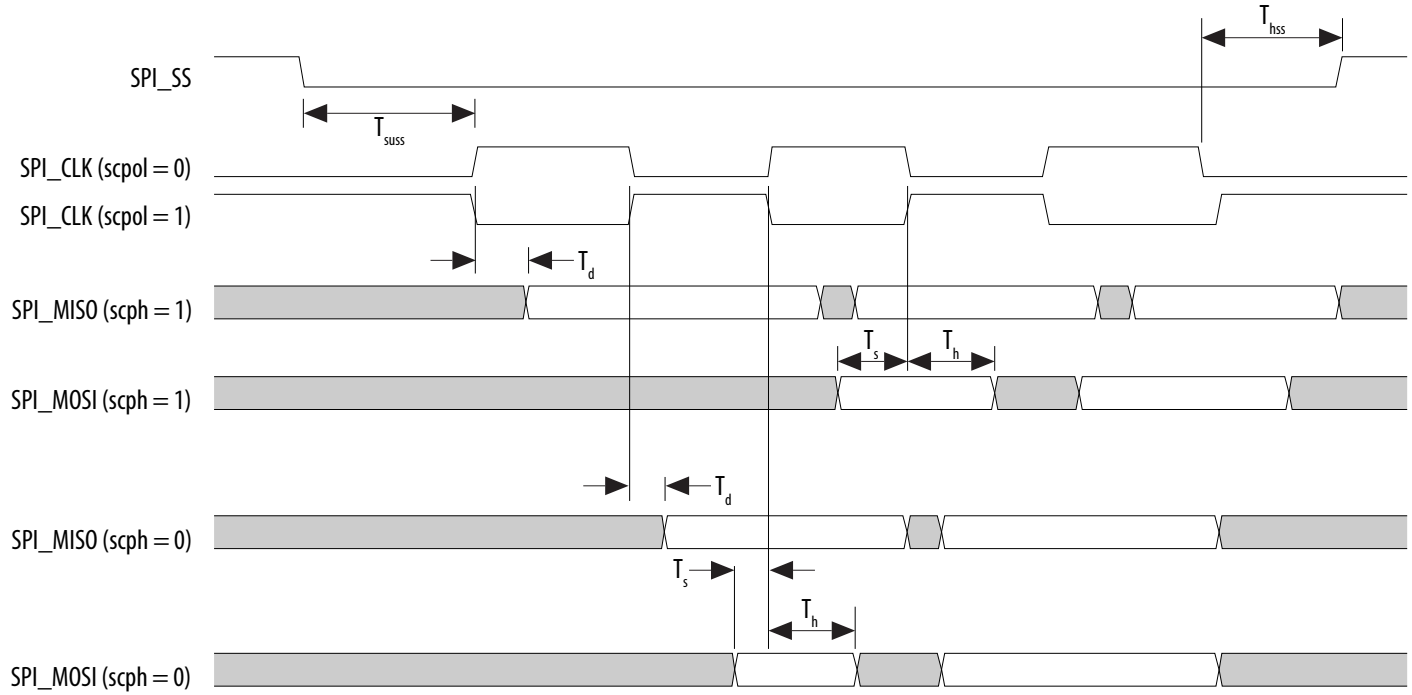
Table 44: SPI Slave Timing Requirements for Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns

Symbol	Description	Min	Max	Unit
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	MISO output delay	—	6	ns

Figure 7: SPI Slave Timing Diagram



Related Information

SPI Controller, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 45: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Devices

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smplsel` via the system manager. `drvsel` can be set from 1 to 7 and `smplsel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

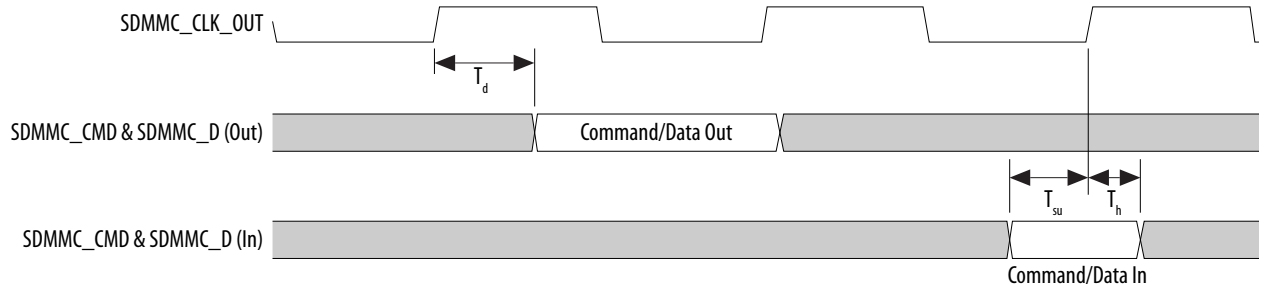
The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Max	Unit
T_{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{sdmmc\_clk\_out}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	(T_{sdmmc_clk} × `drvsel`)/2 − 1.23 (70)	(T_{sdmmc_clk} × `drvsel`)/2 + 1.69 (70)	ns

(70) `drvsel` is the drive clock phase shift select value.

Symbol	Description	Min	Max	Unit
T_{su}	Input setup time	1.05 – (T_{sdmmc_clk} × smplsel)/2 (71)	—	ns
T_h	Input hold time	(T_{sdmmc_clk} × smplsel)/2 (71)	—	ns

Figure 8: SD/MMC Timing Diagram



Related Information

Booting and Configuration Chapter, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

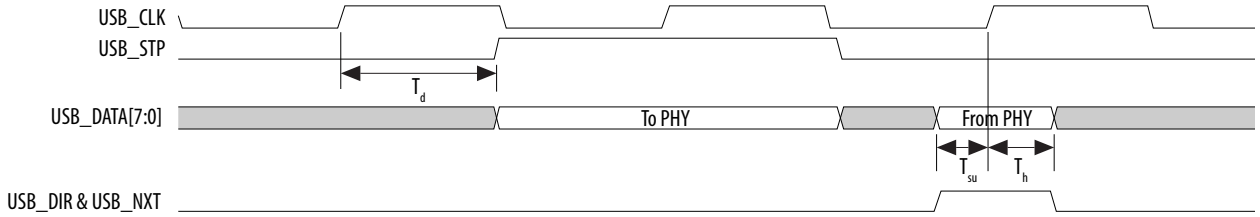
Table 46: USB Timing Requirements for Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns

(71) smplsel is the sample clock phase shift select value.

Symbol	Description	Min	Typ	Max	Unit
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 9: USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 47: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	–0.85	—	0.15	ns

Figure 10: RGMII TX Timing Diagram

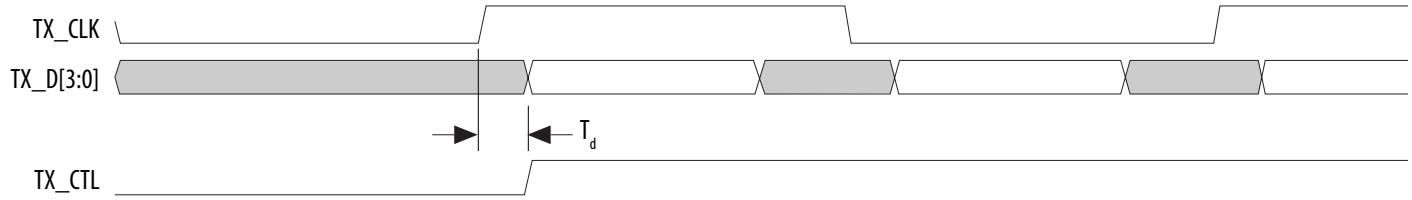


Table 48: RGMII RX Timing Requirements for Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_h	RX_D/RX_CTL hold time	1	—	ns

Figure 11: RGMII RX Timing Diagram

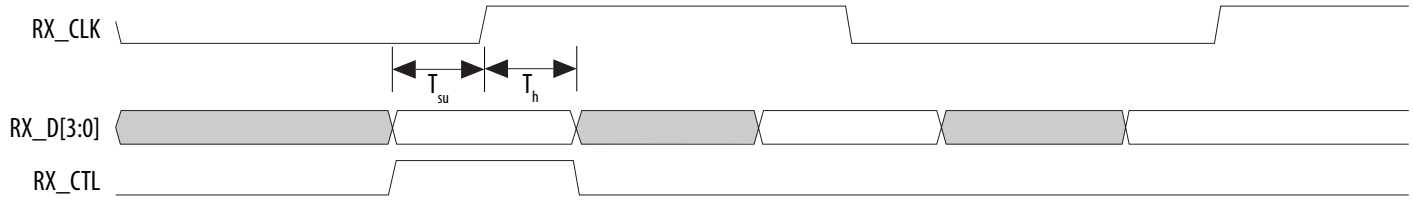
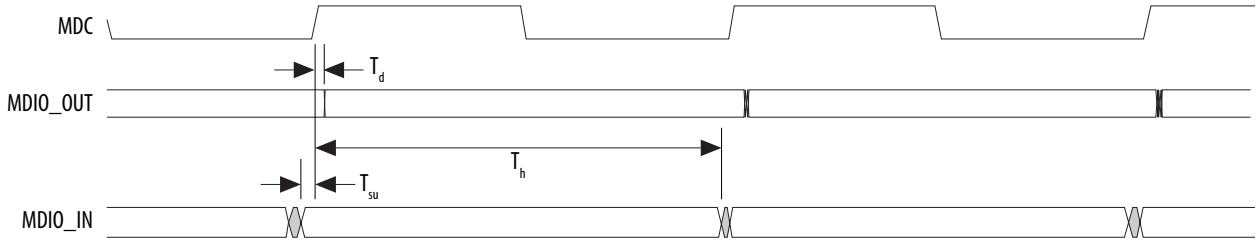


Table 49: Management Data Input/Output (MDIO) Timing Requirements for Devices

Symbol	Description	Min	Typ	Unit
T_{clk}	MDC clock period	—	400	ns
T_d	MDC to MDIO output data delay	10	—	ns

Symbol	Description	Min	Typ	Unit
T_s	Setup time for MDIO data	10	—	ns
T_h	Hold time for MDIO data	0	—	ns

Figure 12: MDIO Timing Diagram

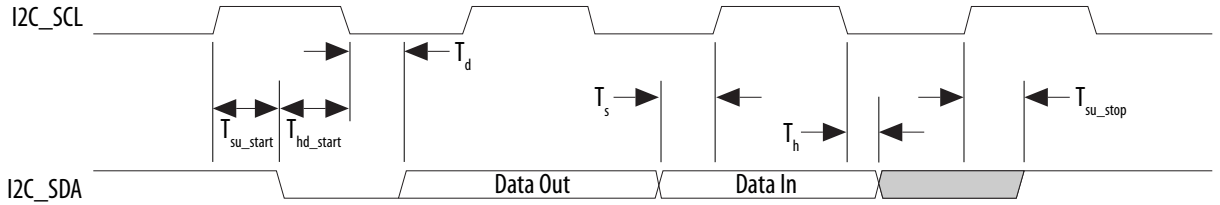


I²C Timing Characteristics

Table 50: I²C Timing Requirements for Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Figure 13: I²C Timing Diagram



NAND Timing Characteristics

Table 51: NAND ONFI 1.0 Timing Requirements for Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the `C4` output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T_{wp} (72)	Write enable pulse width	10	—	ns
T_{wh} (72)	Write enable hold time	7	—	ns
T_{rp} (72)	Read enable pulse width	10	—	ns
T_{reh} (72)	Read enable hold time	7	—	ns
T_{clesu} (72)	Command latch enable to write enable setup time	10	—	ns
T_{cleh} (72)	Command latch enable to write enable hold time	5	—	ns
T_{cesu} (72)	Chip enable to write enable setup time	15	—	ns
T_{ceh} (72)	Chip enable to write enable hold time	5	—	ns
T_{alesu} (72)	Address latch enable to write enable setup time	10	—	ns
T_{aleh} (72)	Address latch enable to write enable hold time	5	—	ns
T_{dsu} (72)	Data to write enable setup time	10	—	ns

(72) Timing of the NAND interface is controlled through the NAND configuration registers.

Symbol	Description	Min	Max	Unit
T_{dh} (72)	Data to write enable hold time	5	—	ns
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 14: NAND Command Latch Timing Diagram

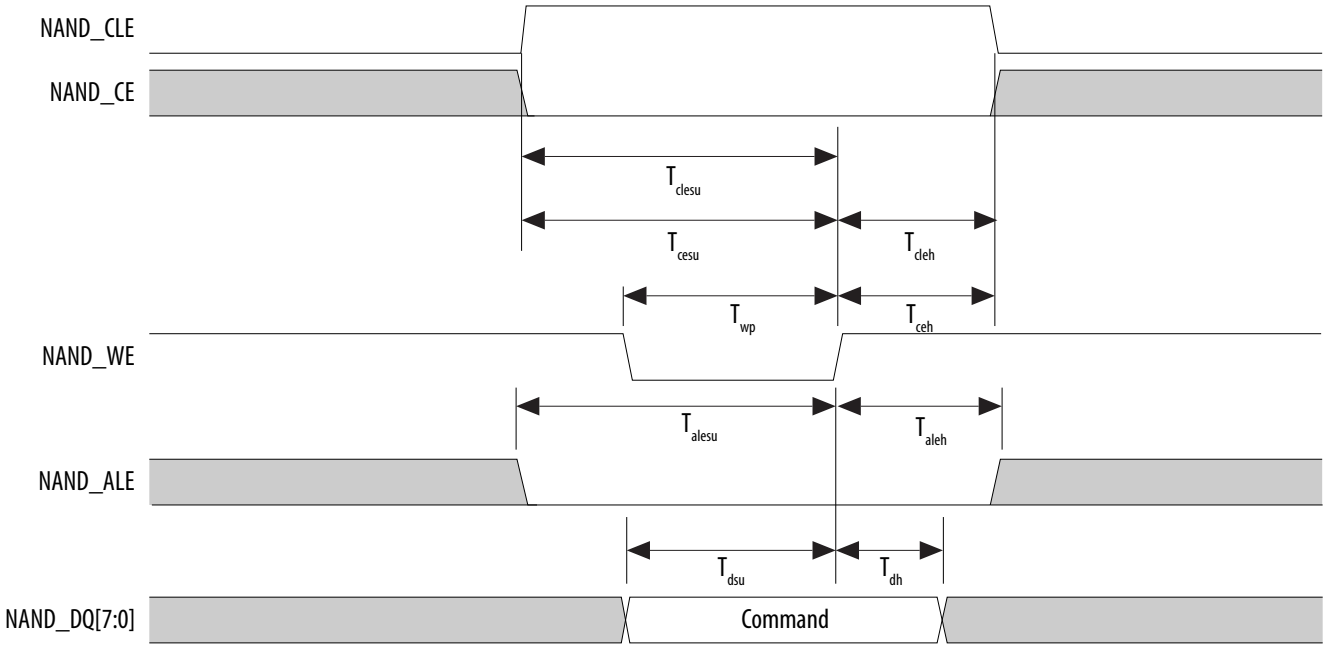


Figure 15: NAND Address Latch Timing Diagram

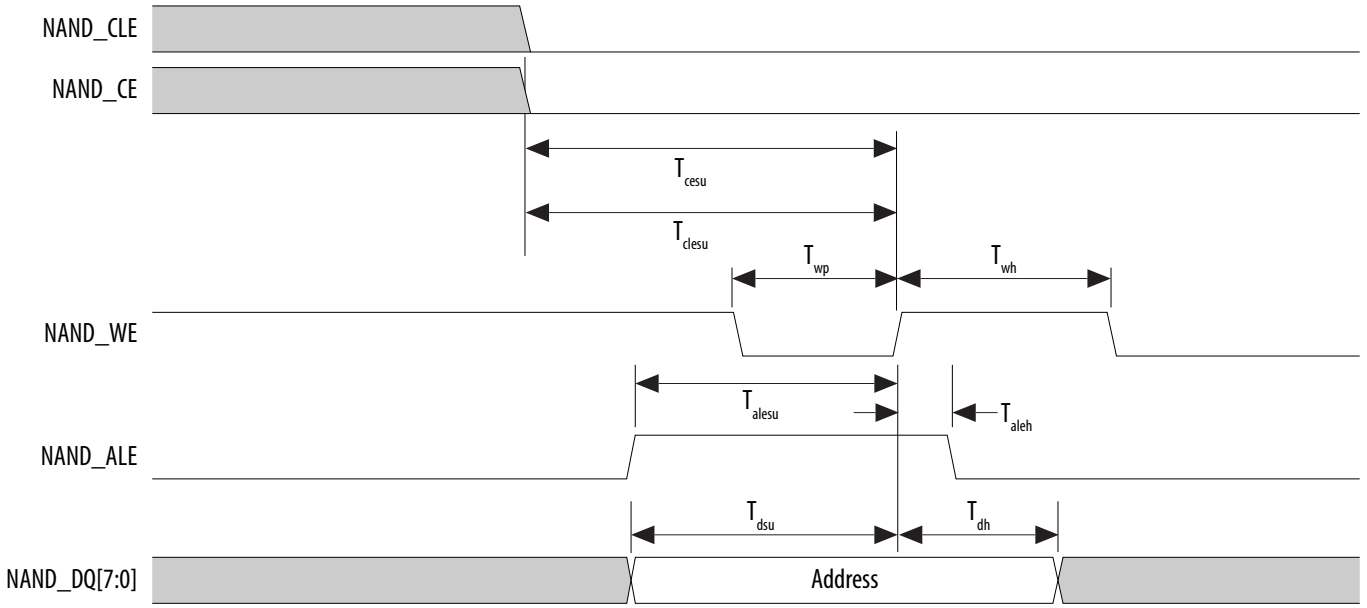


Figure 16: NAND Data Write Timing Diagram

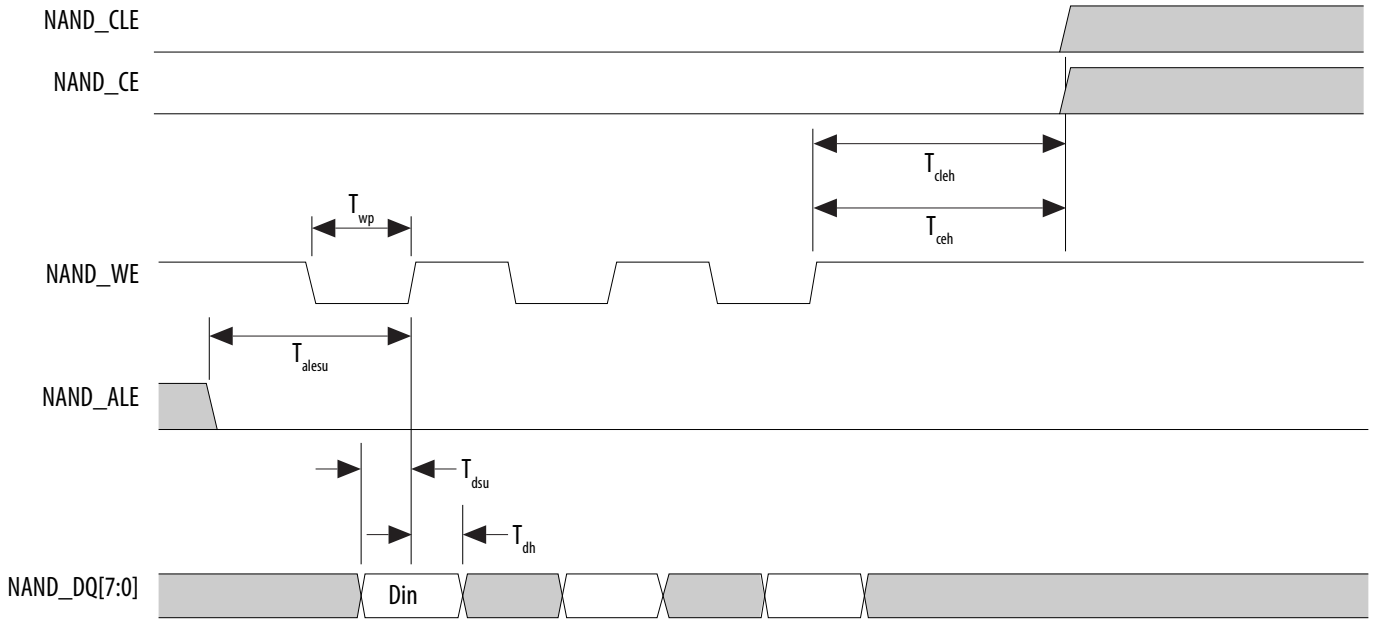
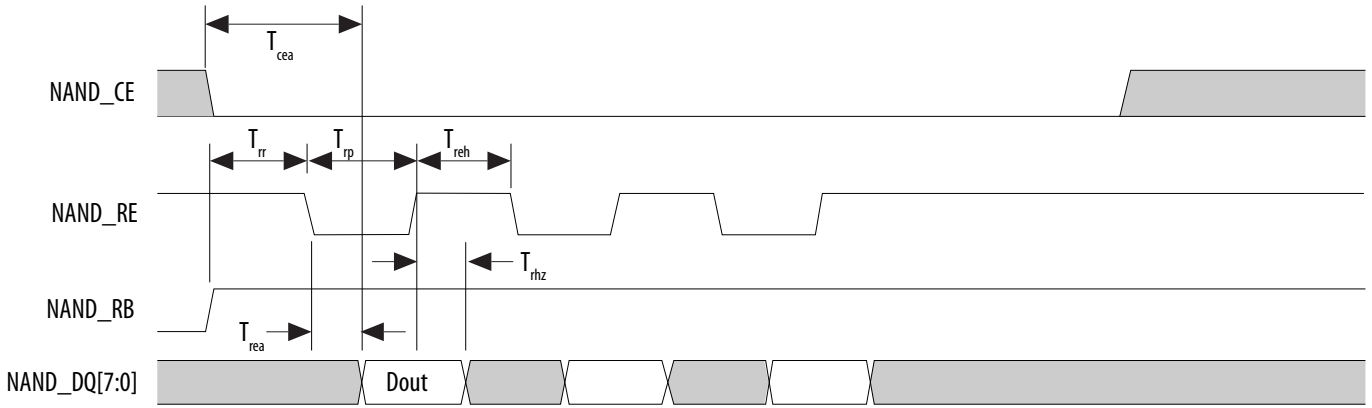


Figure 17: NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 52: ARM Trace Timing Requirements for Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.

CAN Interface

The maximum controller area network (CAN) data rate is 1 Mbps.

HPS JTAG Timing Specifications

Table 53: HPS JTAG Timing Parameters and Values for Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12[73]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14[73]	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14[73]	ns

Configuration Specifications

This section provides configuration specifications and timing for devices.

[73] A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO}= 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

POR Specifications

Table 54: Fast and Standard POR Delay Specification for Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12[74]	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 55: FPGA JTAG Timing Parameters and Values for Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167[75]	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11[76]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14[76]	ns

(74) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.
(75) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.
(76) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Symbol	Description	Min	Max	Unit
t_{JPXZ}	JTAG port valid output to high impedance	—	14(76)	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the device.

Table 56: DCLK-to-DATA[] Ratio for Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Devices table.

Table 57: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(77)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(78)	µs
t_{CF2CK}(79)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(79)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(80)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

(77) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.
(78) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(79) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(80) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 58: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(81)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(82)	µs
t_{CF2CK}(83)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(83)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$(84)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_R	Input rise time	—	40	ns

(81) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(82) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
(83) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(84) N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

Symbol	Parameter	Minimum	Maximum	Unit
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode(85)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 59: AS Timing Parameters for AS ×1 and ×4 Configurations in Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—

(85) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Symbol	Parameter	Minimum	Maximum	Unit
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Related Information

- **PS Configuration Timing** on page 74
- **AS Configuration Timing**
  Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 60: DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

PS Configuration Timing

Table 61: PS Timing Parameters for Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(86)	µs

(86) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(87)	µs
t_{CF2CK}(88)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(88)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(89)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.

(87) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.
(88) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(89) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Initialization

Table 62: Initialization Clock Source Option and the Maximum Frequency for Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR(90)	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

(90) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Table 63: Uncompressed .rbf Sizes for Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the software. However, for a specific version of the software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (**.rbf**) size is specifically for the Configuration via Protocol (CvP) feature.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device[91]
E [92]	A2	21,061,280	275,608	EPCQ64
	A4	21,061,280	275,608	EPCQ64
	A5	33,958,560	322,072	EPCQ128
	A7	56,167,552	435,288	EPCQ128
	A9	102,871,776	400,408	EPCQ256
GX	C3	14,510,912	320,280	EPCQ32
	C4	33,958,560	322,072	EPCQ128
	C5	33,958,560	322,072	EPCQ128
	C7	56,167,552	435,288	EPCQ128
	C9	102,871,776	400,408	EPCQ256
GT	D5	33,958,560	322,072	EPCQ128
	D7	56,167,552	435,288	EPCQ128
	D9	102,871,776	400,408	EPCQ256

[91] The recommended EPCQ serial configuration devices are able to store more than one image.
[92] No PCIe hard IP, configuration via protocol (CvP) is not supported in this family.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device[91]
SE [92]	A2[93]	33,958,560	322,072	EPCQ128
	A4[93]	33,958,560	322,072	EPCQ128
	A5	56,057,632	324,888	EPCQ128
	A6	56,057,632	324,888	EPCQ128
SX	C2[93]	33,958,560	322,072	EPCQ128
	C4[93]	33,958,560	322,072	EPCQ128
	C5	56,057,632	324,888	EPCQ128
	C6	56,057,632	324,888	EPCQ128
ST	D5	56,057,632	324,888	EPCQ128
	D6	56,057,632	324,888	EPCQ128

[91] The recommended EPCQ serial configuration devices are able to store more than one image.
[93] This device will be supported in a future release of the software.

Minimum Configuration Time Estimation

Table 64: Minimum Configuration Time Estimation for Devices

The estimated values are based on the configuration **.rbf** sizes in Uncompressed .rbf Sizes for Devices table.

Variant	Member Code	Active Serial[94]			Fast Passive Parallel[95]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
E	A2	4	100	53	16	125	11
	A4	4	100	53	16	125	11
	A5	4	100	85	16	125	17
	A7	4	100	140	16	125	28
	A9	4	100	257	16	125	51
GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28

(94) DCLK frequency of 100 MHz using external CLKUSR.

Variant	Member Code	Active Serial[94]			Fast Passive Parallel[95]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

Related Information

Configuration Files on page 77

Remote System Upgrades

Table 65: Remote System Upgrade Circuitry Timing Specifications for Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$[96]	250	ns
$t_{RU\_nRSTIMER}$[97]	250	ns

Related Information

- **Remote System Upgrade State Machine**
  Provides more information about configuration reset (RU_CONFIG) signal.

[94] DCLK frequency of 100 MHz using external CLKUSR.
[95] Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.
[95] Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.
[96] This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.
[97] This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

- **User Watchdog Timer**
  Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 66: User Watchdog Internal Oscillator Frequency Specifications for Devices

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

offers two ways to determine I/O timing—the Excel-based I/O timing and the Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Cyclone V I/O Timing Spreadsheet
Provides the Cyclone V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 67: I/O element (IOE) Programmable Delay for Devices

Parameter[98]	Available Settings	Minimum Offset[99]	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C6	–C7	–C8	–I7	–A7	
D1	32	0	0.508	0.517	0.971	1.187	1.194	1.179	1.160	ns

[98] You can set this value in the software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.
[99] Minimum offset does not include the intrinsic delay.

Parameter[98]	Available Settings	Minimum Offset[99]	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C6	–C7	–C8	–I7	–A7	
D3	8	0	1.761	1.793	3.291	4.022	3.961	3.999	3.929	ns
D4	32	0	0.510	0.519	1.180	1.187	1.195	1.180	1.160	ns
D5	32	0	0.508	0.517	0.970	1.186	1.194	1.179	1.179	ns

Programmable Output Buffer Delay

Table 68: Programmable Output Buffer Delay for Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

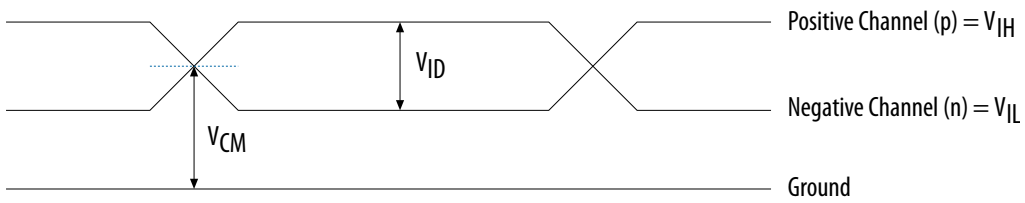
Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

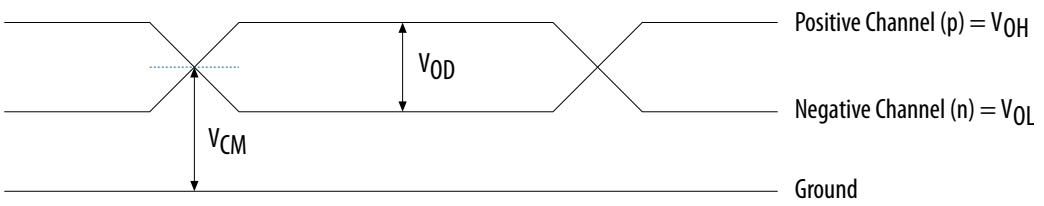
Glossary

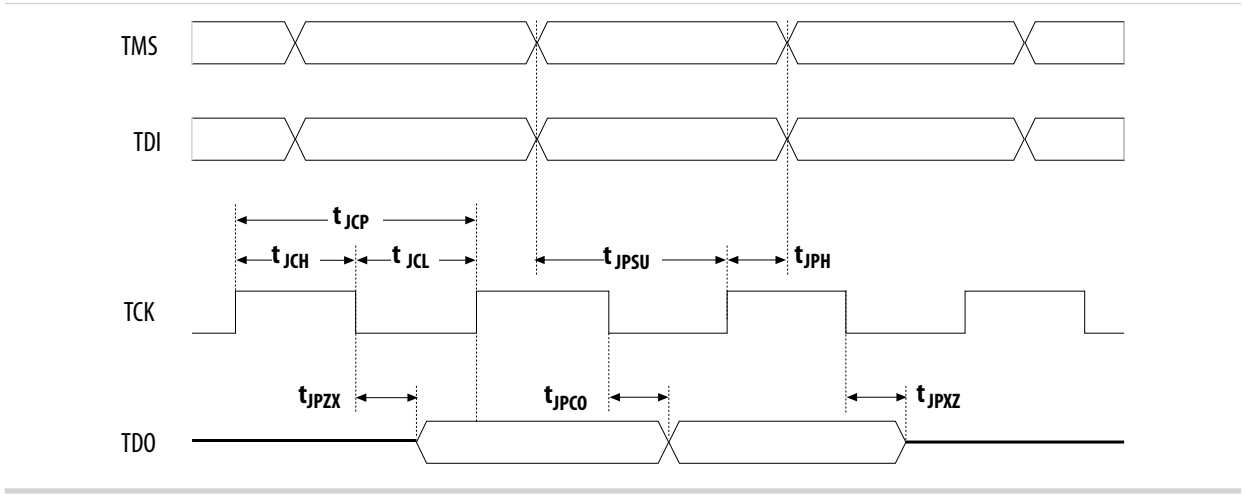
Table 69: Glossary

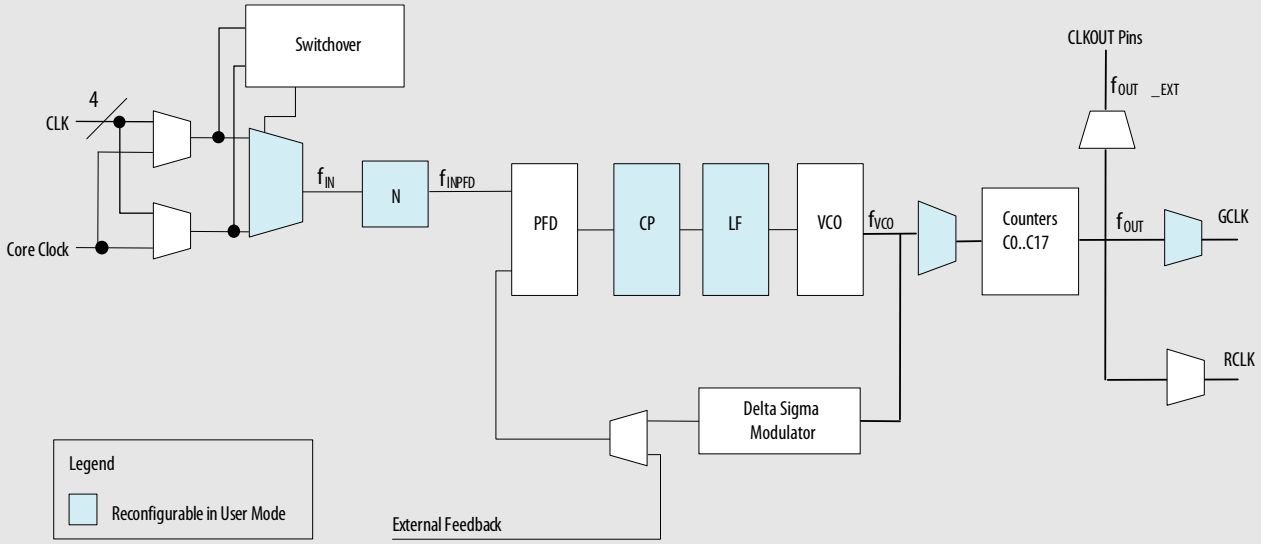
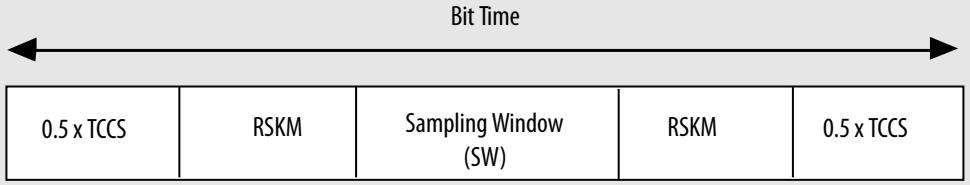
Term	Definition
Differential I/O standards	Receiver Input Waveforms

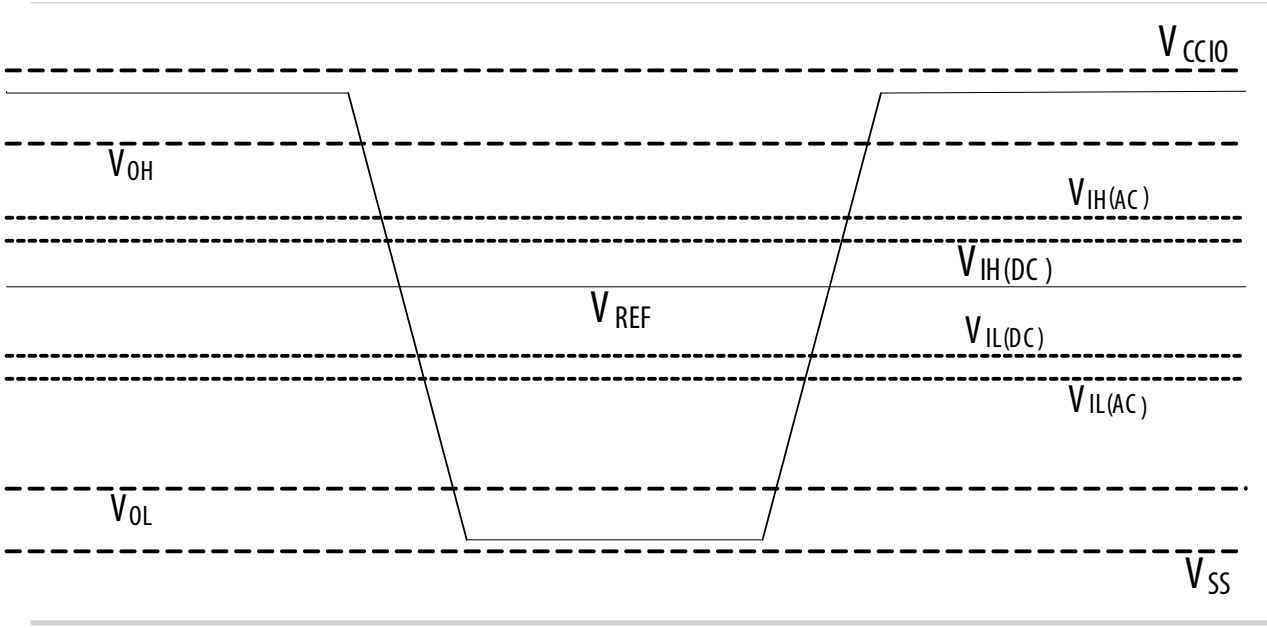
[98] You can set this value in the software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.
[99] Minimum offset does not include the intrinsic delay.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms

Term	Definition
	Single-Ended Waveform  **Differential Waveform** 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI).
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

Term	Definition
JTAG timing specifications	JTAG Timing Specifications 

Term	Definition
PLL specifications	Diagram of PLL specifications  **Note:** (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.
R_L	Receiver differential input discrete resistor (external to the device).
Sampling window (SW)	Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 

Term	Definition
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard 
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.

Term	Definition
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
$V_{CM(DC)}$	DC common mode input voltage.
V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage

Term	Definition
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes

June 2016	2016.06.10	• Changed pin capacitance to maximum values.
		• Updated SPI Master Timing Requirements for Devices table.
		  • Added T_{su} and T_h specifications.
		  • Removed T_{dinmax} specifications.
		• Updated SPI Master Timing Diagram.
		• Updated T_{clk} spec from maximum to minimum in I^2C Timing Requirements for Devices table.

Date	Version	Changes

December 2015	2015.12.04	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Devices table.
		  • Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications.
		  • Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Devices table.
		• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Devices table.
		  • Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol.
		  • Updated $T_{sdmmc\_clk\_out}$ and T_d specifications.
		  • Added T_{sdmmc_clk}, T_{su}, and T_h specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the following diagrams:
		  • Quad SPI Flash Timing Diagram
		  • SD/MMC Timing Diagram
		• Updated configuration .rbf sizes for devices.
		• Changed instances of *Quartus II* to *Quartus Prime*.

Date	Version	Changes

June 2015	2015.06.12	• Updated the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Devices table:
		  • True RSDS output standard: data rates of up to 360 Mbps
		  • True mini-LVDS output standard: data rates of up to 400 Mbps
		• Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		• Updated T_h location in I^2C Timing Diagram.
		• Updared T_{wp} location in NAND Address Latch Timing Diagram.
		• Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Devices chapter.
		  • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		  • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		  • AS Configuration Timing Waveform
		  • PS Configuration Timing Waveform

March 2015	2015.03.31	• Added V_{CC} specifications for devices with internal scrubbing feature (with SC suffix) in Recommended Operating Conditions table. • Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Devices table.

Date	Version	Changes

January 2015	2015.01.23	• Updated the transceiver specification for ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables:
		  • Transceiver Power Supply Operating Conditions for GX, GT, SX, and ST Devices
		  • Transceiver Specifications for GX, GT, SX, and ST Devices
		  • Transceiver Compliance Specification for All Supported Protocol for Devices
		• Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC\_AUX\_SHARED}$ must be powered by the same source as VCC_AUX for SX C5, C6, D5, and D6 devices, and SE A5 and A6 devices. Updated in the following tables:
		  • Absolute Maximum Ratings for Devices
		  • HPS Power Supply Operating Conditions for SE, SX, and ST Devices
		• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.
		• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.
		• Updated f_{VCO} maximum value from 1400 MHz to 1600 MHz for –C7 and –I7 speed grades in the PLL specifications table.
		• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.
		• Added the following notes in the High-Speed I/O Specifications for Devices table:
		  • The devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks.
		  • The devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks.
		• Updated HPS Clock Performance main_base_clk specifications from 462 MHz to 400 MHz for –C6 speed grade.
		• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C7, –I7, –A7, and –C8 speed grades) and 1,850 MHz (for –C6 speed grade).
		• Changed the symbol for HPS PLL input jitter divide value from NR to N.

Date	Version	Changes

		• Removed “Slave select pulse width (Texas Instruments SSP mode)” parameter from the following tables:
		  • SPI Master Timing Requirements for Devices
		  • SPI Slave Timing Requirements for Devices
		• Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.
		• Added HPS JTAG timing specifications.
		• Updated the configuration **.rbf** size (bits) for devices.
		• Added a note to Uncompressed .rbf Sizes for Devices table: The recommended EPCQ serial configuration devices are able to store more than one image.

July 2014	3.9	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20. • Updated h2f_user2_clk specification for –C6, –C7, and –I7 speed grades in Table 34. • Updated description in “HPS PLL Specifications” section. • Updated VCO range maximum specification in Table 35. • Updated T_d and T_h specifications in Table 41. • Added T_h specification in Table 43 and Figure 10. • Updated a note in Figure 17, Figure 18, and Figure 20 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed “Remote update only in AS mode” specification in Table 54. • Added DCLK device initialization clock source specification in Table 56. • Added description in “Configuration Files” section: The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature. • Added "Recommended EPCQ Serial Configuration Device" values in Table 57. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 59.

Date	Version	Changes
February 2014	3.8	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.7	• Updated Table 1, Table 3, Table 19, Table 20, Table 23, Table 25, Table 27, Table 34, Table 44, Table 51, Table 52, Table 55, and Table 61. • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 24, Table 25, Table 26, Table 27, Table 28, Table 32, Table 33, Table 49, Table 50, Table 51, Table 52, Table 53, Table 54, Table 55, Table 57, Table 58, Table 59, Table 60, and Table 62.
November 2013	3.6	Updated Table 23, Table 30, and Table 31.
October 2013	3.5	• Added "HPS PLL Specifications". • Added Table 23, Table 35, and Table 36. • Updated Table 1, Table 5, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, Table 28, Table 34, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, and Table 53. • Updated Figure 1, Figure 2, Figure 4, Figure 10, Figure 12, Figure 13, and Figure 16. • Removed table: GPIO Pulse Width for Devices.

June 2013	3.4	• Updated Table 20, Table 27, and Table 34.
		• Updated "UART Interface" and "CAN Interface" sections.
		• Removed the following tables:
		  • Table 45: UART Baud Rate for Devices
		  • Table 47: CAN Pulse Width for Devices

May 2013	3.3	• Added Table 33. • Updated Figure 5, Figure 6, Figure 17, Figure 19, and Figure 20. • Updated Table 1, Table 4, Table 5, Table 10, Table 13, Table 19, Table 20, Table 26, Table 32, Table 35, Table 36, Table 43, Table 53, Table 54, Table 57, and Table 61.

Date	Version	Changes
March 2013	3.2	• Added HPS reset information in the "HPS Specifications" section. • Added Table 57. • Updated Table 1, Table 2, Table 17, Table 20, Table 52, and Table 56. • Updated Figure 18.
January 2013	3.1	Updated Table 4, Table 20, and Table 56.

November 2012	3.0	• Updated Table 1, Table 4, Table 5, Table 9, Table 14, Table 16, Table 17, Table 19, Table 20, Table 25, Table 28, Table 52, Table 55, Table 56, and Table 59.
		• Removed table: Transceiver Block Jitter Specifications for GX Devices.
		• Added HPS information:
		  • Added "HPS Specifications" section.
		  • Added Table 33, Table 34, Table 35, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, and Table 46.
		  • Added Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16.
		  • Updated Table 3.

June 2012	2.0	Updated for the software v12.0 release: • Restructured document. • Removed "Power Consumption" section. • Updated Table 1,Table 3, Table 19, Table 20, Table 25, Table 27, Table 28, Table 30, Table 31, Table 34, Table 36, Table 37, Table 38, Table 39, Table 41, Table 43, and Table 46. • Added Table 22, Table 23, and Table 29. • Added Figure 1 and Figure 2. • Added "Initialization" and "Configuration Files" sections.

Date	Version	Changes
February 2012	1.2	• Added automotive speed grade information. • Added Figure 2–1. • Updated Table 2–3, Table 2–8, Table 2–9, Table 2–19, Table 2–20, Table 2–21, Table 2–22, Table 2–23, Table 2–24, Table 2–25, Table 2–26, Table 2–27, Table 2–28, Table 2–30, Table 2–35, and Table 2–43. • Minor text edits.
November 2011	1.1	• Added Table 2–5. • Updated Table 2–3, Table 2–4, Table 2–11, Table 2–13, Table 2–20, and Table 2–21.
October 2011	1.0	Initial release.