APS12625 and APS12626

2D Hall-Effect Speed and Direction Sensor ICs

FEATURES AND BENEFITS

- Flexible and easy-to-use sensor for motors/encoders
- ISO 26262:2011 / ASIL A functional safety compliance
- 2D magnetic sensing via planar and vertical Hall elements
  - □ Quadrature independent of magnet pole pitch and air gap—no target optimization required
  - □ Works in almost any orientation to the target (XY, ZX, and ZY options)
- Reduces accumulation of lost counts/pulses
  - □ System can restore correct state after power-cycling (-P option)
- Dual outputs of quadrature or speed/direction signals
- High magnetic sensitivity
- Optimized for applications with regulated power rails
  - □ Operation from 2.8 to 5.5 V
- Automotive grade/qualified per AEC-Q100
  - □ T_J up to 175°C
  - □ Output short-circuit protection
  - □ Resistant to physical stress
- Small size

TYPICAL APPLICATIONS

- Automotive
  - □ Power closures/actuators
  - □ Electronic power steering
  - □ Seat/window/sunroof motors
  - □ Trunk/door/liftgate motors
- Industrial motors/encoders
- Garage door openers
- Motorized window blinds
- White goods

DESCRIPTION

The APS12625 and APS12626 integrated circuits are dual ultrasensitive Hall-effect latches optimized for use with ring magnets. They feature both vertical and planar Hall elements with sensing axes that are orthogonal to one another, providing 90° of phase separation. This phase separation is inherently independent of magnet pole spacing and air gap. No target optimization is required, making them extremely flexible and easy to use.

For example, the ring magnet pole-pitch can be changed without having to modify the sensor position or other mechanical design details. Additionally, XY, ZX, and ZY options are available to work in almost any orientation to the target. The APS12625 features Speed and Direction outputs, while the APS12626 has quadrature outputs (Channel A/B).

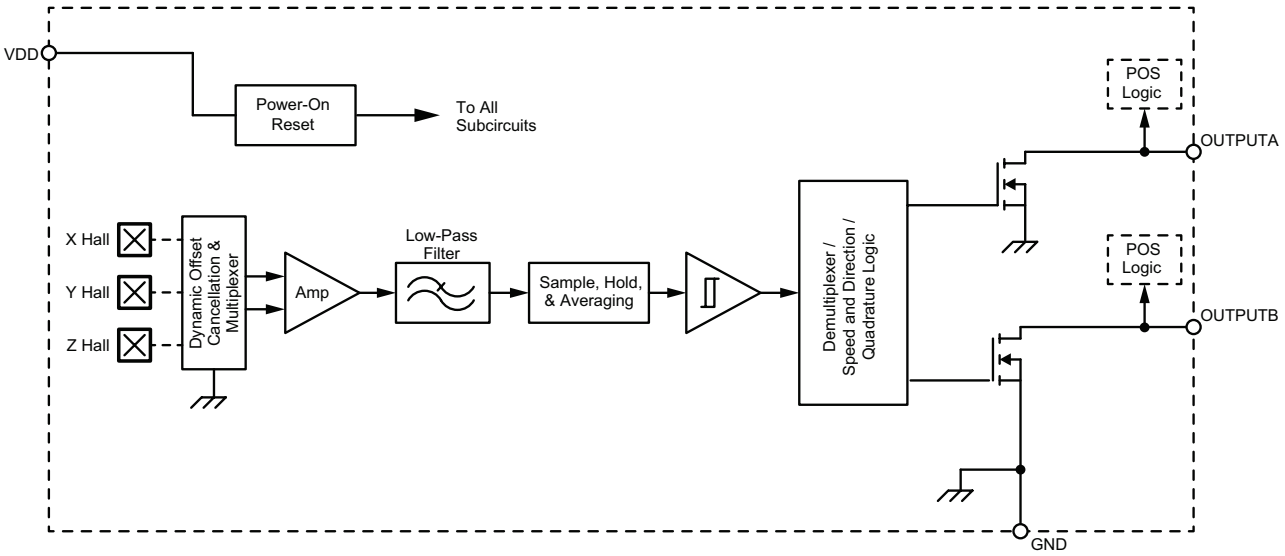
A unique feature allows the host system to restore the correct state after power-cycling the device (-P option). This reduces the potential accumulation of lost counts/pulses when the device wakes up with one or more sensors in its hysteresis region.

Continued on the next page…

PACKAGE

5-Pin SOT23-W (Suffix LH)

Not to scale



Functional Block Diagram

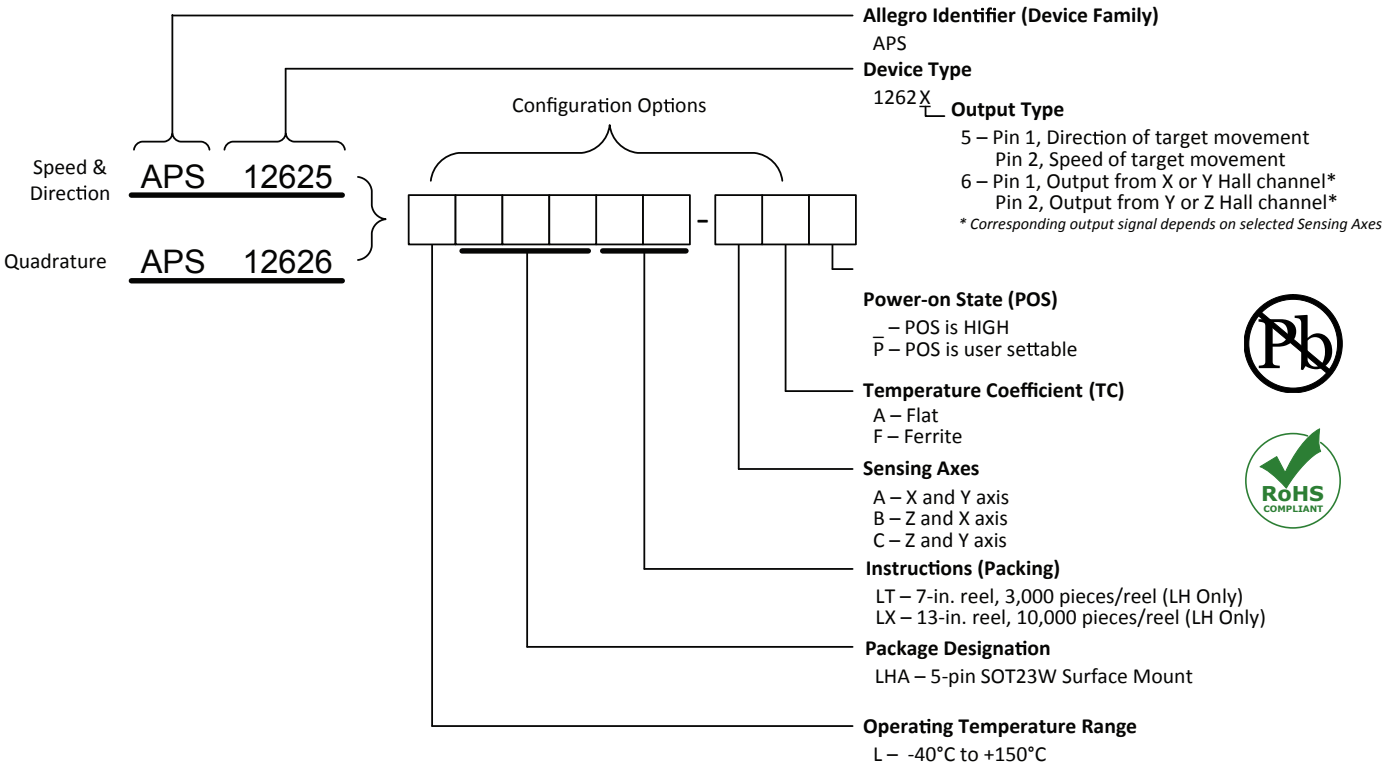
DESCRIPTION (continued)

On a single silicon chip, these devices include: three Hall plates (one planar and two vertical), a multiplexer, a small-signal amplifier, chopper stabilization, a Schmitt trigger, and two NMOS output transistors which can sink up to 10 mA continuously. They operate from a regulated supply voltage of 2.8 to 5.5 V and have been qualified beyond the requirements of AEC-Q100 grade 0 for operation up to 175°C junction temperature.

The small geometries of the BiCMOS process allow these devices to be offered in an ultrasmall package. Package designator "LH" indicates a modified SOT23-W surface-mount package. This package is RoHS compliant and lead (Pb) free, with 100% matte tin leadframe plating.

SELECTION GUIDE

Complete Part Number Format



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{DD}		6	V
Reverse Supply Voltage	V_{RDD}		–0.3	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUT}		6	V
Output Current	I_{OUT}	Through short-circuit current-limiting device	45	mA
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
		For 500 hours	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C

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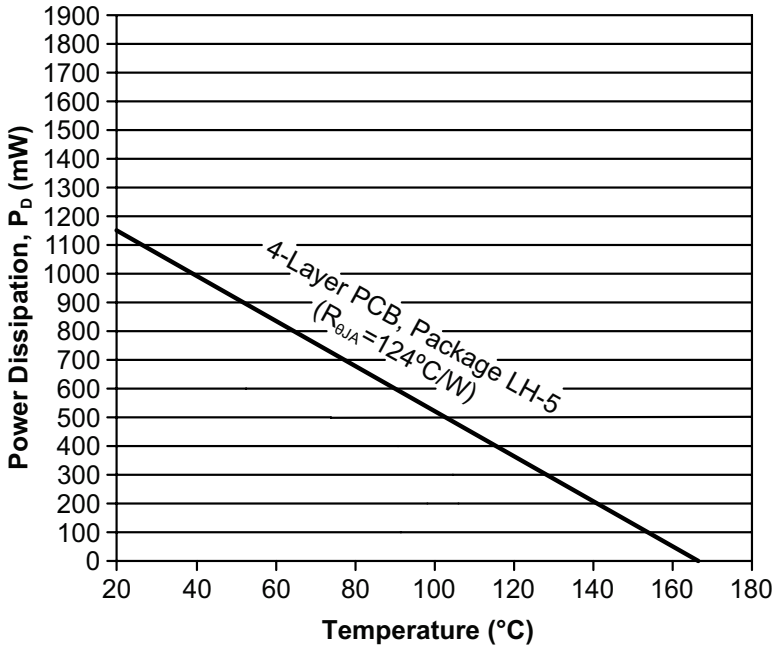
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Notes	Rating	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH-5 4-layer board based on the JEDEC standard JESD51-7	124	°C/W

* Additional thermal information available on the Allegro website.



Maximum Power Dissipation versus Ambient Temperature

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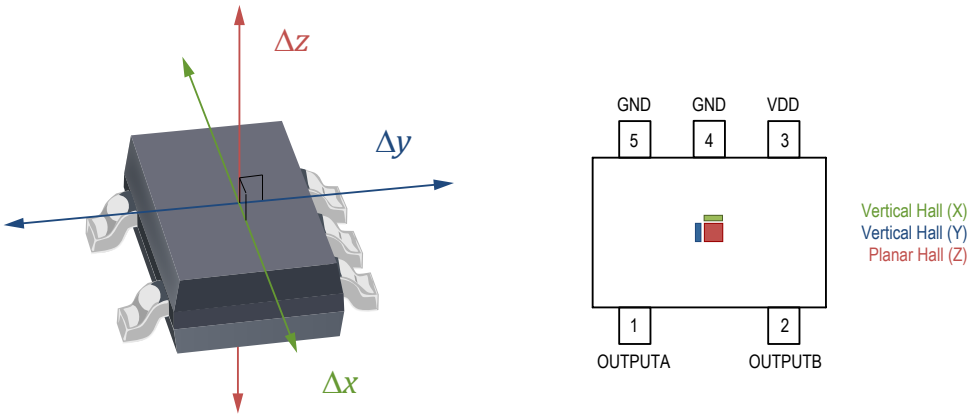
PINOUT DIAGRAMS, TERMINAL LIST, AND OUTPUT OPTION TABLES



Package LH, 5-Pin SOT23-W

Terminal List Table

Number	Symbol	Description
1	OUTPUTA	*See output option table*
2	OUTPUTB	*See output option table*
3	VDD	Connects power supply to chip
4	GND	Ground [1]
5	GND	Ground [1]

[1] Only one GND connection is required; other GND pin can float or also be tied to GND.

Output Option Table

Device	Order Option [2]	Sensing Axes	OUTPUT A (Pin 1)	OUTPUTB (Pin 2)
APS12625	A	XY	Speed of target movement	Direction of target movement
	B	ZX		
	C	ZY		
APS12626	A	XY	X channel output	Y channel output
	B	ZX	Z channel output	X channel output
	C	ZY	Z channel output	Y channel output

[2] See Selection Guide.

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ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature range T_A = –40°C to 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
Supply Voltage	V_{DD}	Operating, $T_J \le T_J$(max)	2.8	–	5.5	V
Output Leakage Current	I_{OUTOFF}	$B < B_{RP}$	–	–	10	µA
Output On Voltage	$V_{OUT(SAT)}$	I_{OUT} = 2 mA, $B > B_{OP}$	–	180	500	mV
Output Off Voltage	$V_{OUT(OFF)}$	OUTA and OUTB are open-drain; application sets output off voltage	–	–	5.5	V
Supply Current	I_{DD}		–	3	4.5	mA
Output Current	I_{OUT}	Value used during characterization	–	5	–	mA
Output Sink Current	$I_{OUTPUT(SINK)}$		–	–	10	mA
Output Short-Circuit Current Limit	I_{OM}	V_{DD} = 5.5 V, $T_J \le T_J$(max)	15	–	45	mA
Output Rise Time [2][3]	t_r	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	0.2	–	µs
Output Fall Time [2][3]	t_f	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	0.1	–	µs
Power-On Time	t_{ON}	Both outputs, APS12625	–	150	300	µs
		Both outputs, APS12626	–	50	100	µs
Power-On State External Input	t_{POS_input}	Hold time for external POS setting signal, *-P* option only; see Figure 10	100	–	–	µs
Power-On State, Output A and B	POS		High			–
Delay Between Direction and Speed Pin Update	$t_{dir\text{-}to\text{-}speed}$	Only valid for APS12625	2.8	4.0	8	µs
Speed Pin Input Low Level Channel A / B Input Low Level	$V_{IN(LOW)}$	For APS12625 *-P* option For APS12626 *-P* option	–	–	0.8	V
Speed Pin Input High Level Channel A / B Input High Level	$V_{IN(HIGH)}$	For APS12625 *-P* option For APS12626 *-P* option	2.0	–	–	V

[1] Typical data are at T_A = 25°C and V_{DD} = 4 V.
[2] Power-on time, rise time, and fall time are guaranteed through device characterization.
[3] C_{LOAD} = oscilloscope probe capacitance.

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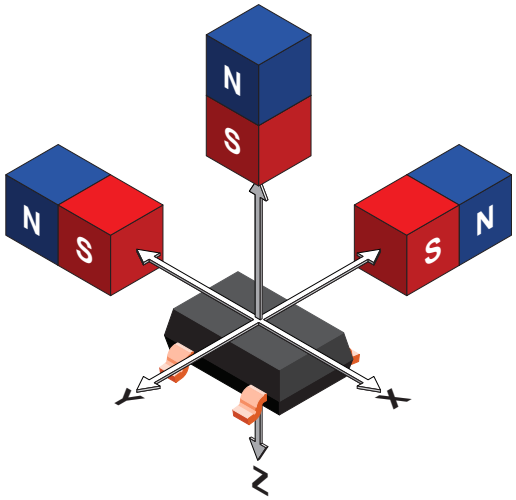
MAGNETIC CHARACTERISTICS: **Valid over full operating voltage and temperature ranges, unless otherwise specified**

Characteristics	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit [2]
Operate Point [3]	$B_{OP(A)}$, $B_{OP(B)}$	TC = 0	T_A = –40°C	12	27.8	44	G
			T_A = 25°C	11	25.0	41	G
			T_A = 150°C	1	19.7	39	G
		TC = 1		1	21	40	G
Release Point [3]	$B_{RP(A)}$, $B_{RP(B)}$	TC = 0	T_A = –40°C	–44	–27.8	–12	G
			T_A = 25°C	–41	–25.0	–11	G
			T_A = 150°C	–39	–19.7	–1	G
		TC = 1		–40	–21	–1	G
Hysteresis ($B_{OP} – B_{RP}$)	$B_{HYS(A)}$, $B_{HYS(B)}$	TC = 0	T_A = –40°C	38	55.5	72	G
			T_A = 25°C	35	50.0	66	G
			T_A = 150°C	25	39.4	54	G
		TC = 1		25	42	65	G
Symmetry: Channel A, Channel B, $B_{OP(A)} + B_{RP(A)}$, $B_{OP(B)} + B_{RP(B)}$	$B_{SYM(A)}$, $B_{SYM(B)}$			–35	–	35	G
Operate Symmetry: $B_{OP(A)} – B_{OP(B)}$	$B_{SYM(AB,OP)}$			–15	–	15	G
Release Symmetry: $B_{RP(A)} – B_{RP(B)}$	$B_{SYM(AB,RP)}$			–15	–	15	G
Temperature Coefficient	TC	TC = 0, APS12625-F, APS12626-F		–	–0.17	–	%/°C
		TC = 1, APS12625, APS12626		–	0	–	%/°C

[1] Typical data are at T_A = 25°C and V_{DD} = 4 V.
[2] 1 G (gauss) = 0.1 mT (millitesla)
[3] Applicable to all directions (X, Y, and Z).

South polarity magnetic fields, in the orientations illustrated (right), are considered positive fields.



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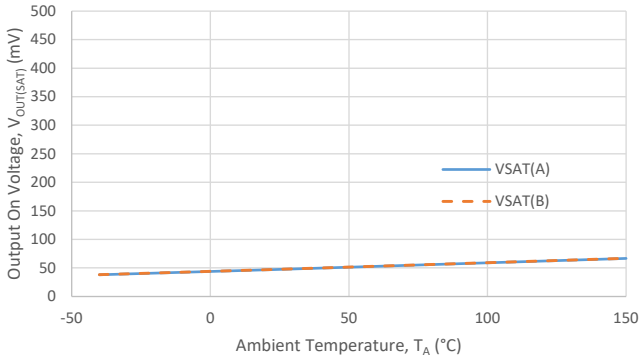
CHARACTERISTIC DATA

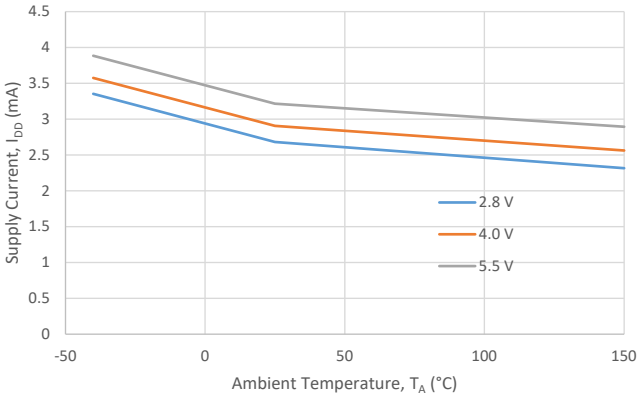
Electrical Characteristics

Output On Voltage vs. Temperature

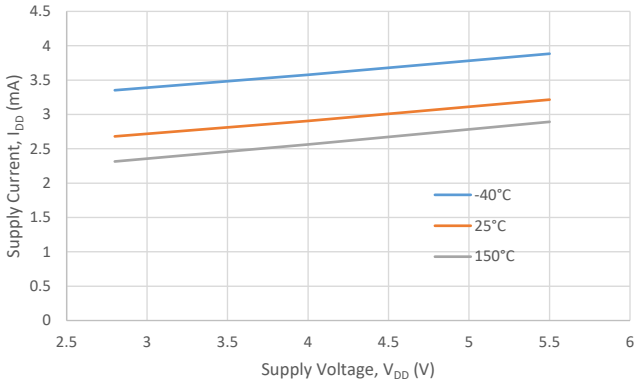
I_{OUT} = 2 mA, B > B_{OP}



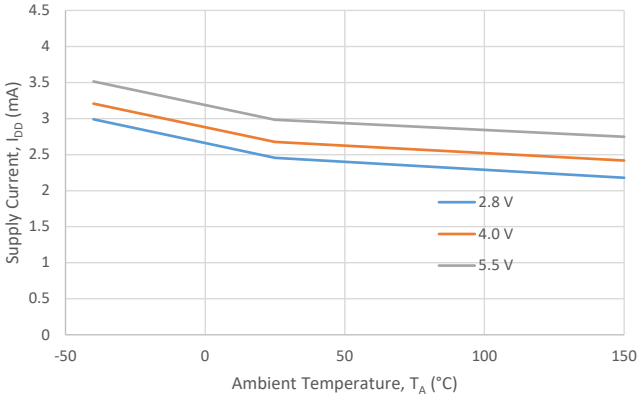
Supply Current (XY) vs. Temperature



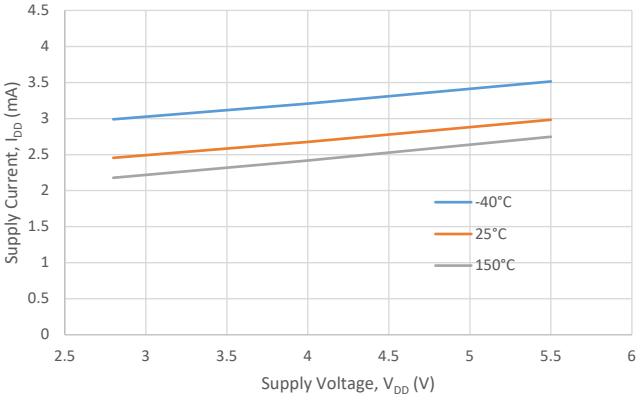
Supply Current (XY) vs. Supply Voltage



Supply Current (ZX & ZY) vs. Temperature



Supply Current (ZX & ZY) vs. Supply Voltage



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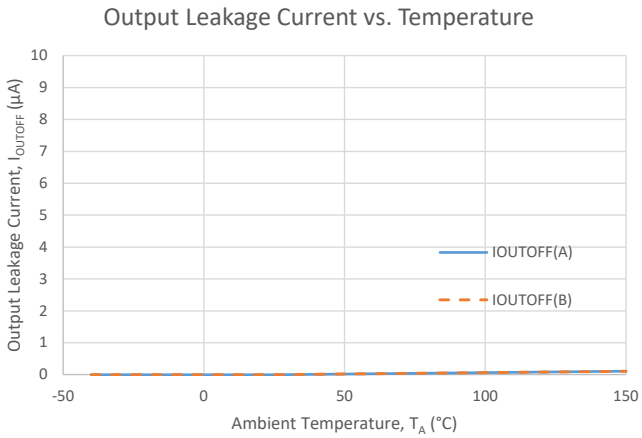
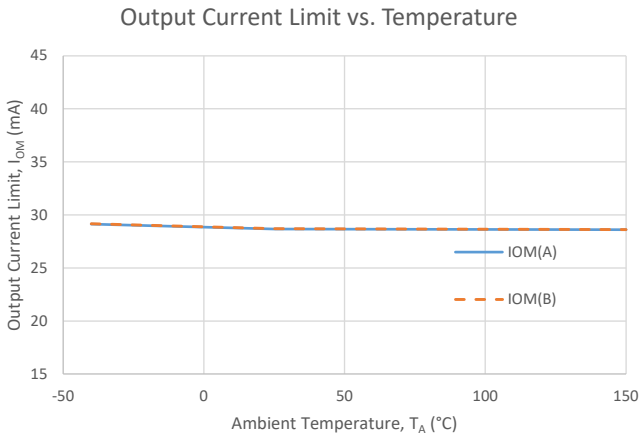
CHARACTERISTIC DATA

Electrical Characteristics (continued)





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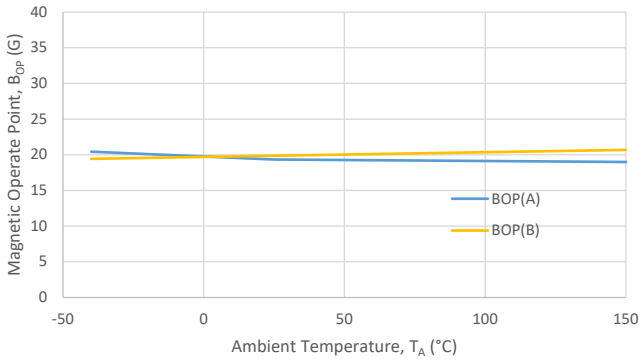
CHARACTERISTIC DATA

Magnetic Characteristics

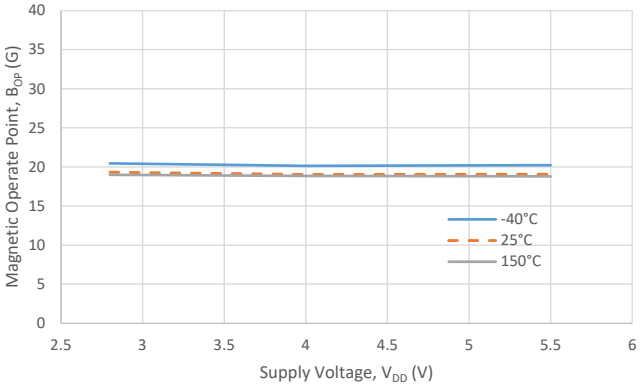
Option A (XY) with TC option A (flat)

Operate Point vs. Temperature

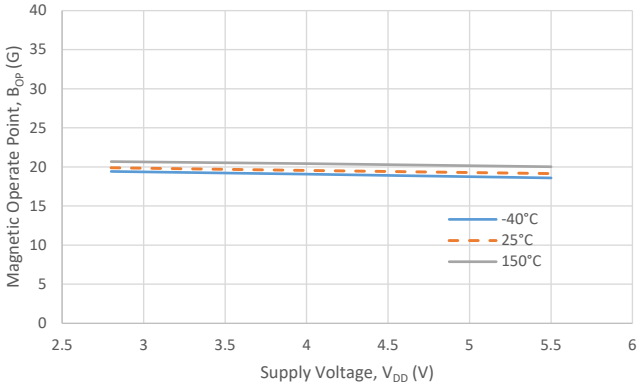
V_{DD} = 2.8 V



Operate Point (A) vs. Supply Voltage



Operate Point (B) vs. Supply Voltage



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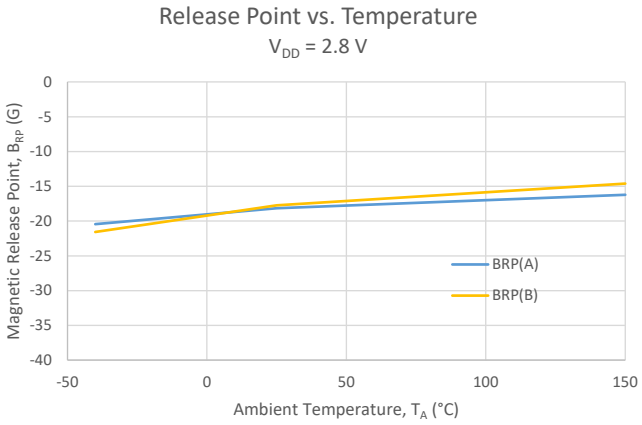
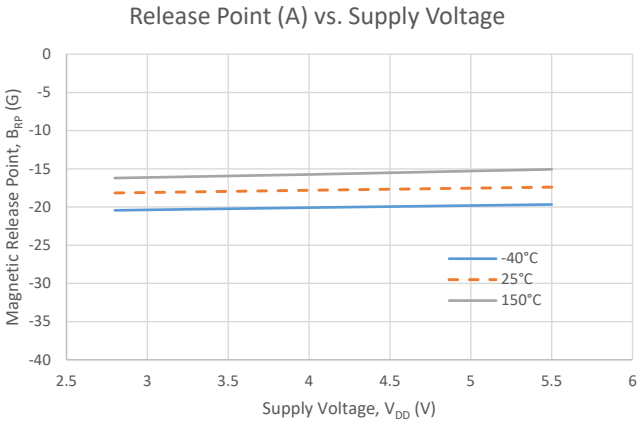
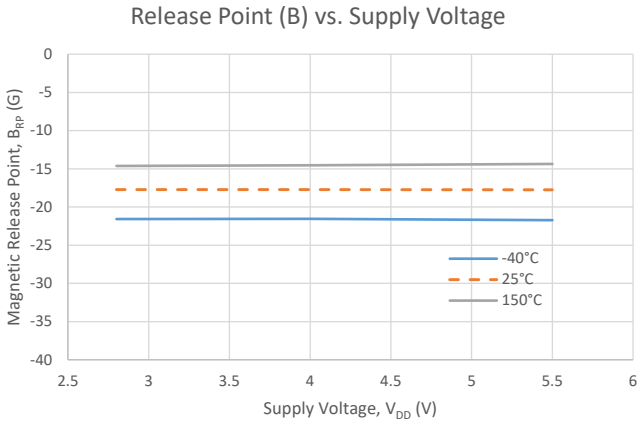
CHARACTERISTIC DATA

Magnetic Characteristics

Option A (XY) with TC option A (flat) (continued)







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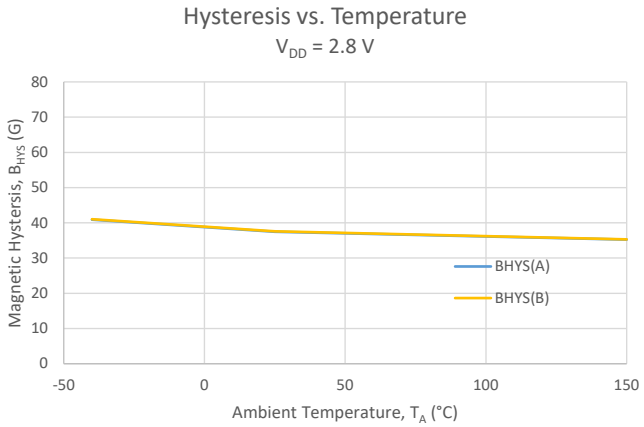
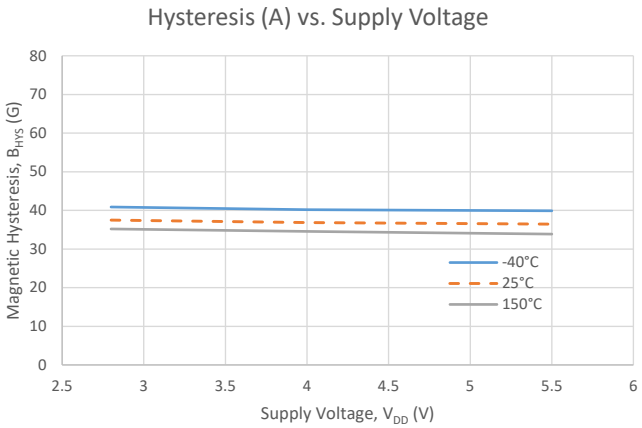
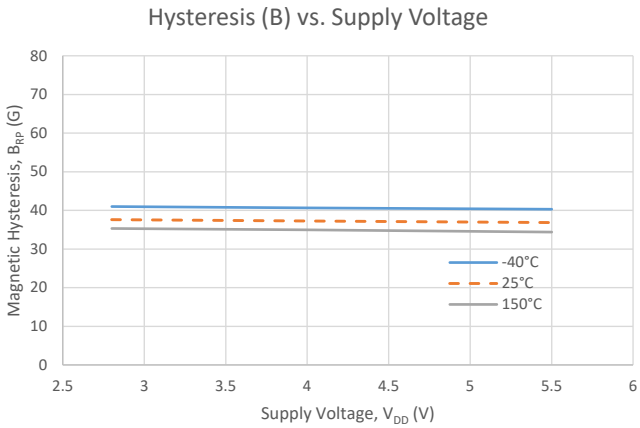
CHARACTERISTIC DATA

Magnetic Characteristics

Option A (XY) with TC option A (flat) (continued)







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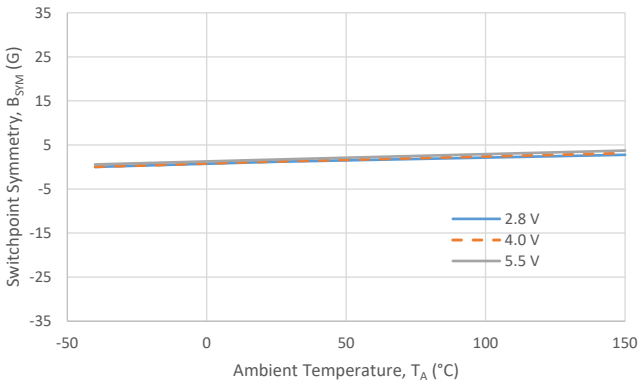
CHARACTERISTIC DATA

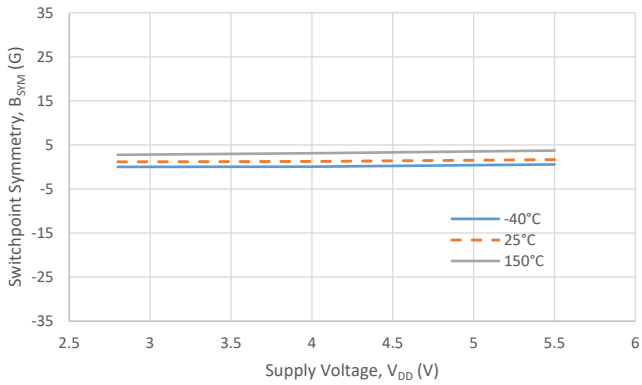
Magnetic Characteristics

Option A (XY) with TC option A (flat) (continued)

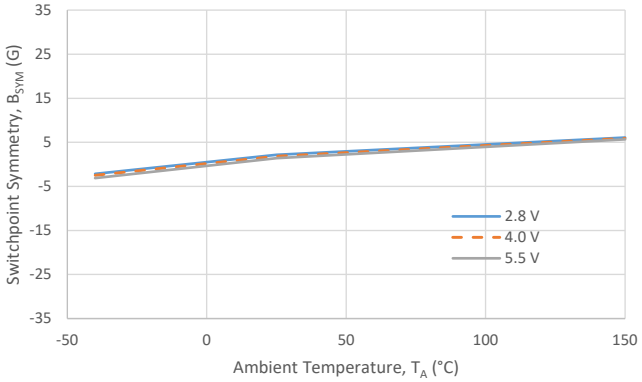
Symmetry (A) vs. Temperature



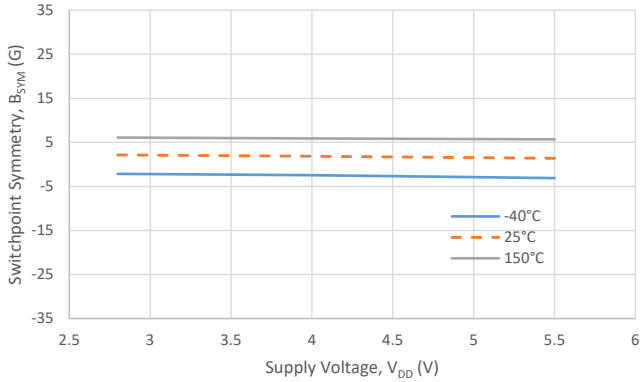
Symmetry (A) vs. Supply Voltage



Symmetry (B) vs. Temperature



Symmetry (B) vs. Supply Voltage



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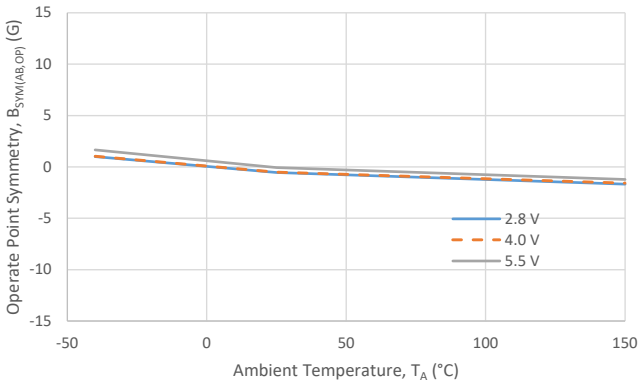
CHARACTERISTIC DATA

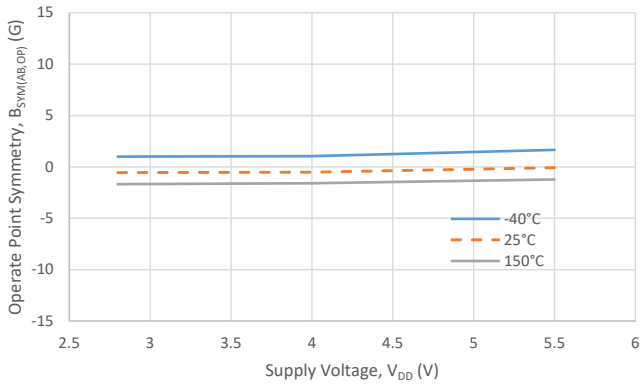
Magnetic Characteristics

Option A (XY) with TC option A (flat) (continued)

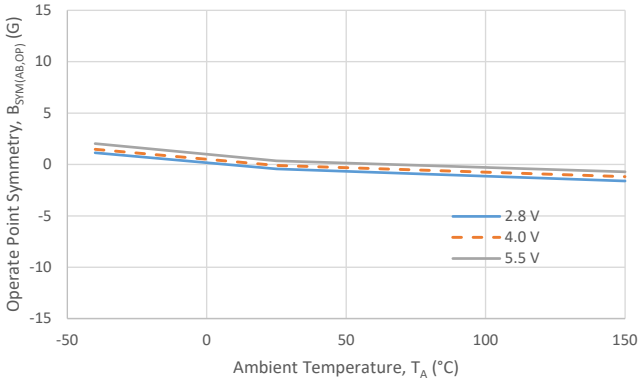
Operate Symmetry (AB) vs. Temperature



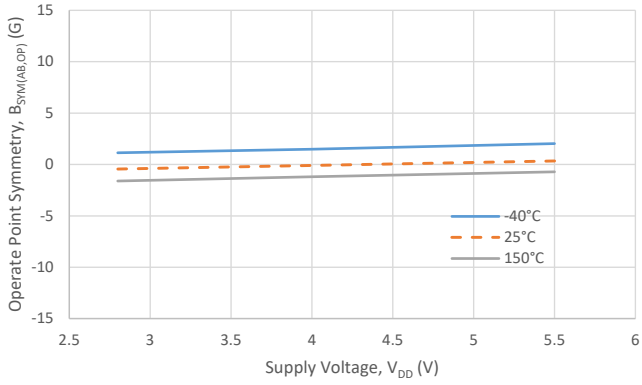
Operate Symmetry (AB) vs. Supply Voltage



Release Symmetry (AB) vs. Temperature



Release Symmetry (AB) vs. Supply Voltage



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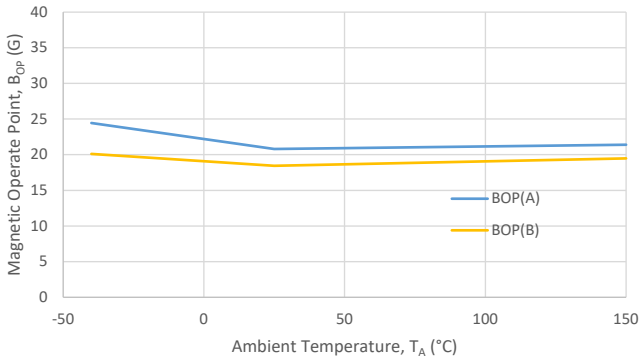
CHARACTERISTIC DATA

Magnetic Characteristics

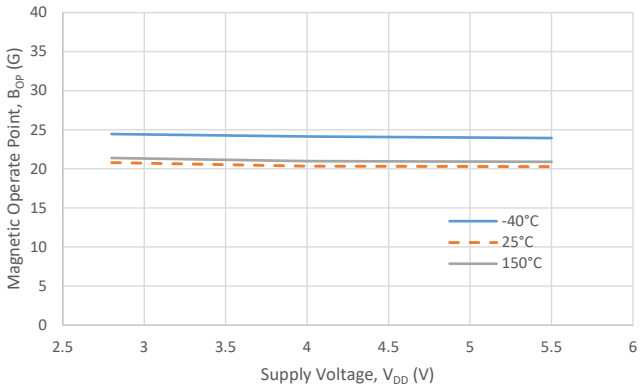
Option B & C (ZX & ZY) with TC option A (flat)

Operate Point vs. Temperature

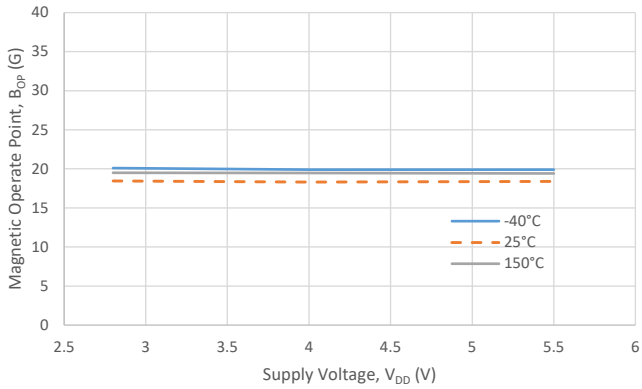
V_{DD} = 2.8 V



Operate Point (A) vs. Supply Voltage



Operate Point (B) vs. Supply Voltage



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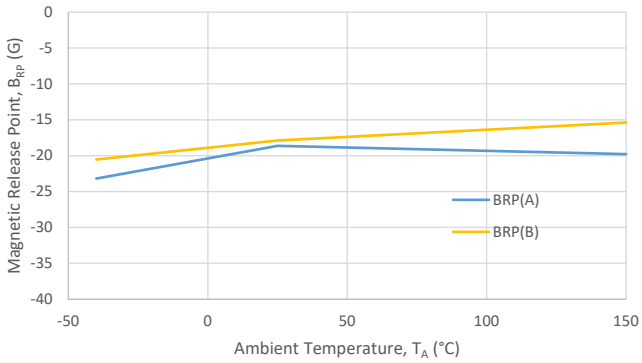
CHARACTERISTIC DATA

Magnetic Characteristics

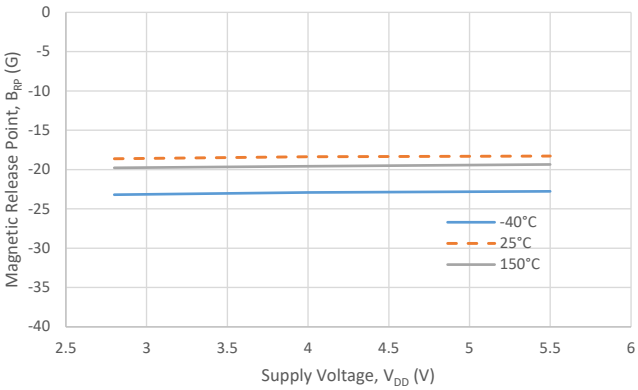
Option B & C (ZX & ZY) with TC option A (flat) (continued)

Release Point vs. Temperature

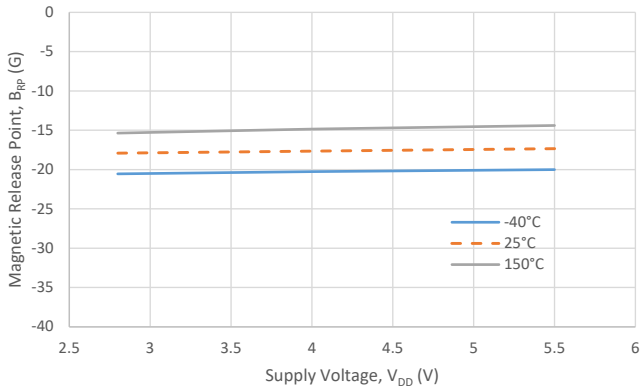
V_{DD} = 2.8 V



Release Point (A) vs. Supply Voltage



Release Point (B) vs. Supply Voltage



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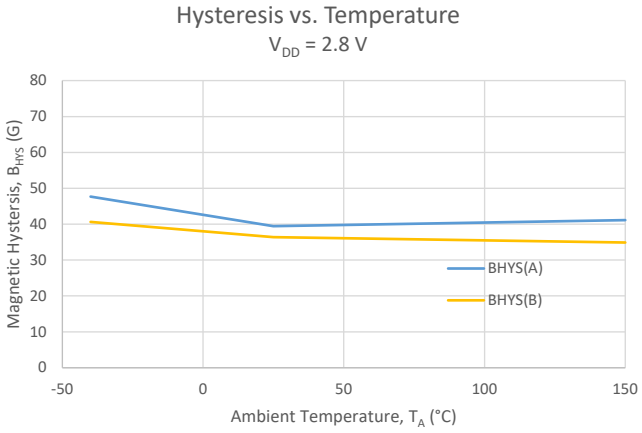
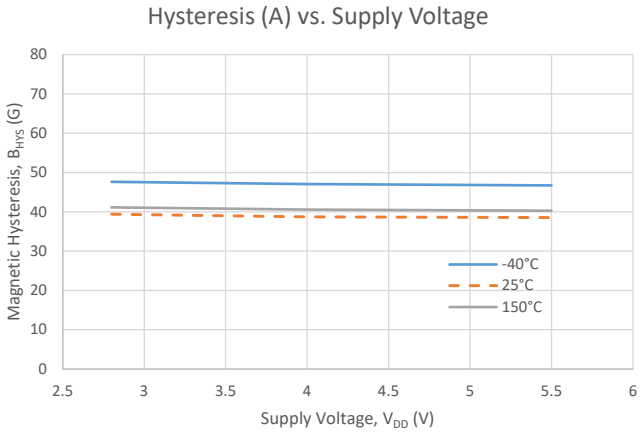
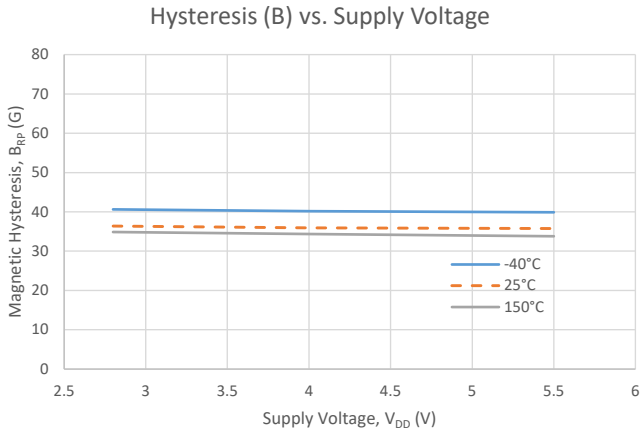
CHARACTERISTIC DATA

Magnetic Characteristics

Option B & C (ZX & ZY) with TC option A (flat) (continued)







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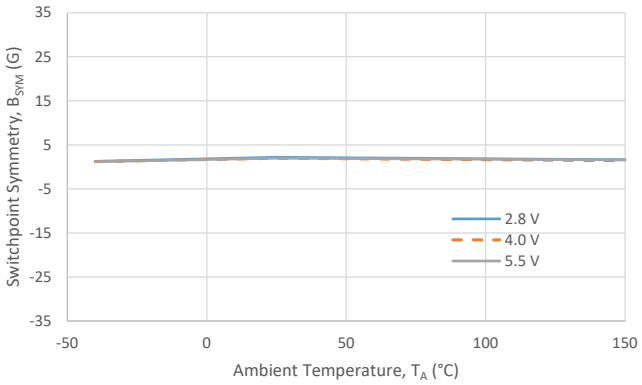
CHARACTERISTIC DATA

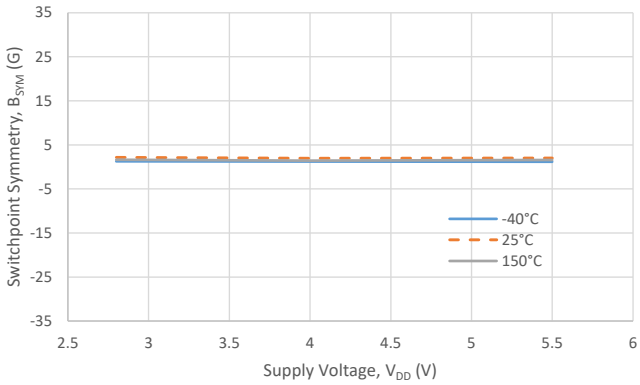
Magnetic Characteristics

Option B & C (ZX & ZY) with TC option A (flat) (continued)

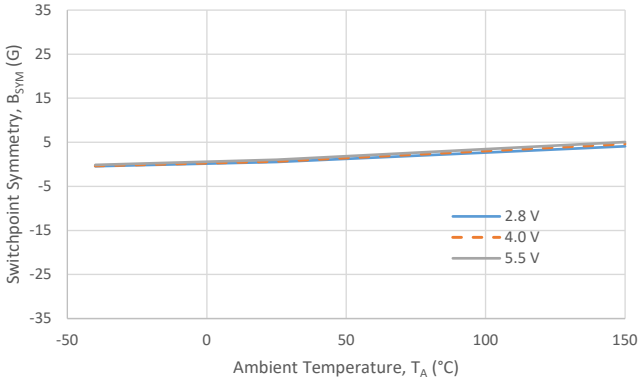
Symmetry (A) vs. Temperature



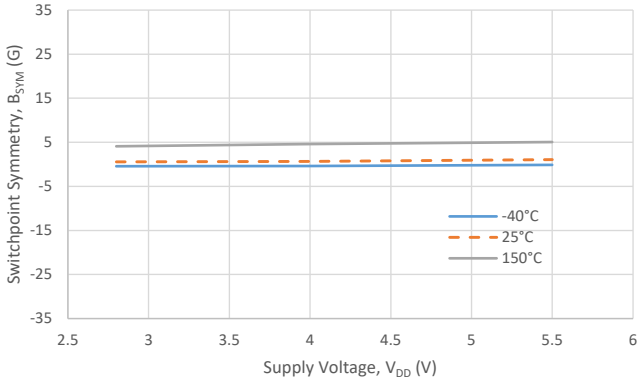
Symmetry (A) vs. Supply Voltage



Symmetry (B) vs. Temperature



Symmetry (B) vs. Supply Voltage



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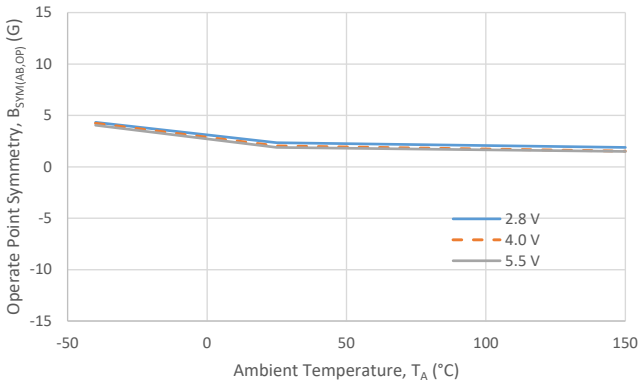
CHARACTERISTIC DATA

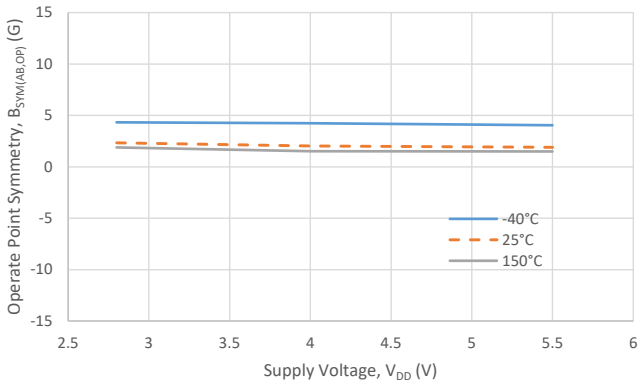
Magnetic Characteristics

Option B & C (ZX & ZY) with TC option A (flat) (continued)

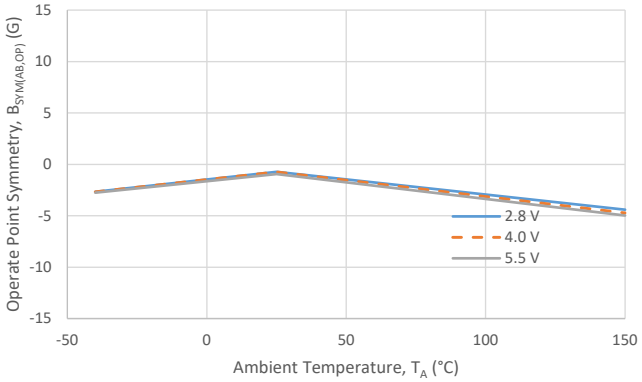
Operate Symmetry (AB) vs. Temperature



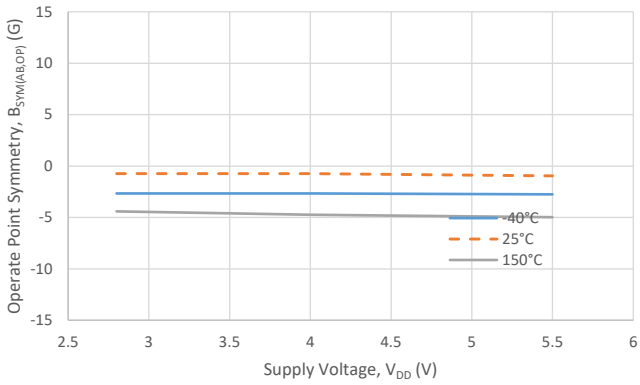
Operate Symmetry (AB) vs. Supply Voltage



Release Symmetry (AB) vs. Temperature



Release Symmetry (AB) vs. Supply Voltage



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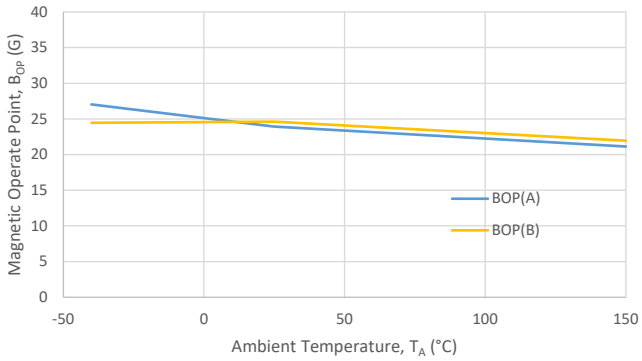
CHARACTERISTIC DATA

Magnetic Characteristics

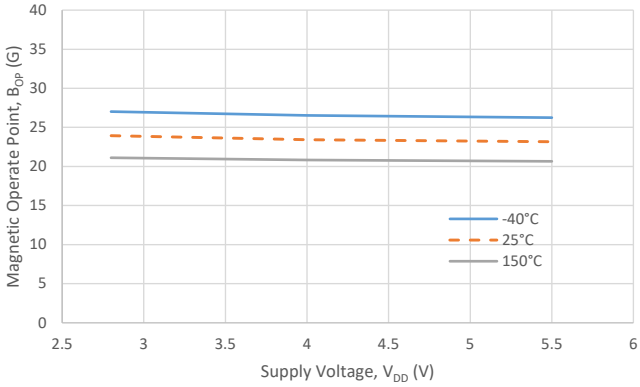
Option A (XY) with TC option F (ferrite)

Operate Point vs. Temperature

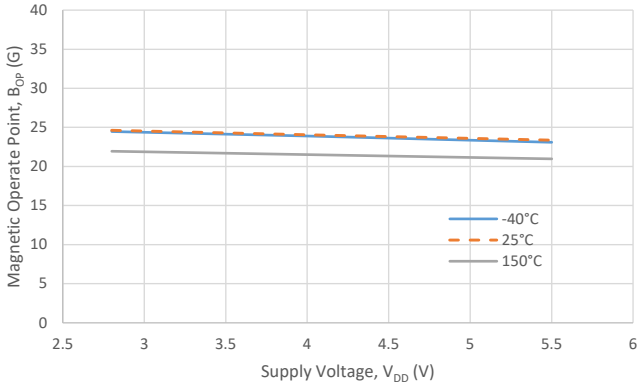
V_{DD} = 2.8 V



Operate Point (A) vs. Supply Voltage



Operate Point (B) vs. Supply Voltage



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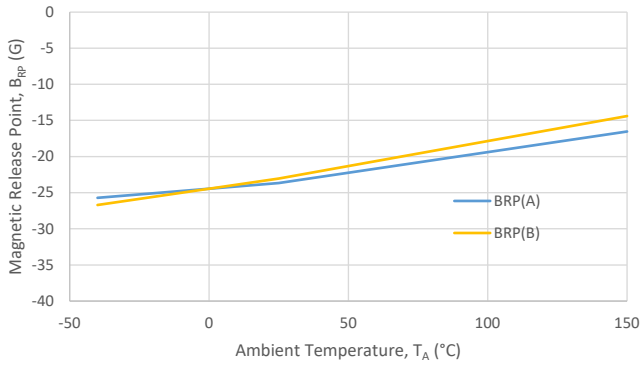
CHARACTERISTIC DATA

Magnetic Characteristics

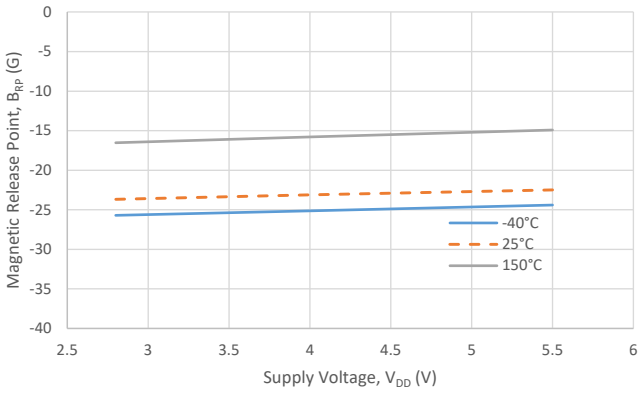
Option A (XY) with TC option F (ferrite) (continued)

Release Point vs. Temperature

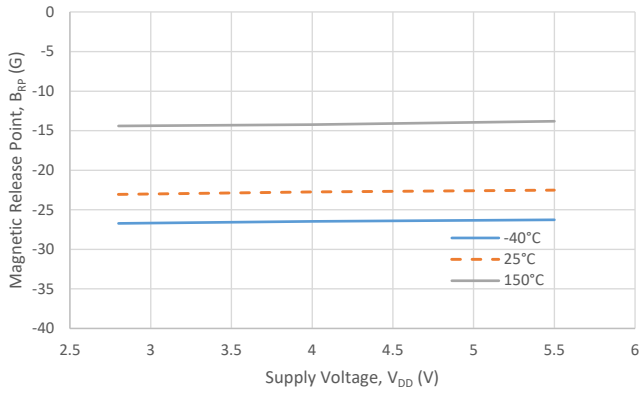
V_{DD} = 2.8 V



Release Point (A) vs. Supply Voltage



Release Point (B) vs. Supply Voltage



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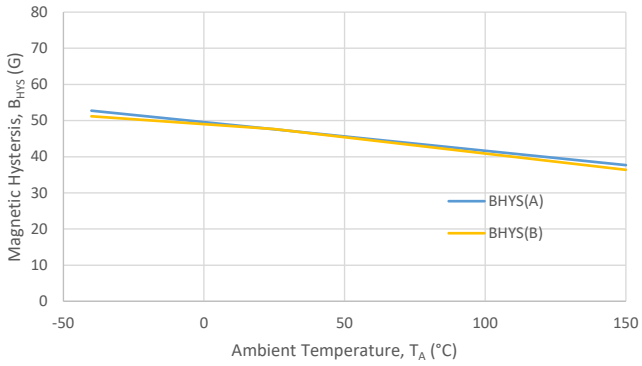
CHARACTERISTIC DATA

Magnetic Characteristics

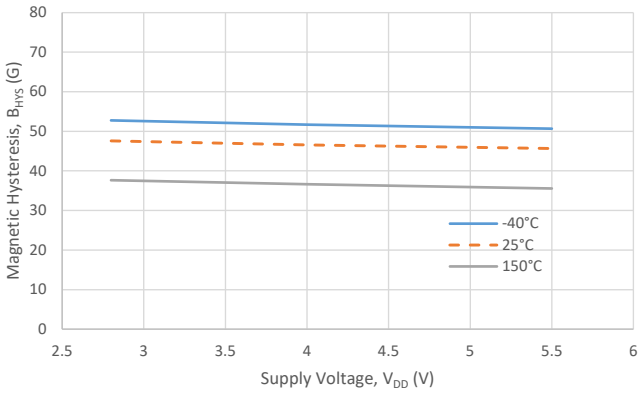
Option A (XY) with TC option F (ferrite) (continued)

Hysteresis vs. Temperature

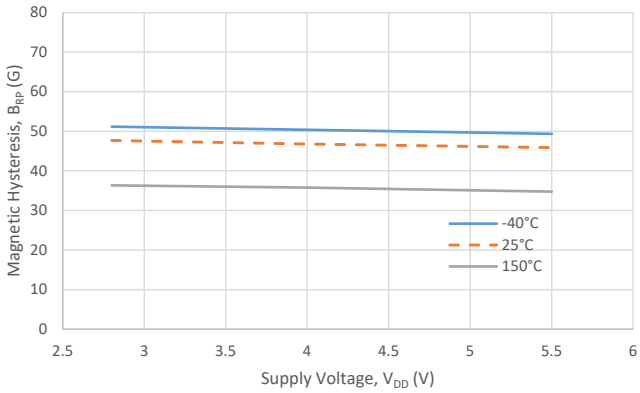
V_{DD} = 2.8 V



Hysteresis (A) vs. Supply Voltage



Hysteresis (B) vs. Supply Voltage



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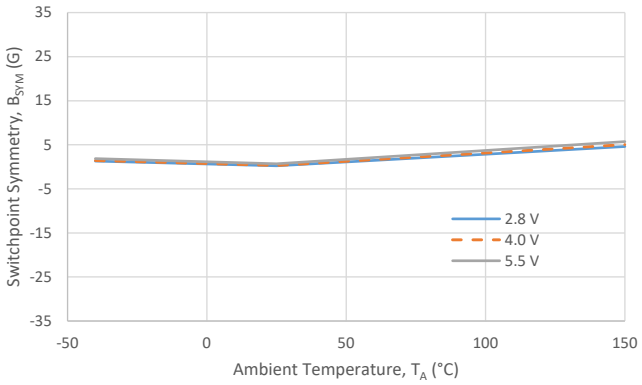
CHARACTERISTIC DATA

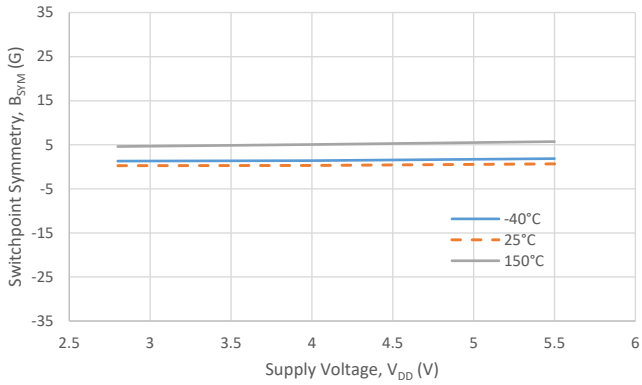
Magnetic Characteristics

Option A (XY) with TC option F (ferrite) (continued)

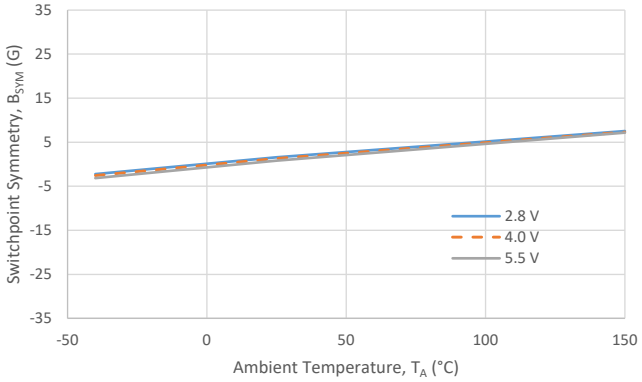
Symmetry (A) vs. Temperature



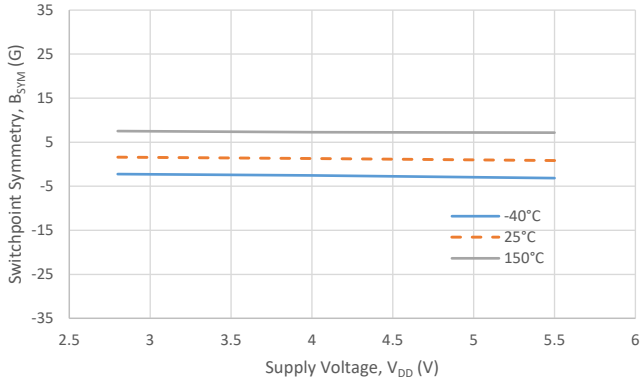
Symmetry (A) vs. Supply Voltage



Symmetry (B) vs. Temperature



Symmetry (B) vs. Supply Voltage



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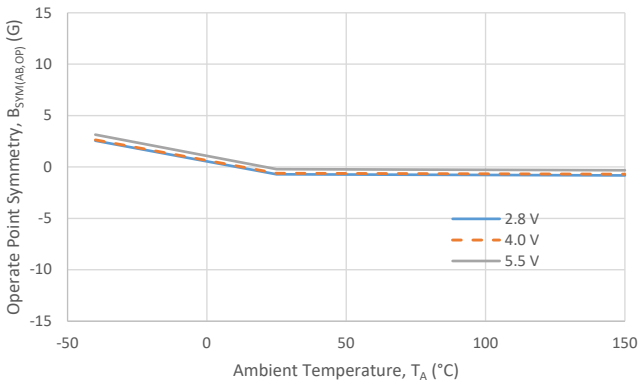
CHARACTERISTIC DATA

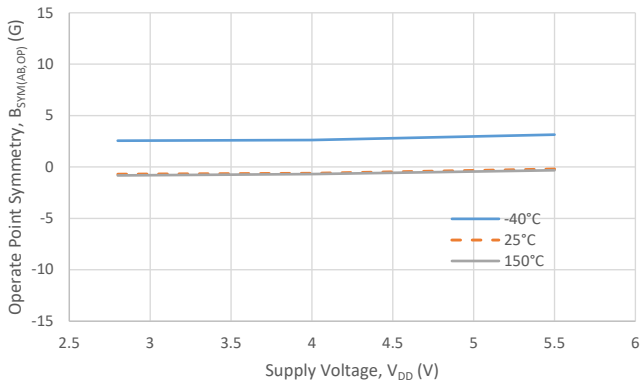
Magnetic Characteristics

Option A (XY) with TC option F (ferrite) (continued)

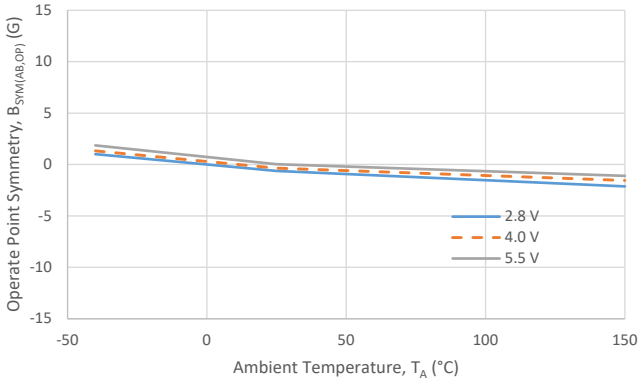
Operate Symmetry (AB) vs. Temperature



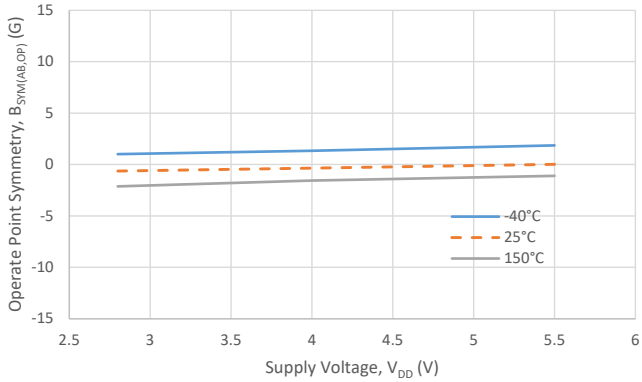
Operate Symmetry (AB) vs. Supply Voltage



Release Symmetry (AB) vs. Temperature



Release Symmetry (AB) vs. Supply Voltage



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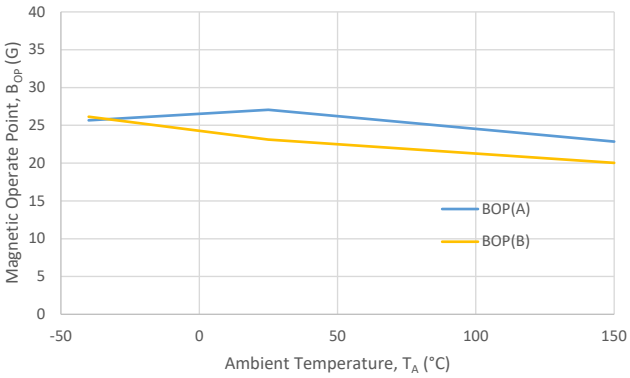
CHARACTERISTIC DATA

Magnetic Characteristics

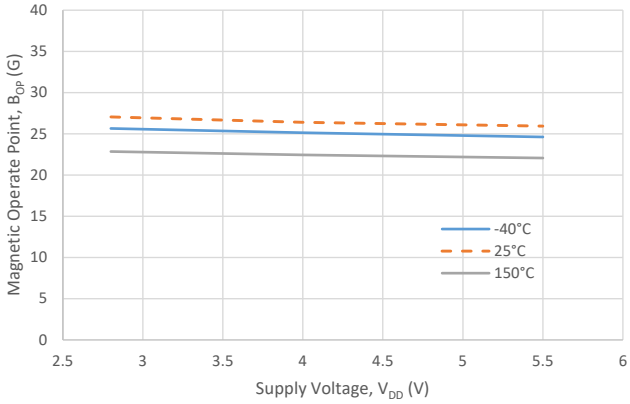
Option B & C (ZX & ZY) with TC option F (ferrite)

Operate Point vs. Temperature

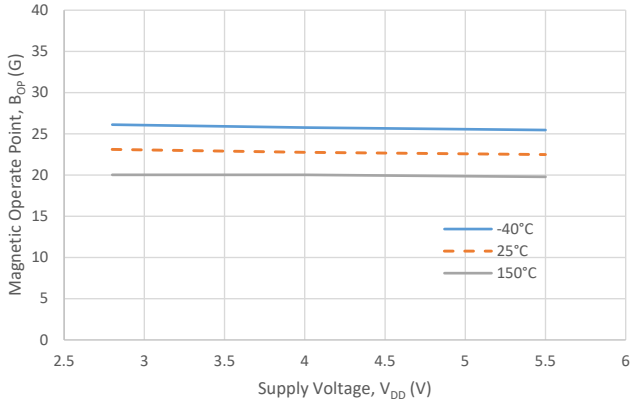
V_{DD} = 2.8 V



Operate Point (A) vs. Supply Voltage



Operate Point (B) vs. Supply Voltage



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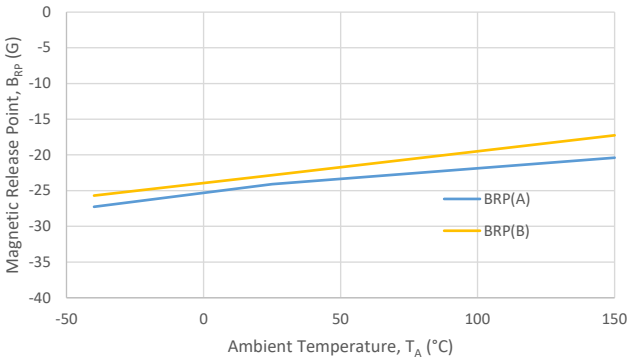
CHARACTERISTIC DATA

Magnetic Characteristics

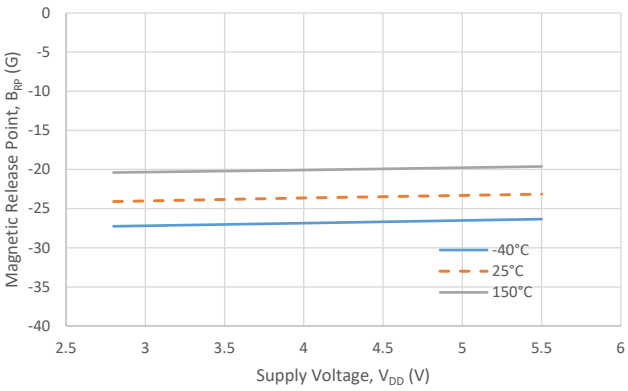
Option B & C (ZX & ZY) with TC option F (ferrite) (continued)

Release Point vs. Temperature

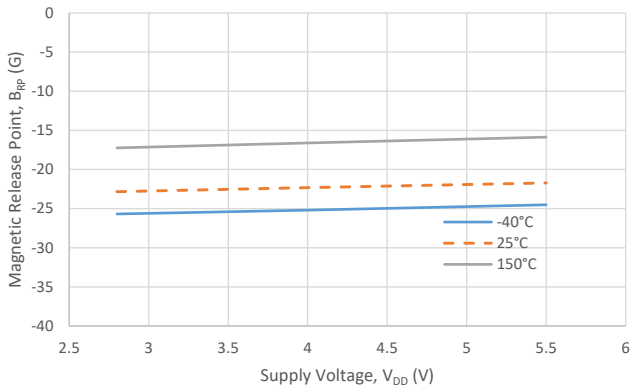
V_{DD} = 2.8 V



Release Point (A) vs. Supply Voltage



Release Point (B) vs. Supply Voltage



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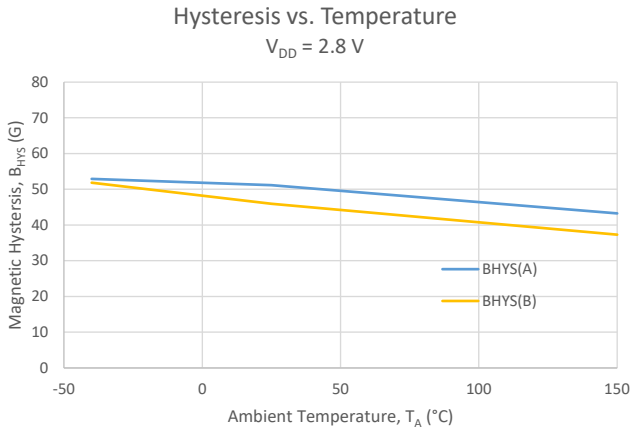
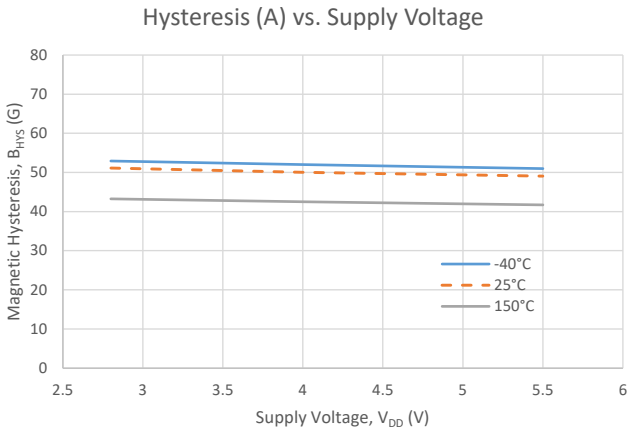
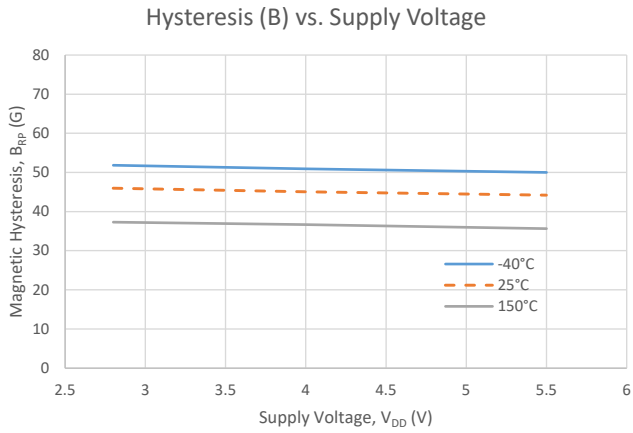
CHARACTERISTIC DATA

Magnetic Characteristics

Option B & C (ZX & ZY) with TC option F (ferrite) (continued)







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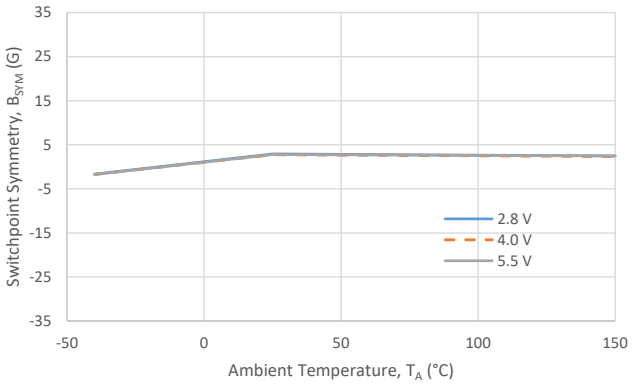
CHARACTERISTIC DATA

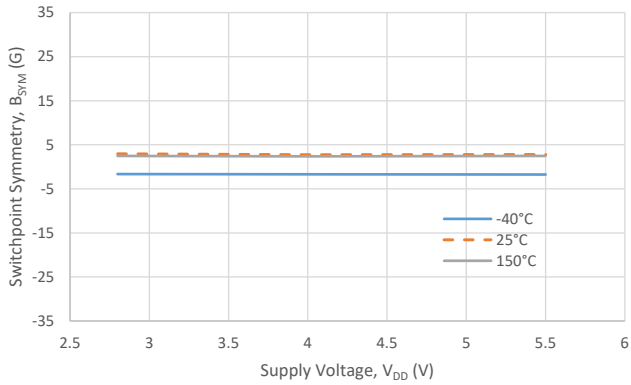
Magnetic Characteristics

Option B & C (ZX & ZY) with TC option F (ferrite) (continued)

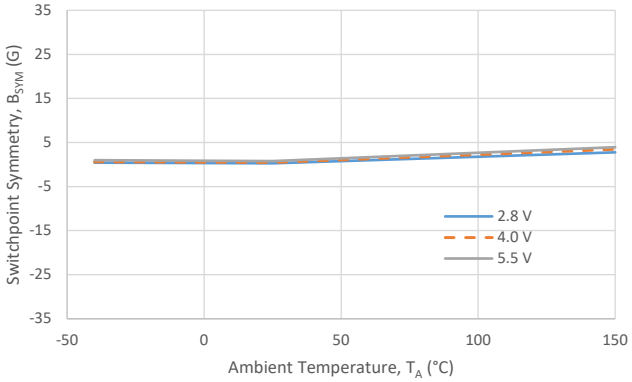
Symmetry (A) vs. Temperature



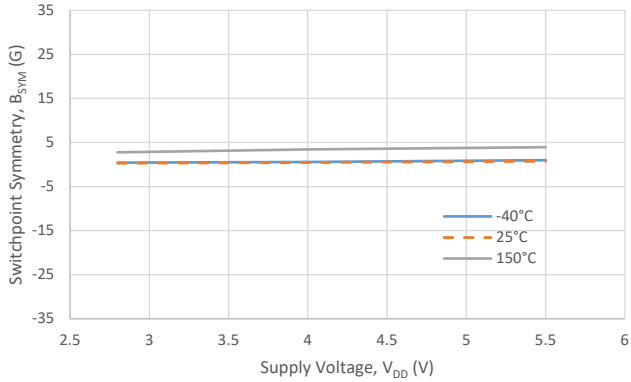
Symmetry (A) vs. Supply Voltage



Symmetry (B) vs. Temperature



Symmetry (B) vs. Supply Voltage



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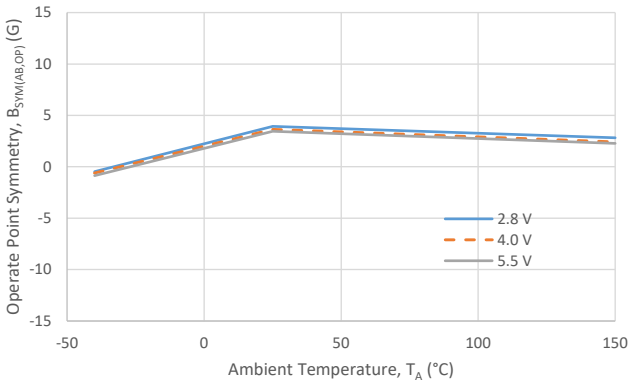
CHARACTERISTIC DATA

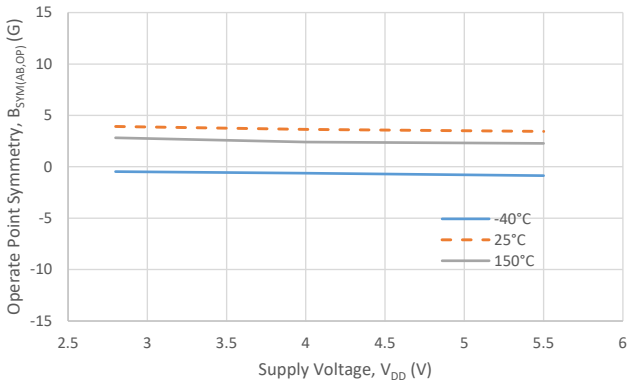
Magnetic Characteristics

Option B & C (ZX & ZY) with TC option F (ferrite) (continued)

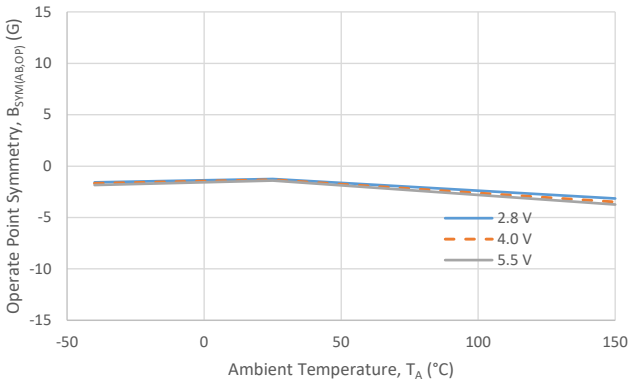
Operate Symmetry (AB) vs. Temperature



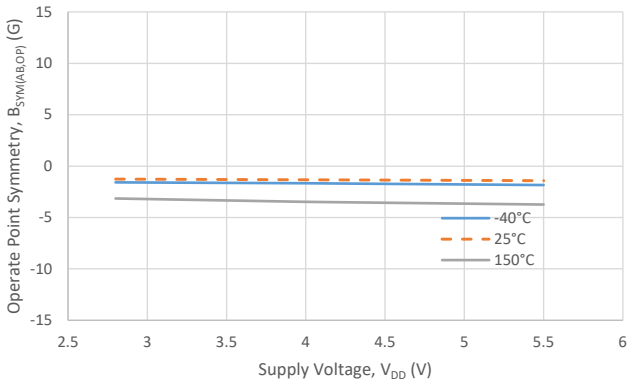
Operate Symmetry (AB) vs. Supply Voltage



Release Symmetry (AB) vs. Temperature



Release Symmetry (AB) vs. Supply Voltage



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FUNCTIONAL DESCRIPTION

2-Dimensional Sensing

With dual-planar Hall sensors, the ring magnet must be properly designed and optimized for the physical Hall element spacing (distance) to have the two channels in quadrature or 90 degrees out of phase. With the APS12625/6, which uses one planar and one vertical Hall-effect sensing element, or two vertical Hall-effect sensing elements perpendicular to one another, no target optimization is required. When the face of the IC is facing the ring magnet, the planar Hall senses the magnet poles and the vertical Hall senses the transition between poles; therefore, the two channels will inherently be in quadrature, regardless of the ring-magnet pole spacing. The same is true in the dual-vertical Hall configuration, with the vertical Hall element facing the magnet poles sensing the magnet IC poles and the other vertical Hall element sensing the transitions between poles. The quadrature relationship allows for the direction signal to be appropriately updated.

Outputs

SPEED AND DIRECTION

Internal logic circuitry of the APS12625 provides outputs representing the speed and direction of the magnetic field across the package.

The Speed (SPD) output is the XOR of the output of the two active Hall elements, providing two times the resolution of a single channel, while the direction (DIR) output provides the direction of the target. The direction output, DIR, is always updated before SPD, according to $t_{dir\text{-}to\text{-}speed}$. It is updated on every transition of either Hall sensor, allowing the use of up-down counters without loss of pulses.

QUADRATURE

The APS12626 offers individual outputs of the two active Hall sensors, referred to here as Channel A and Channel B. The Output Option Table indicates which Hall sensing element corresponds to “Channel A” and “Channel B” in each configuration.

The Channel A and Channel B outputs of the APS12626 switch low (turn on) when the corresponding Hall element is presented with a perpendicular south magnetic field of sufficient strength ($>B_{OP}$). The device outputs switch high (turn off) when the strength of a perpendicular north magnetic field exceeds the release point (B_{RP}). The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device. See Figure 1.

Removal of the magnetic field will leave the device output latched on if the last crossed switchpoint is B_{OP}, or latched off if the last crossed switchpoint is B_{RP}.

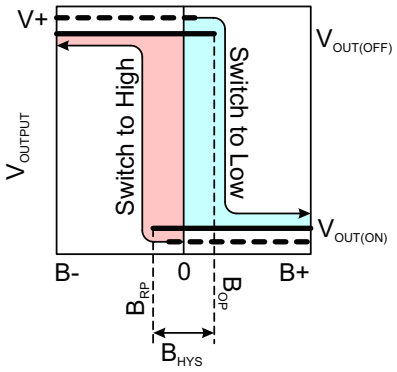

Figure 1: Switching Behavior of Latches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity)

This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The outputs will power-on in the high output state, even when powering-on in the hysteresis region, between B_{OP} and B_{RP} for both versions of the device, with and without the power-on state setting feature.

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Operation

With dual-planar Hall sensors, the ring magnet must be properly designed and optimized for the physical Hall spacing (distance) for the outputs of the two latches to be in quadrature, or 90 degrees out of phase. With the APS12625 and APS12626, no target optimization is required. When the face of the IC is facing the ring magnet, the planar Hall senses the magnet poles and the vertical Hall senses the transition between poles; therefore, the two channels will inherently be in quadrature, regardless of the ring-magnet pole spacing.

Figure 2 shows a ring magnet optimized for the E1-to-E2 spacing of a dual-planar sensor, resulting in quadrature, or 90 degrees phase separation between channels. This same target also results in quadrature for the 2D sensing APS12625/6. However when a different ring magnet is used which is not optimized for the E1-to-E2 spacing, the dual-planar sensor exhibits diminished phase separation, making signal processing the outputs into speed and direction less robust. Using a different ring-magnet geometry has no effect on the APS12625/6, and the two channels remain in quadrature (see Figure 3).

The relationship of the various signals and the typical system timing is shown in Figure 4.

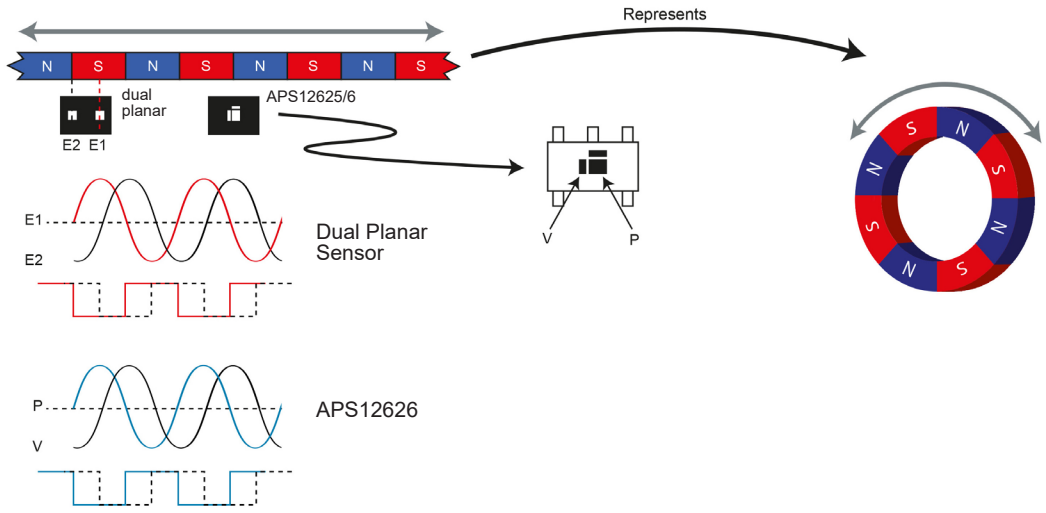

Figure 2: Ring magnet optimized for a dual-planar Hall-effect sensor resulting in output quadrature also results in quadrature for the APS12625/6.

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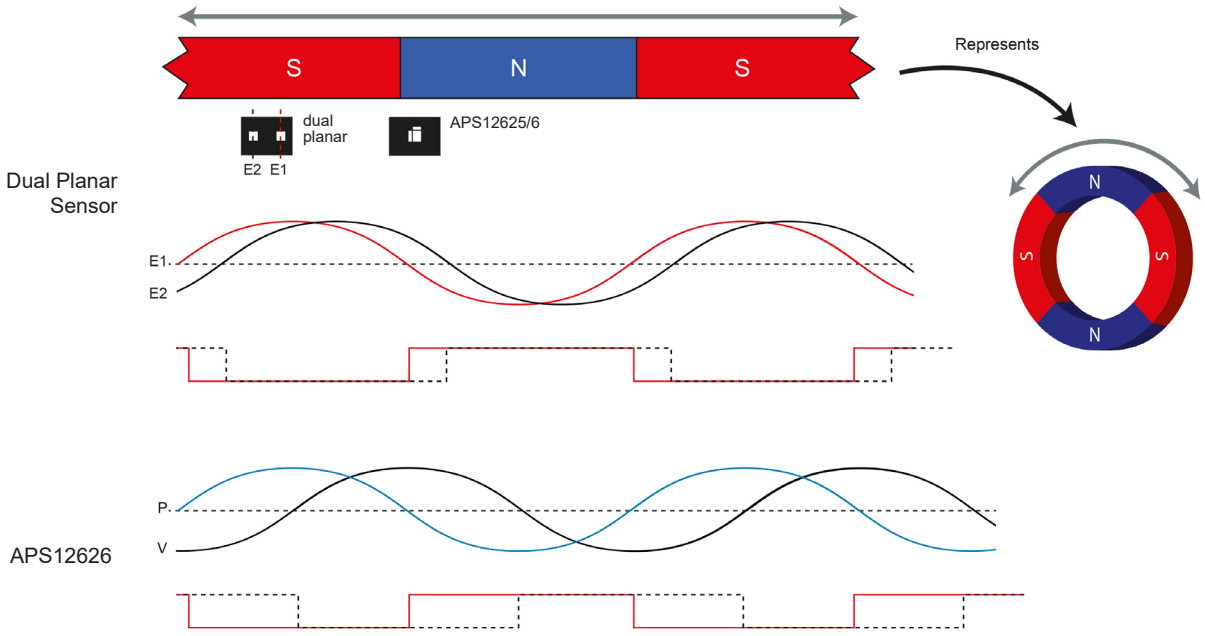

Figure 3: Ring magnet not optimized for a dual-planar Hall-effect sensor resulting in significantly reduced output phase separation, however still results in quadrature for the APS12625/6.

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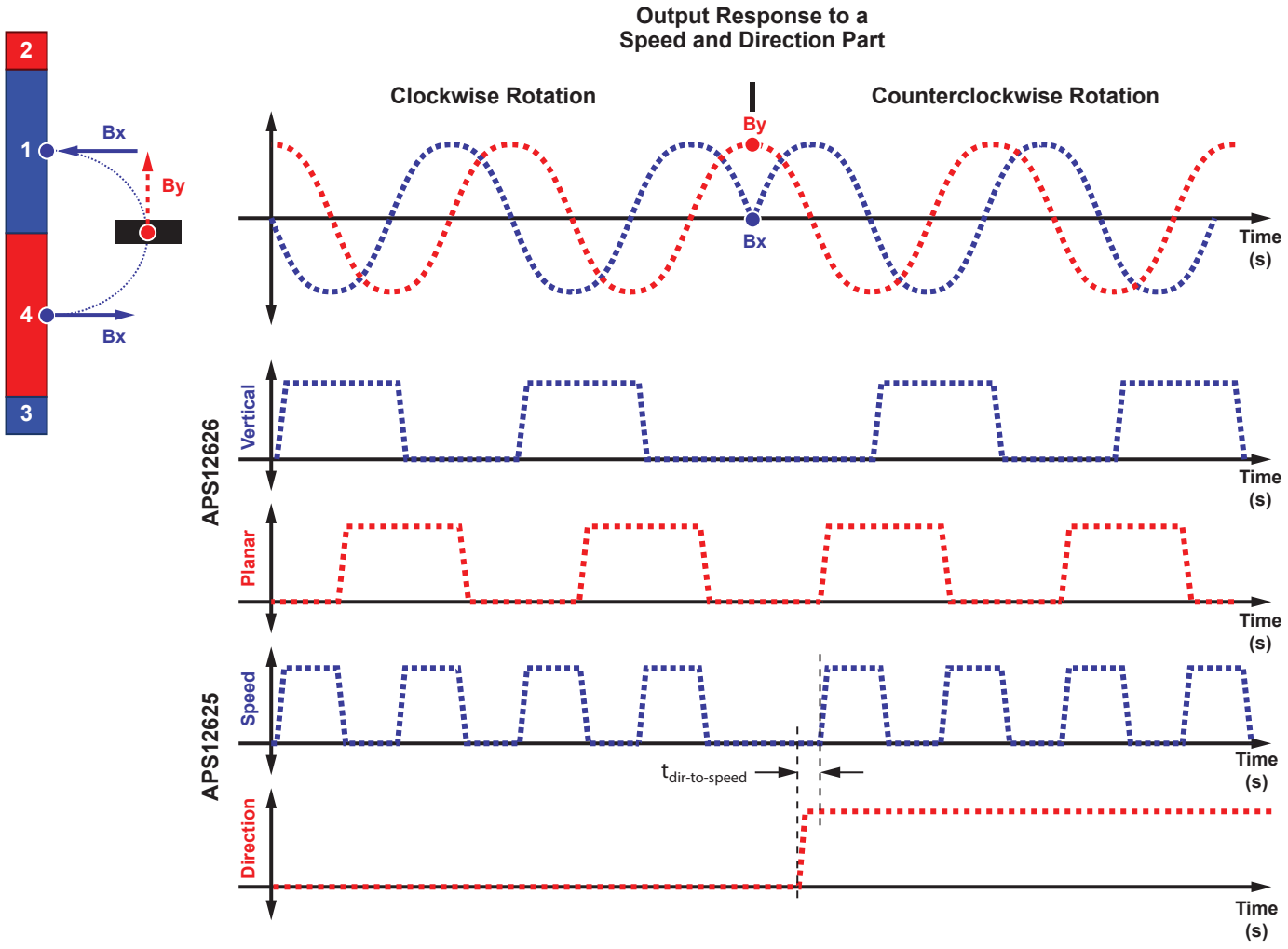

Figure 4: Typical System Timing

The two active Hall signals represent the magnetic input signal, which is converted to the device outputs, OUTPUTA and OUTPUTB, respectively for the Quadrature Output configuration. If the Speed and Direction option is selected, the outputs will reflect Direction and Speed. The Direction output will update before Speed output by $t_{dir\text{-}to\text{-}speed}$. Only one case is shown above; however, the Direction output will indicate a direction change after any one channel has two consecutive output transitions without the other channel having any output transitions.

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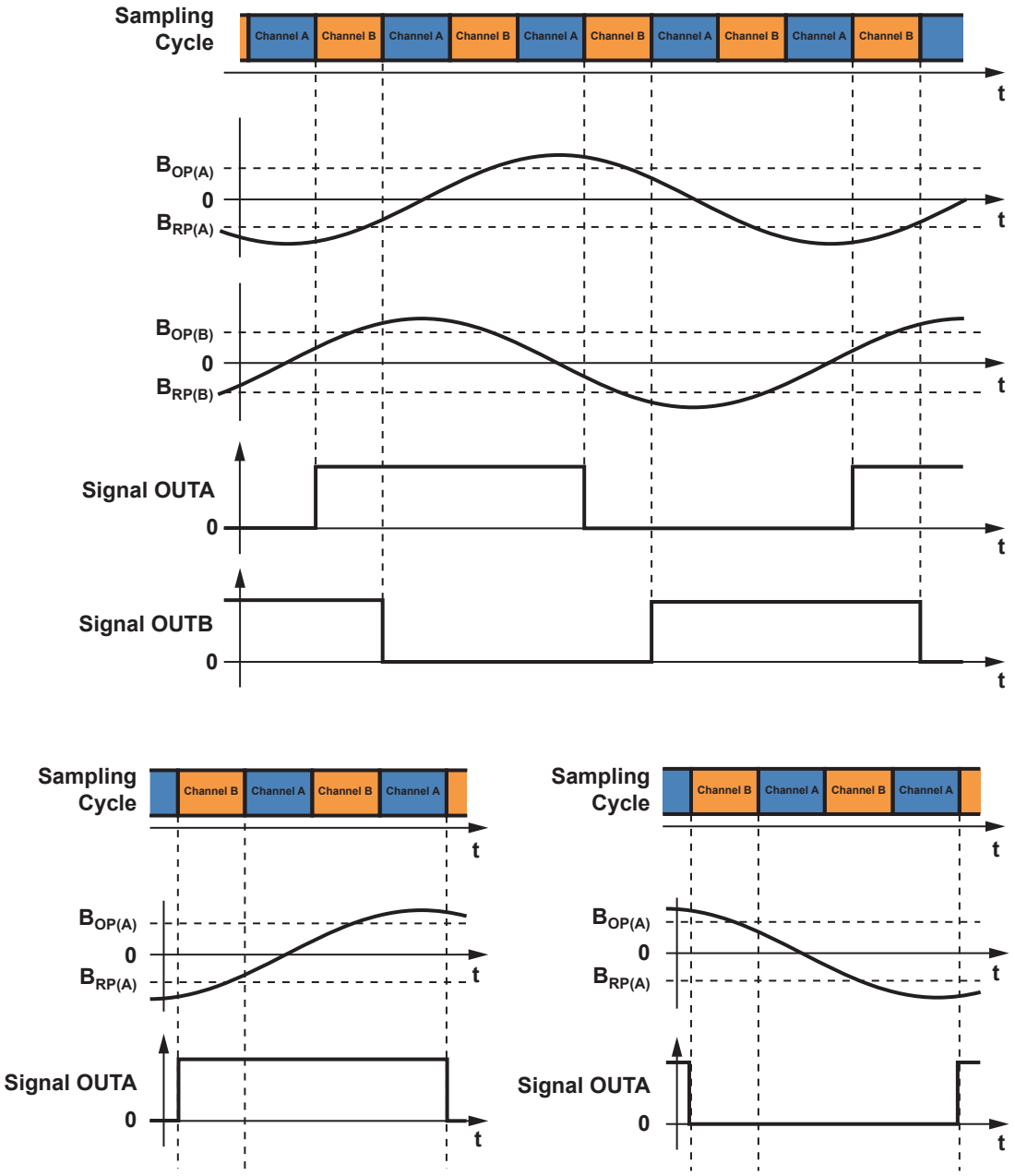

Figure 5: Output signal updating with respect to the channel sampling

The two active channels are multiplexed with a typical 20 µs sampling period per channel. If the magnetic signal crosses the respective B_{OP} or B_{RP} of a particular channel, that channel's output will not be updated until the end of its sampling period. If the signal crosses the thresholds while the alternate channel is sampling, the update will occur at the end of the next sampling period (as long as the signal does not cross back over the thresholds). This is illustrated in Figure 5. The sampling error introduced by the multiplexing increases with magnetic input frequency, which can affect the output duty cycle and phase separation between outputs. Contact your Allegro field applications engineer (FAE) for more information regarding suitability to high frequency applications.

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APS12625/6 Sensor and Relationship to Target

There are no output options for the APS12625; it is always Speed/Direction. The APS12626 has A/B outputs. Additionally, each device is available in 3 different sensing configurations, with X-axis vertical Hall and Y-axis vertical Hall active, with Z-axis planar Hall and the X-axis vertical Hall active, or with the Z-axis planar Hall and the Y-axis vertical Hall active. This offers incredible flexibility for positioning the IC within various applications.

Axes option A (X-Y) supports having the IC positioned with the face of the package in-plane with the ring magnet from either the leadless (Figure 6a) or leaded (Figure 6b) sides of the package.

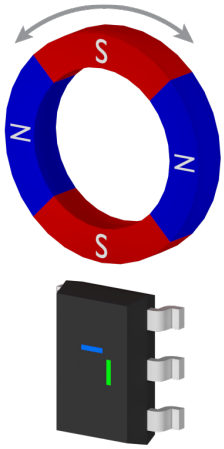

Figure 6a

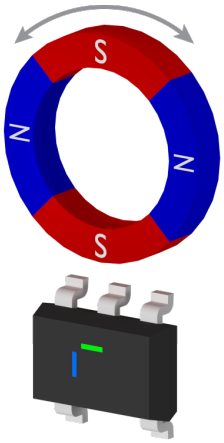

Figure 6b

Axes option B (Z-X) supports having the IC positioned with the face of the package facing the ring magnet, and the axis of rotation (Figure 7a) lengthwise along the package body, or with either of the non-leaded sides of the package facing the ring magnet (Figure 7b). This latter configuration has the advantage of being able to be mounted extremely close to the ring magnet, since there are no leads or solder pads to accommodate in that dimension.

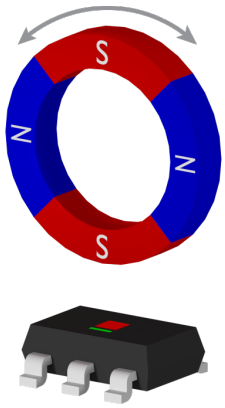

Figure 7a

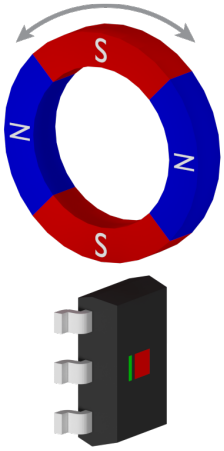

Figure 7b

Axes option C (Z-Y) supports the traditional configuration with the face of the package facing the ring magnet (Figure 8a), with the axis of rotation going across the leads, or with either of the leaded sides of the package facing the ring magnet (Figure 8b).

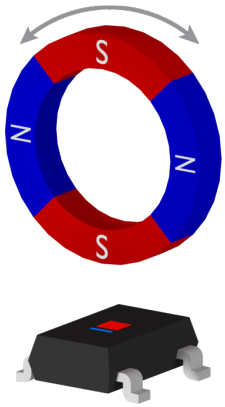

Figure 8a

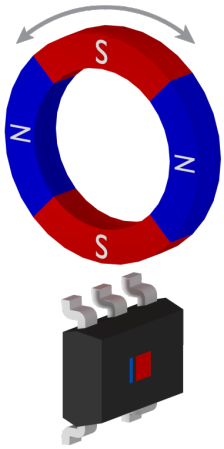

Figure 7b

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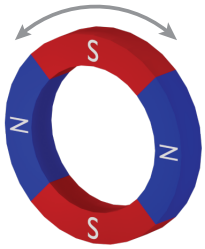
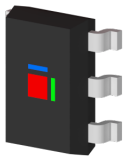
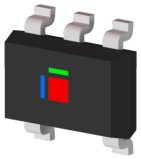
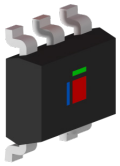
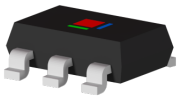
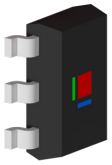
Table 1 : APS12625 Sensor and Relationship to Target

	IC and Relationship to Target	State of Direction Output	
Target		**Clockwise**	**Counterclockwise (anticlockwise)**
XY		High	Low
		High	Low
ZY		Low	High
		Low	High
ZX		High	Low
		High	Low

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Temperature Coefficient and Magnet Selection

The APS12625/6 allows the user to select the magnetic temperature coefficient to compensate for the drift of SmCo and ferrite magnets over temperature, as indicated in the specifications table on page 5. This compensation improves the magnetic system performance over the entire temperature range. For example, the magnetic field strength from ferrite decreases as the temperature increases from 25°C to 150°C. This lower magnetic field strength means that a lower switching threshold is required to maintain switching at the same distance from the magnet to the sensor. Correspondingly, higher switching thresholds are required at cold temperatures, as low as –40°C, due to the higher magnetic field strength from the ferrite magnet. The APS12625/6 compensate the switching thresholds over temperature as described above. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.

For example, the typical ferrite compensation is –0.17%/°C. With a 25°C temperature B_{OP} switchpoint of 25 G, the switchpoint changes nominally by –0.17%/°C × 25 × (150°C – 25°C) = –5.3 G to 25 G – 5.3 G = 19.7 G at 150°C. And at –40°C, the switchpoint changes by –0.17%/°C × 25 × (–40°C – 25°C) = 2.8 G to 25 G + 2.8 G = 27.8 G.

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Power-On Sequence and Timing

NON-*P* OPTION

The default power-on state has been achieved when the supply voltage is within the specified operating range ($V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$) and the power-on time has elapsed ($t > t_{ON}$). Refer to Figure 9: Power-On Sequence and Timing for an illustration of the power-on sequence.

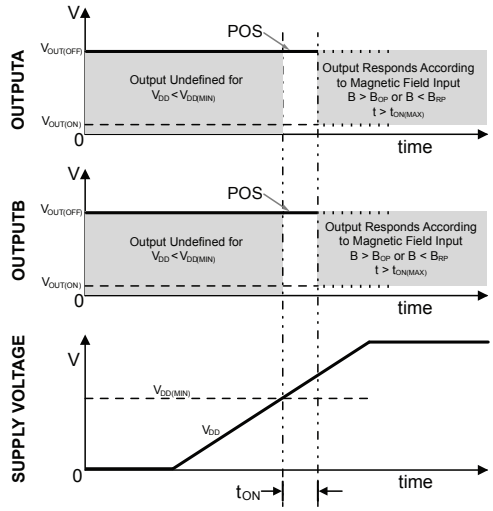

Figure 9: Power-On Sequence and Timing

Once the supply voltage is within the operational range, the outputs will be in the high state (power-on state), regardless of the magnetic field. The outputs will remain high until the sensor is fully powered on ($t > t_{ON}$)—note that the vertical Hall channel typically responds before the planar Hall channel.

-*P* OPTION

For the –*P* option device (user/externally set power-on state), the power-on sequence is similar to the default with the exception that if either of the outputs have input field in the hysteresis band, the output state can be externally set low with a low setting pulse.

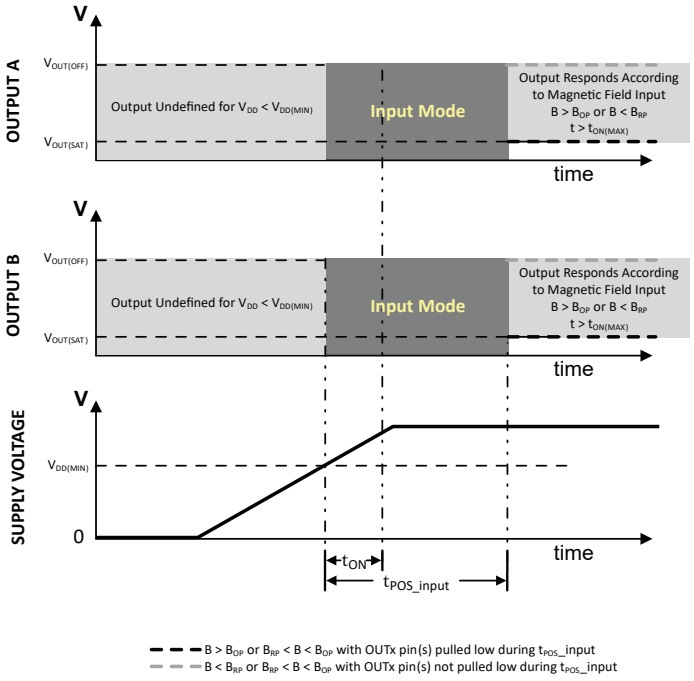

Figure 10: Power-On Sequence and Timing, -P option

If the desired power-on state is high, the user should not input a power-on state pulse. The outputs will default to the high state until the device is fully powered on.

If the desired power-on state is low, the user should input a low output state setting pulse for at least t_{POS_input}. The output will switch low after t_{ON} if the field level is within the hysteresis band ($B_{RP} < B < B_{OP}$). For the APS12625-P, the power-on state can only be set on the Speed output (OUTPUT A).

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Setting the Power-On State (-P option only)

The power-on state can be set by the host so that when the sensor is being power-cycled for power savings, the outputs can be restored to the desired state. The start-up flow for quadrature outputs (APS12626) is shown in Figure 11, and the flow for speed and direction outputs (APS12625) is shown in Figure 12.

APS12626

When the sensor powers on, each channel assumes an output state based on the input magnetic field present at the time, unless the field level is within the hysteresis band. In that case (field within hysteresis band), the output can be forced low externally during the time where no conclusive field is seen by the sensor. The forcing signal needs to be provided for more than 100 µs, the minimum Power-On State External Input time (t_{POS_input}). The state of each channel will be copied by the sensor.

This allows setting a wake-up state that is consistent with the shutdown state, thus avoiding errors in the total pulse count. If the target starts moving before $t > t_{POS\_input}$, the desired wake-up state may not be correctly set. The sensor will exit POS mode once either of the output channels has an output transition (i.e. sufficient target movement).

Channels A and B are set independently of one another.

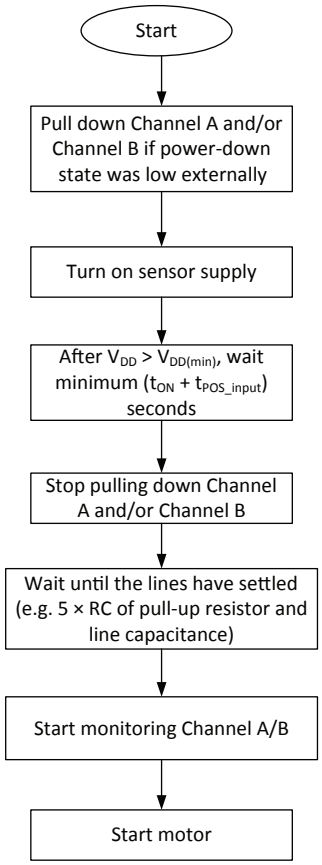

Figure 11: Output setting at power-on, dual quadrature outputs (APS12626)

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APS12625

For the Speed and Direction option (APS12625), when the sensor powers-on, the Speed output is set as A XOR B, and Direction is in the high state until a transition on internal channels A or B has been seen.

If one of the channels wakes up with the magnetic input field in the hysteresis band, then it is possible to set the speed pin value to be consistent with the state at shutdown. A default value of high will be assumed by the sensor, unless a low state-setting pulse is seen during t_{POS_input}. If the target starts moving before $t > t_{POS\_input}$, the desired wake-up state may not be correctly set. The forcing signal needs to be provided for more than 100 µs, the minimum Power-On State External Input time (t_{POS_input}). The sensor will exit POS mode once either of the output channels has an output transition (i.e. sufficient target movement).

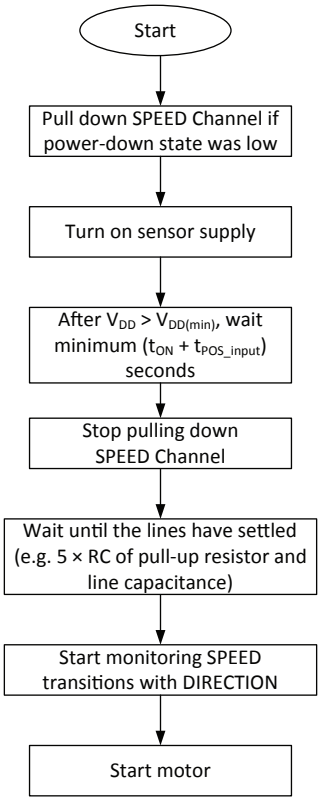

Figure 12: Output setting at power-on, Speed and Direction (APS12625)

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Functional Safety

The APS12625/6 was designed in accordance with the international standard for automotive functional safety, ISO 26262:2011. This product achieves an ASIL (Automotive Safety Integrity Level) rating of ASIL A according to the standard. The APS12625/6 is classified as a SEOoC (Safety Element Out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. Contact your local FAE for A²-SIL™ documentation: www.allegromicro.com/ASIL.

The APS12625/6 has internal diagnostics to check the voltage supply (an undervoltage lockout regulator).

Applications

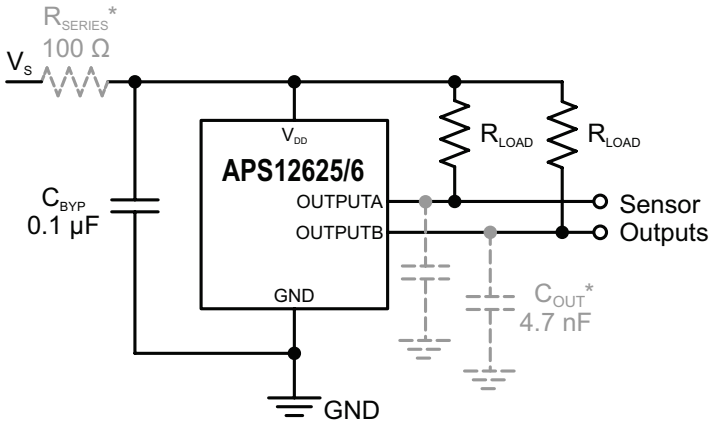
An external bypass capacitor must be connected (in close proximity to the Hall sensor) between the supply and ground of the device to guarantee correct performance and to reduce noise from internal circuitry. As shown in Figure 13, a 0.1 µF capacitor is typical. If the application requires additional EMC protection, additional components are suggested in gray in the same figure.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices, AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*
- *Air-Gap-Independent Speed and Direction Sensing Using the Allegro A1262, AN296124*
- *Improved Speed and Direction Sensing Using Vertical Hall Technology, AN296130*

All are provided on the Allegro website:

www.allegromicro.com



* Optional components for enhanced EMC protection.

Figure 13: Typical Application Circuit

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a proven approach used to minimize Hall offset on the chip.

The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain through modulation.

The subsequent demodulation acts as a modulation process for the offset, causing the magnetic-field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic signal then can pass through a low-pass filter, while the modulated DC offset is suppressed.

The chopper stabilization technique uses a high frequency clock, generally at hundreds of kilohertz. A sample-and-hold technique is used for demodulation, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

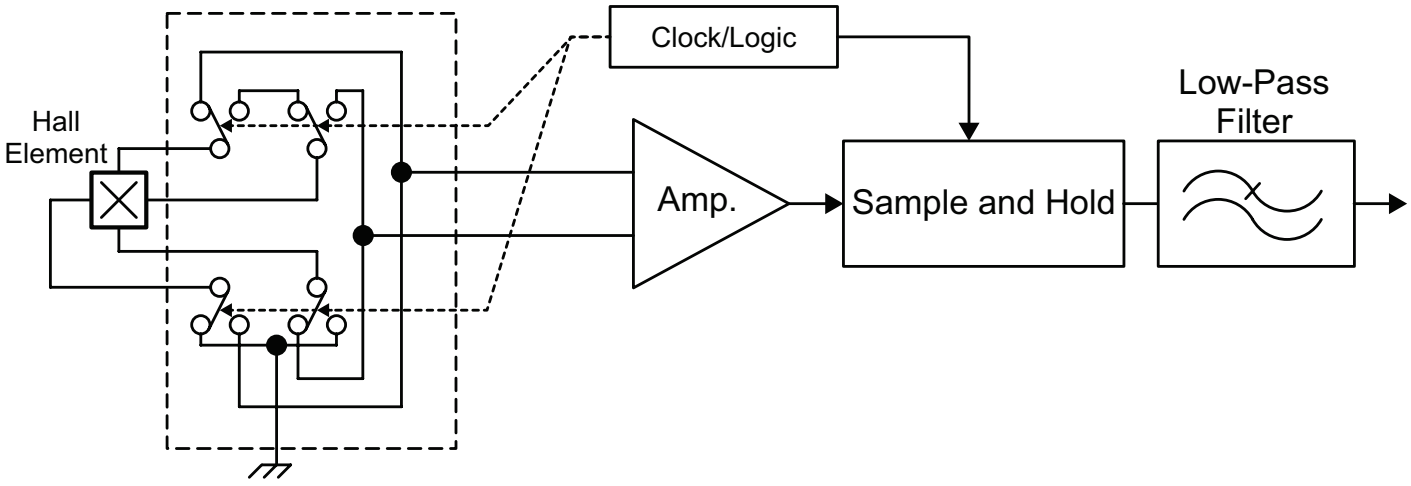

Figure 14: Model of Chopper Stabilization Technique

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A = 25°C, V_{DD} = 5 V, I_{DD} = 3 mA, and $R_{\theta JA}$ = 124°C/W for the LH-5 package, then:

$$P_D = V_{DD} \times I_{DD} = 5\ V \times 3\ mA = 15\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 15\ mW \times 124°C/W = 1.9°C$$

$$T_J = T_A + \Delta T = 25°C + 1.9°C = 26.9°C$$

A worst-case estimate ($P_{D(max)}$) represents the maximum allowable power level ($V_{DD(max)}$, $I_{DD(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{DD} at T_A = 150°C, package LH-5, using low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 124°C/W, $T_{J(max)}$ = 165°C, $V_{DD(max)}$ = 5.5 V, and $I_{DD(max)}$ = 4.5 mA.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 124°C/W = 121\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{DD(est)} = P_{D(max)} \div I_{DD(max)}$$

$$V_{DD(est)} = 121\ mW \div 4.5\ mA$$

$$V_{DD(est)} = 26.9\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{DD(est)}$.

Compare $V_{DD(est)}$ to $V_{DD(max)}$. If $V_{DD(est)} \le V_{DD(max)}$, then reliable operation between $V_{DD(est)}$ and $V_{DD(max)}$ requires enhanced $R_{\theta JA}$. If $V_{DD(est)} \ge V_{DD(max)}$, then operation between $V_{DD(est)}$ and $V_{DD(max)}$ is reliable under these conditions.

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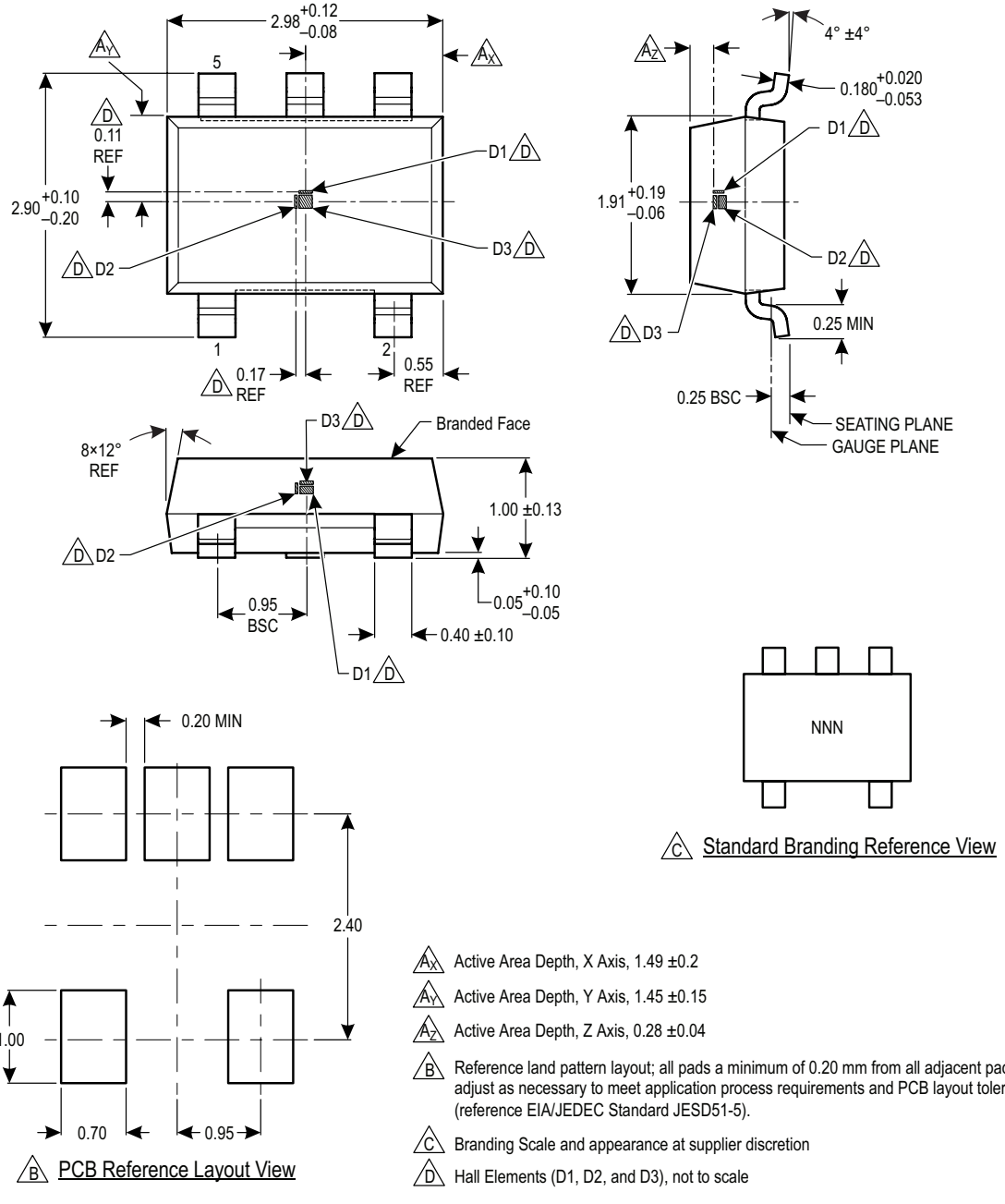
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-9069)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Ax Active Area Depth, X Axis, 1.49 ±0.2

Ay Active Area Depth, Y Axis, 1.45 ±0.15

Az Active Area Depth, Z Axis, 0.28 ±0.04

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances (reference EIA/JEDEC Standard JESD51-5).

C Branding Scale and appearance at supplier discretion

D Hall Elements (D1, D2, and D3), not to scale

Figure 15: Package LH, 5-Pin SOT23-W

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Revision History

Number	Date	Description
–	November 15, 2017	Initial release
1	December 19, 2018	Updated Figure 10 and other minor editorial updates
2	January 9, 2020	Minor editorial updates

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