APS11900

Two-Wire End-of-Line Programmable Hall-Effect Switch/Latch

FEATURES AND BENEFITS

- ASIL A functional safety
  - Developed in accordance with ISO 26262:2011 (pending assessment)
  - Internal diagnostics and a defined Safe State
  - A^2-SIL™ documentation available
- Highly programmable
  - Magnetic polarity, switch points, and hysteresis
  - Temperature coefficient (supports SmCo, NdFeB, and ferrite magnets)
  - Output polarity and current levels
- Reduces module bill of materials (BOM) and assembly cost
  - Integrated overvoltage clamp (40 V load dump) and reverse-battery diode
  - Integrated series resistor and bypass capacitor (UC package)
  - Enables PCB-less sensor modules
- Automotive-grade ruggedness and fault tolerance
  - Extended AEC-Q100 qualification
  - Operation from –40°C to 175°C junction temperature
  - 3 to 24 V operating voltage range
  - High EMC/ESD immunity
  - Overtemperature indication

PACKAGES

3-pin SOT23-W (LH) 3-pin ultramini SIP (UA) 3-pin SIP (UC)

Not to scale

DESCRIPTION

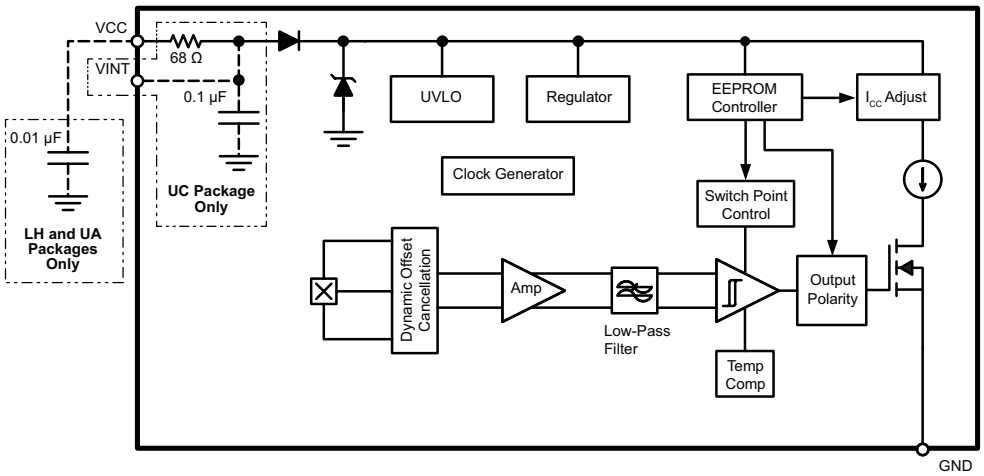
APS11900 devices are highly programmable, two-wire planar Hall-effect sensor integrated circuits (ICs) developed in accordance with ISO 26262:2011 (pending assessment). They include internal diagnostics and support a functional safety level of ASIL A. The enhanced two-wire current-mode interface provides interconnect open/short diagnostics and adds a Safe State to communicate diagnostic information while maintaining compatibility with legacy two-wire systems. Two-wire sensors are well-suited to safety applications, especially those involving long wire harnesses.

Programming can be performed at end of line to optimize the sensor on a per unit or per module basis. The user can select the magnetic switch points, temperature coefficient, and hysteresis, and whether the device responds to north or south magnetic fields (unipolar switch) or both (bipolar latch or omnipolar switch). The response can be matched to SmCo, NdFeB, or low-cost ferrite magnets. There is a choice of two output current levels and either output polarity. In addition to a benchtop programmer (ASEK) for development and evaluation, universal software drivers are available to facilitate programming in a production environment.

Continued on the next page…

TYPICAL APPLICATIONS

- Automotive and industrial safety systems
- Seat position detection
- Seat belt buckles
- Hood/trunk/door latches
- Sunroof/convertible top/tailgate/liftgate actuation
- Brake/clutch pedals
- Electric power steering (EPS)
- Transmissions and shift selectors
- Wiper motors



Functional Block Diagram

DESCRIPTION (continued)

APS11900 sensors are engineered to operate in the harshest environments with minimal external components. They are qualified beyond the requirements of AEC-Q100 Grade 0 and will survive extended operation at 175°C junction temperature. These monolithic ICs include on-chip reverse-battery protection, overvoltage protection (40 V load dump), ESD protection, overtemperature detection, and an internal voltage regulator for operation directly from an automotive battery bus. These integrated features reduce the end-product bill-of-materials (BOM) and assembly cost.

The available SIP package with integrated discrete components (UC) enables PCB-less applications by incorporating all of the EMC protection components into the IC package. Other package options include industry-standard surface-mount SOT (LH) and through-hole SIP (UA) packages. All three packages are RoHS-compliant and lead (Pb) free with 100% matte-tin-plated leadframes.

For situations where a functionally equivalent but factory-programmed two-wire switch or latch is preferred, refer to the APS11500 and APS12400 device families, respectively.

SELECTION GUIDE

Part Number	Package	Packing [1]	Operating Ambient Temperature, T_A (°C)
APS11900LLHALT	3-pin SOT23-W surface mount	7-inch reel, 3000 pieces/reel	–40 to 150
APS11900LLHALX	3-pin SOT23-W surface mount	13-inch reel, 10000 pieces/reel	
APS11900LUAA	3-pin SIP through-hole	Bulk, 500 pieces/bag	
APS11900LUCDTN	3-pin SIP through-hole with integrated passive components	13-inch reel, 4000 pieces/reel	

[1] Contact Allegro for additional packing options.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage [1]	V_{CC}		40	V
Reverse Supply Voltage	V_{RCC}		–23	V
Magnetic Flux Density	B		Unlimited	G
Maximum Number of EEPROM Write Cycles	EEPROMW(max)		100	cycles
Maximum Junction Temperature	T_J(max)		165	°C
		For 500 hours	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] This rating does not apply to extremely short voltage transients such as load dump and/or ESD. Those events have individual ratings specific to the respective transient voltage event. Contact your local field applications engineer for information on EMC test results.

INTERNAL DISCRETE COMPONENT RATINGS (UC Package Only)

Component	Symbol	Test Conditions	Characteristics				
			Rated Nominal Resistance/Capacitance	Rated Voltage	Rated Tolerance	Rated Temp. Range	Rated Power Handling
Resistor	R_{SERIES}	In series with VCC	68 Ω	50 V	±15%	–	1/8 W
Capacitor	C_{SUPPLY}	Connected between VCC and GND	100 nF	50 V	±10%	X7R	–

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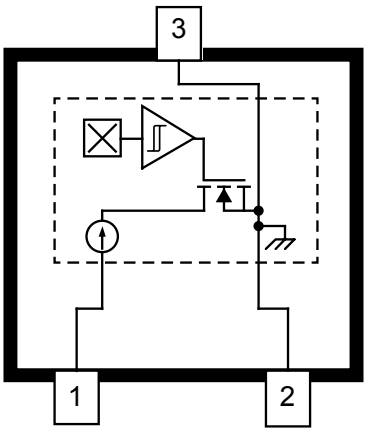
PINOUT DIAGRAMS AND TERMINAL LIST TABLES

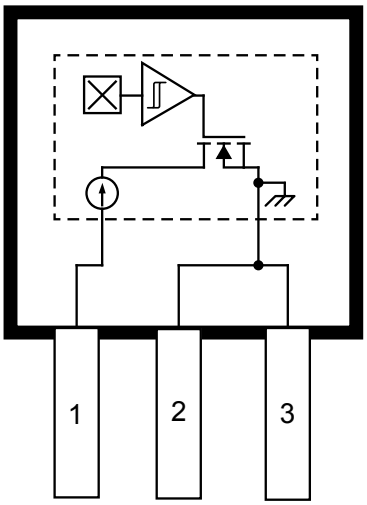
Terminal List Table (LH, UA Packages)

Number	Package Name		Function
	LH	UA	
1	VCC	VCC	Supply voltage
2	GND	GND	Ground terminal
3	GND	GND	Ground terminal

Note: For best performance, tie Pins 2 and 3 together close to the IC.



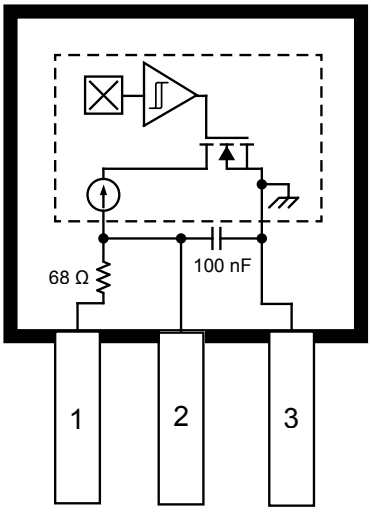
LH Package, 3-Pin SOT23W Pinout



UA Package, 3-Pin SIP Pinout

Terminal List Table (UC Package)

Number	Package Name	Function
	UC	
1	VCC	Supply voltage
2	VINT	This pin reflects the internal voltage, V_{INT}, after the internal series resistor. This pin should be kept floating.
3	GND	Ground terminal



UC Package, 3-Pin SIP Pinout

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ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J(max)$ and C_{BYP} = 0.01 µF, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ. [3]	Max.	Unit
Supply Voltage	V_{CC}	Operating, T_J < 165°C	LH and UA packages	3.0	–	24	V
		Operating, T_J < 165°C	UC package	4.4 [4]	–	24	V
Undervoltage Lockout [4]	$V_{CC(UV)DIS}$	After power-on, as V_{CC} increases, output is forced to POS until this voltage is reached	LH and UA packages	–	2.6	–	V
			UC package	–	3.5	–	V
	$V_{CC(UV)EN}$	After POK, when V_{CC} drops below this voltage, output is forced to POS	LH and UA packages	–	2.3	–	V
			UC package	–	3.2	–	V
Supply Current	$I_{CC(L1)}$	$I_{CC(L1)}$ is the default $I_{CC(L)}$ current		5	–	6.9	mA
	$I_{CC(L2)}$			2	–	5	mA
	$I_{CC(H)}$			12	–	17	mA
	I_{SAFE}	Safe current state; indicates overtemperature or EEPROM error		–	–	1.8	mA
Output Slew Rate	dI/dt	No bypass capacitor; C_L [5] = 20 pF	LH and UA packages	–	50	–	mA/µs
		C_{BYP} = 100 nF; C_L [5] = 20 pF		–	0.22	–	mA/µs
		Internal bypass capacitor; C_L [5] = 20 pF	UC package	–	0.22	–	mA/µs
Power-On Time [6]	t_{PO}	$V_{CC} \geq V_{CC}(min)$, $B > B_{OP}(max)$, $B < B_{RP}(min)$		–	–	70	µs
Power-On State [7]	POS	$t < t_{PO}$, $V_{CC} \geq V_{CC(UV)EN}$		$I_{CC(H)}$			mA
Chopping Frequency	f_C			–	800	–	kHz
Output Jitter (p-p)		1 kHz square wave signal		–	5	–	µs
ON-BOARD PROTECTION							
Supply Zener Clamp Voltage	V_Z	$I_{CC} = I_{CC(H)}$ + 1 mA, T_A = 25°C		40	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RZ}	I_{CC} = –1 mA		–	–	–23	V
Overtemperature Shutdown	T_{SD}	Temperature increasing		–	205	–	°C
Overtemperature Hysteresis	T_{JHYS}			–	25	–	°C

[3] Typical data is at T_A = 25°C and V_{CC} = 12 V unless otherwise noted; for design information only.
[4] UC minimum V_{CC} is higher to accommodate voltage drop in the internal series resistor. UC package minimum V_{CC} is higher to accommodate voltage drop in the internal series resistor. This also affects the $V_{CC(UV)}$.
[5] C_L – scope capacitance.
[6] Measured from $V_{CC} \geq V_{CC}(min)$ to valid output.
[7] Power-on state is defined only when V_{CC} slew rate 1 V/s or greater

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MAGNETIC CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J(max)$ and C_{BYP} = 0.01 µF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [9]	Max.	Unit [10]
Initial Operate Point	$B_{OP(init)}$	T_A = 25°C	60	80	100	G
Programmable Magnetic Operating Point	$B_{OP(range)}$	Switch Mode, T_A = 25°C; 8 bits	±10	–	±600	G
		Latch Mode, T_A = 25°C; 8 bits	±20	–	±600	G
Average Magnetic Step Size [11]	$B_{OP(STEP)}$	T_A = 25°C	2	3	4.5	G
Initial Hysteresis	$B_{HYS(init)}$	T_A = 25°C	5	15	30	G
Average Hysteresis Step Size [12]	$B_{HYS(STEP)}$	T_A = 25°C	1.5	3	5	G
Programmable Hysteresis in Switch Mode	$B_{HYS(range)}$	T_A = 25°C; 5 bits. Switch mode only. In latch mode, hysteresis is 2 × B_{OP}	15	–	70	G
Initial Release Point	$B_{RP(init)}$	T_A = 25°C	45	–	85	G
Switch Point Temperature Coefficient	TCSEL	00: Flat	–	0	–	%/°C
		01: SmCo	–	–0.035	–	%/°C
		10: NdFeB	–	–0.12	–	%/°C
		11: Ferrite. This is the default value.	–	–0.2	–	%/°C
Initial Operate Point Over Temperature	$B_{OP(init)\_T}$	T_A = –40°C; default programming, ferrite temperature coefficient	65	–	113	G
		T_A = 150°C; default programming, ferrite temperature coefficient	49	–	80	G
Initial Release Point Over Temperature	$B_{RP(init)\_T}$	T_A = –40°C; default programming: $B_{OP(init)}$ = 80 G (typ) at 25°C and ferrite temperature coefficient	51	–	98	G
		T_A = 150°C; default programming: $B_{OP(init)}$ = 80 G (typ) at 25°C and ferrite temperature coefficient	36	–	72	G
Initial Hysteresis Over Temperature	$B_{HYS(init)\_T}$	T_A = –40°C; default programming, ferrite temperature coefficient	5	–	30	G
		T_A = 150°C; default programming, ferrite temperature coefficient	5	–	30	G

[9] Typical data is at T_A = 25°C and V_{CC} = 12 V, unless otherwise noted; for design information only.
[10] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and a positive value for south-polarity magnetic fields.
[11] $B_{OP(STEP)}$ is a calculated average from the cumulative programmed bits.
[12] $B_{HYS(STEP)}$ is a calculated average from the cumulative programmed bits.

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PROGRAMMING CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J(max)$ and C_{BYP} = 0.01 µF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Switch Point Magnitude Selection Bits	BOPSEL		–	8	–	bit
Magnetic Polarity Bits	BOPPOL	The default value is 0 for south polarity.	–	1	–	bit
Unipolar/Omnipolar Selection Bit	UNI	These bits configure whether the device operates like a unipolar or omnipolar switch or latch.	–	1	–	bit
Switch/Latch Selection Bit	LATCH		–	1	–	bit
Magnetic Hysteresis	HYS	If configured as a latch, this selection is ignored and the hysteresis is 2 × BOPSEL	–	5	–	bit
Output Current Level Selection	ICCL	If this bit = 0, ICCL = ICCL2. If this bit = 1, ICCL = ICCL1. This is the default value.	–	1	–	bit
Temperature Coefficient	TCSEL	The default value is 11 for Ferrite temperature coefficient.	–	2	–	bit
Output Polarity Bits	POL	The default value is 0 for Standard output polarity.	–	1	–	bit
Customer ID	CUSTID	The default value is 0.	–	10	–	bit
Device Lock Bits	LOCK	The default value is 0.	–	1	–	bit

Bit		Description
UNI	LATCH	
0	X	Omnipolar Switch
1	0	Unipolar Switch (default setting)
1	1	Latch

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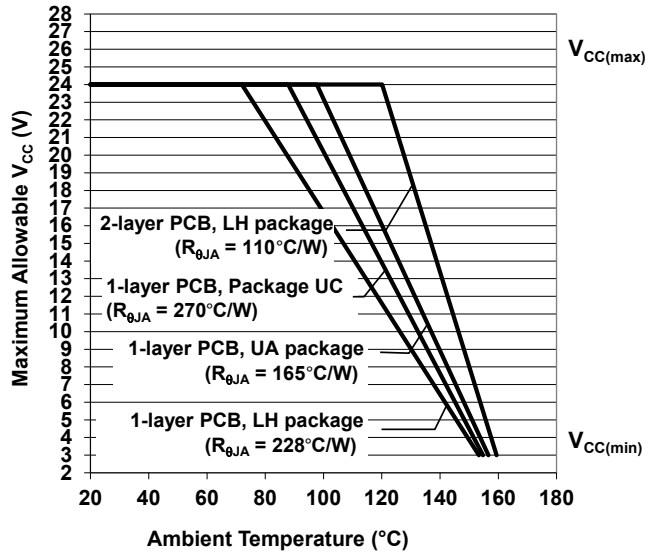
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

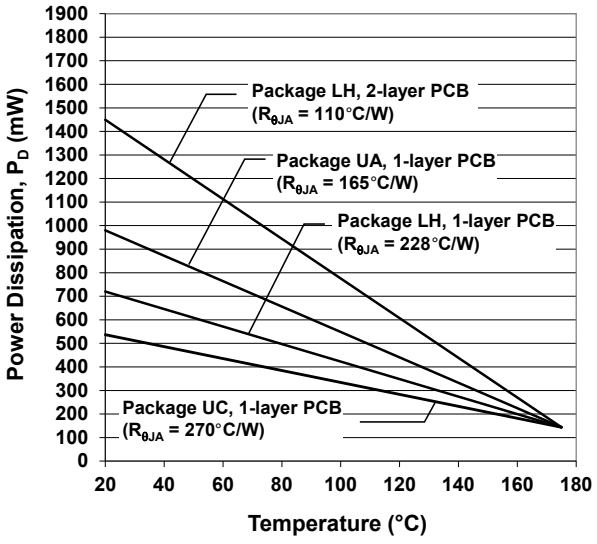
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, on 1-layer PCB based on JEDEC standard	228	°C/W
		Package LH, on 2-layer PCB with 0.463 in.^{2} of copper area each side	110	°C/W
		Package UA, on 1-layer PCB with copper limited to solder pads	165	°C/W
		Package UC, on 1-layer PCB with copper limited to solder pads	270	°C/W

*Additional thermal information available on the Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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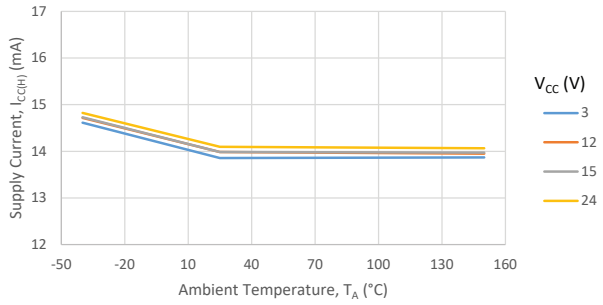
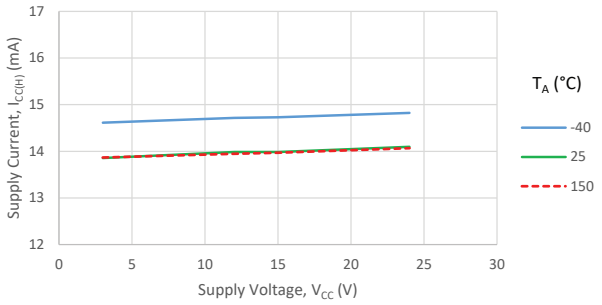
CHARACTERISTIC PERFORMANCE DATA

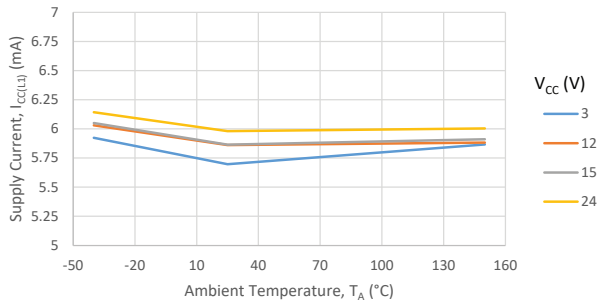
$I_{CC(H)}$ vs. T_A



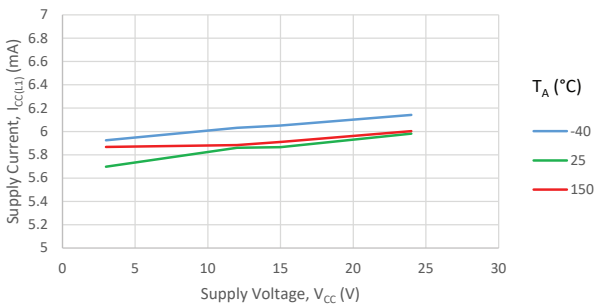
$I_{CC(H)}$ vs. V_{CC}



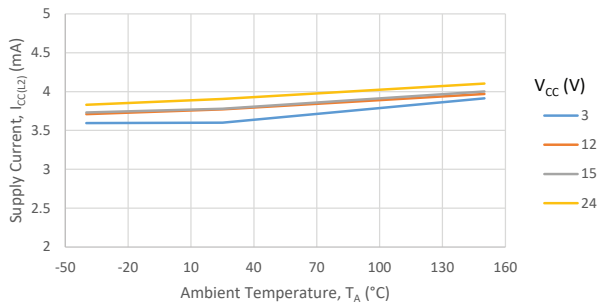
$I_{CC(L1)}$ vs. T_A



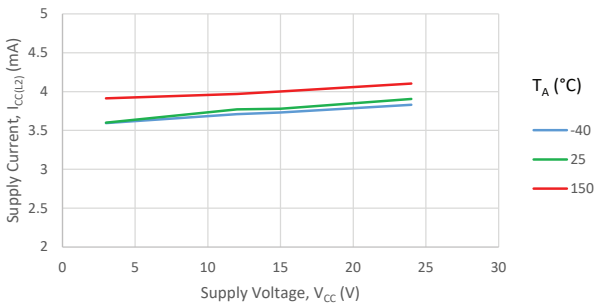
$I_{CC(L1)}$ vs. V_{CC}



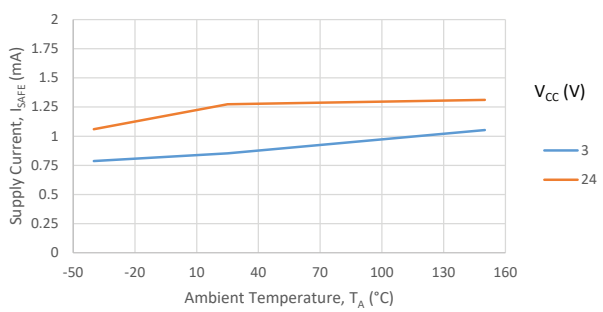
$I_{CC(L2)}$ vs. T_A



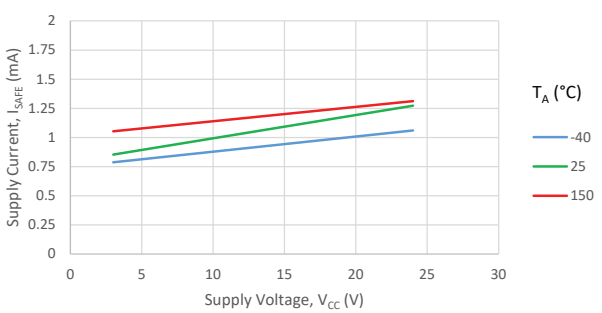
$I_{CC(L2)}$ vs. V_{CC}



I_{SAFE} vs. T_A



I_{SAFE} vs. V_{CC}



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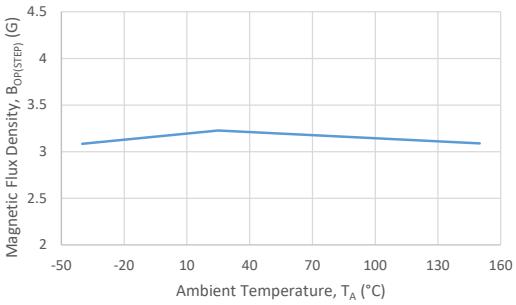
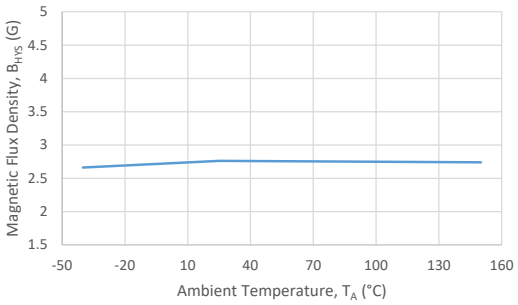
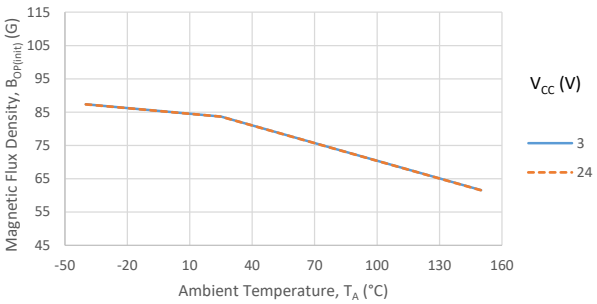
$B_{OP(STEP)}$ vs. T_A



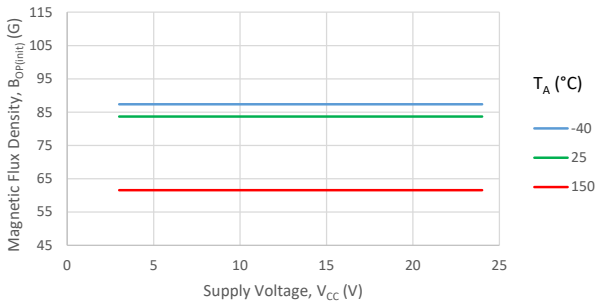
$B_{HYS(STEP)}$ vs. T_A



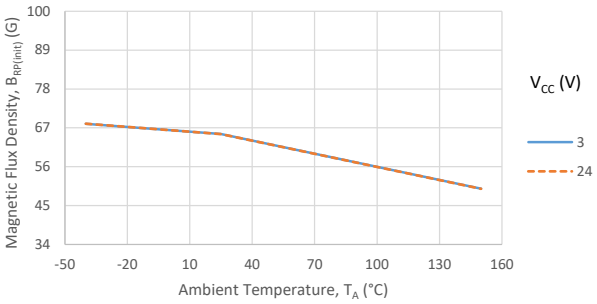
$B_{OP(init)\_T}$ vs. T_A



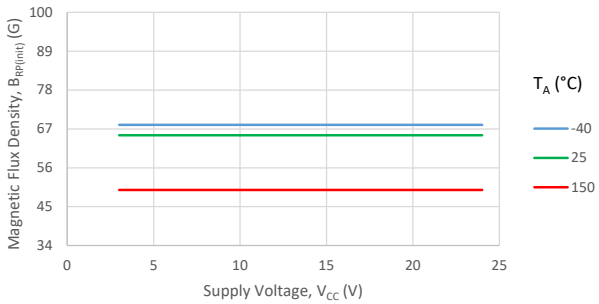
$B_{OP(init)\_T}$ vs. V_{CC}



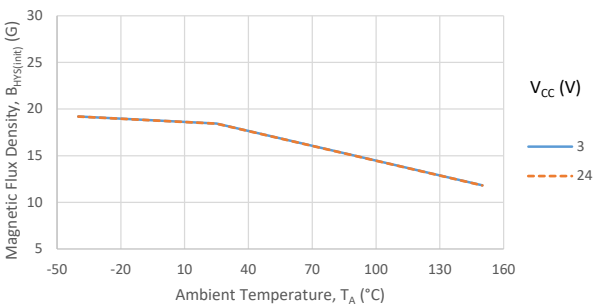
$B_{RP(init)\_T}$ vs. T_A



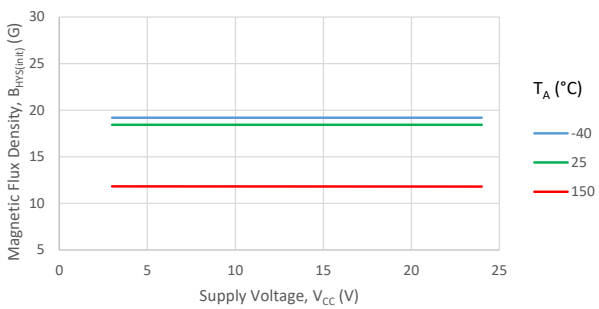
$B_{RP(init)\_T}$ vs. V_{CC}



$B_{HYS(init)\_T}$ vs. T_A



$B_{HYS(init)\_T}$ vs. V_{CC}



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FUNCTIONAL DESCRIPTION

Functional Safety

The APS11900 was designed in accordance with the international standard for automotive functional safety, ISO 26262:2011 (pending assessment). This product achieves an ASIL (Automotive Safety Integrity Level) rating of ASIL A according to the standard. The APS11900 is classified as a SEooC (Safety Element out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. Contact your local FAE for A²-SIL™ documentation: www.allegromicro.com/ASIL.

The APS11900 has internal diagnostics to check the voltage supply (an undervoltage lockout regulator) and to detect overtemperature conditions. See the Diagnostics section for more information.

Operation

The APS11900 devices are two-wire EEPROM-based field-programmable planar Hall-effect devices. The user can select whether the device should respond to a north or south magnetic field (unipolar) or both (bipolar or omnipolar). There is a choice of two output current levels, $I_{CC(L1)}$ and $I_{CC(L2)}$, and the user can determine which output state applies, $I_{CC(L)}$ or $I_{CC(H)}$, when the magnetic field is present.

The difference between the magnetic operate and release points is the hysteresis, B_{HYS}. Hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The user can program the desired hysteresis level when configured as a switch. When configured as a latch, the hysteresis is automatically set to double the programmed operating point, B_{OP}.

Figure 1 shows the potential unipolar and omnipolar options that APS11900 can be configured for when it is used as a switch. Figure 2 shows the output options when configured as a latch. The direction of the applied magnetic field is perpendicular to the branded face for the APS11900. See Figure 3 for an illustration.

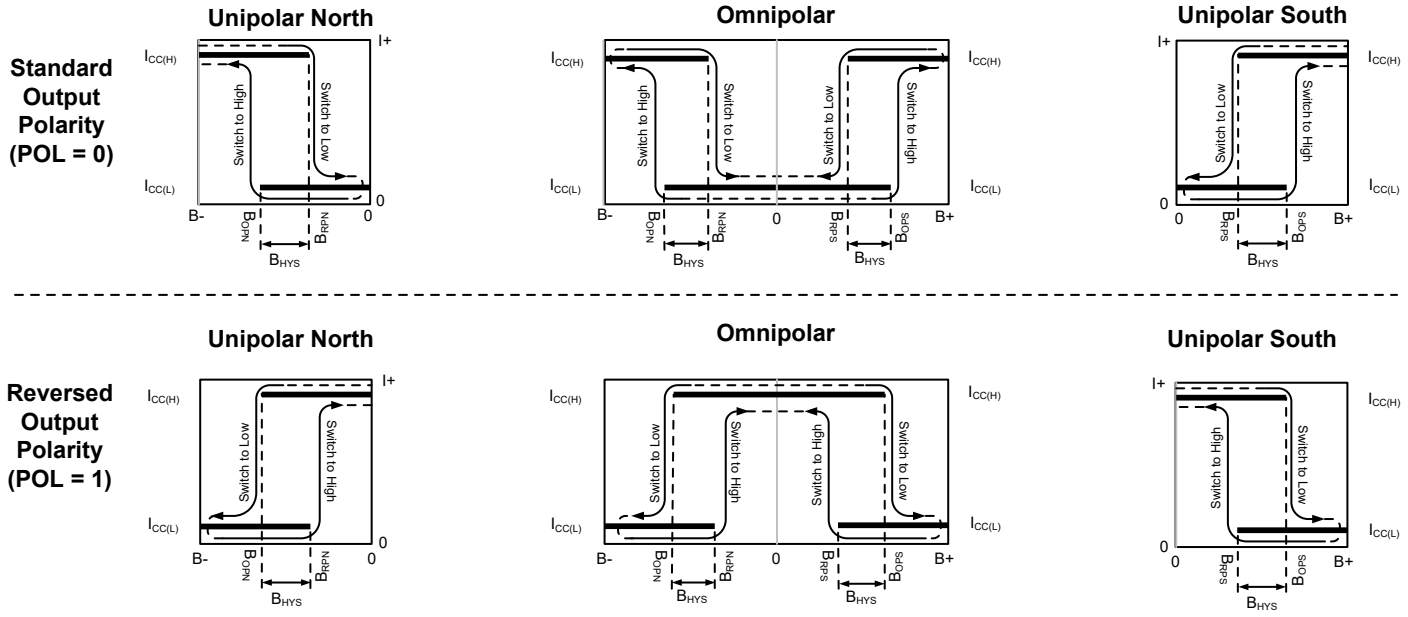

Figure 1: Hall Switch Magnetic and Output Current Polarity Options

B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.

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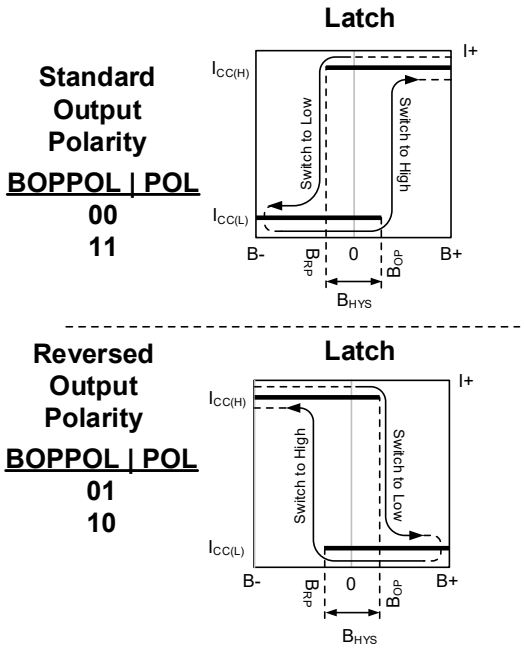

Figure 2: Hall Latch Magnetic and Output Current Polarity Options

B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.

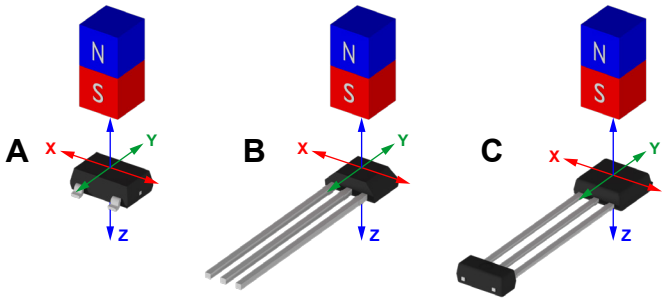

Figure 3: Magnetic Sensing Orientations

APS11900 LH (Panel A), UA (Panel B), and UC (Panel C)

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Power-On Behavior

The APS11900 has an internal voltage regulator with undervoltage lockout. As the device powers up, it stays in the power-on state (POS) of $I_{CC(H)}$ until the supply voltage exceeds $V_{CC(UV)DIS}$. Then the device reads the device configuration registers from EEPROM and checks that the EEPROM values are valid by comparing the calculated Error Correction Code (ECC) for each register against the stored ECC. After t_{PO}, the current consumption is $I_{CC(L)}$ or $I_{CC(H)}$, according to the magnetic field and the device configuration, as shown in Figure 1 and Figure 2.

Similarly, when the supply voltage decreases, the device returns to the power on state (POS) when the supply voltage drops below $V_{CC(UV)EN}$, as shown in Figure 4.

When the device powers on in the hysteresis range (less than B_{OP} and higher than B_{RP}), the output corresponds to the power-on state. In this case, the correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

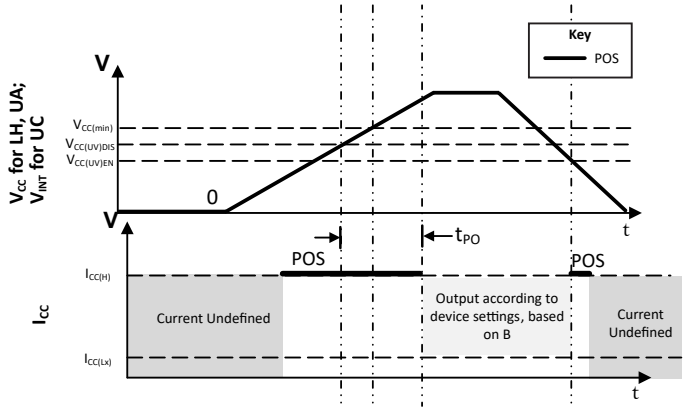

Figure 4: Power-On/UVLO Behavior

Diagnostic Features

When properly supplied, APS11900 always has current flowing at a specified level: either $I_{CC(H)}$, $I_{CC(L)}$, or I_{SAFE}. Any current outside of these narrow ranges is a fault condition. If there is a short, current increases so that $I_{CC} > I_{CC(H)}$ (max), outside the valid $I_{CC(H)}$ range. If there is an open, the current lowers below the $I_{CC(L)}$ (min), outside the valid output current range. In this way, connectivity issues between the ECU and the sensor can easily be detected.

Additionally, the APS11900 has an overtemperature feature: if the junction temperature increases beyond T_{JF}, then the current is reduced to I_{SAFE}. The device current also changes to I_{SAFE} if there is an error in the EEPROM ECC which is checked at power-on and after an overtemperature event. There is a LOCK bit which should be set once end-of-line programming has been completed. Setting the LOCK bit prevents any change in device configuration in the field.

Any value of I_{CC} between the allowed ranges for $I_{CC(H)}$ and $I_{CC(L)}$ indicates a general fault condition.

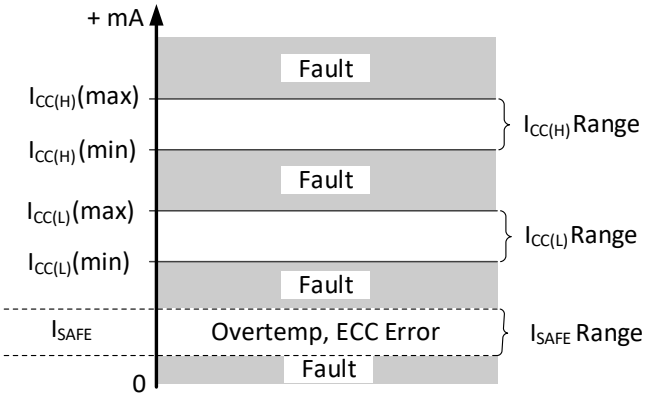

Figure 5: Interpreting I_{CC} for System-Level Diagnostics

Temperature Coefficient and Magnet Selection

The APS11900 allows the user to select the magnetic temperature coefficient to compensate for drifts of SmCo, NdFeB, and ferrite magnets over temperature—as indicated in the specifications table on page 5. This compensation improves the magnetic system performance over the entire temperature range. For example, the magnetic field strength from ferrite decreases as the temperature increases from 25°C to 150°C. This lower magnetic field strength means that a lower switching threshold is required to maintain switching at the same distance from the magnet to the sensor. Correspondingly, higher switching thresholds are required at cold temperatures, as low as –40°C, due to the higher magnetic field strength from the ferrite magnet.

For example, the typical ferrite compensation is –0.2%/°C. With a 25°C temperature B_{OP} switch point of 80 G, the switch point changes nominally by –0.2%/°C × 80 × (150°C – 25°C) = –20 G to 80 G – 20 G = 60 G at 150°C. And at –40°C, the switch point changes by –0.2%/°C × 80 × (–40°C – 25°C) = 10 G to 80 G + 10 G = 90 G. The APS11900 compensate the switching thresholds over temperature as described above. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.

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Applications

For the LH and UA packages, an external bypass capacitor (from 0.01 µF to 0.1 µF) should be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization. Some applications may require additional EMC immunity, which is achieved with an enhanced protection circuit. For example, increasing the bypass capacitor from 0.01 µF to 0.1 µF improves immunity to Powered ESD (ISO 10605) and Direct Capacitive Coupling.

A series resistor and a 0.1 µF bypass capacitor is integrated into the UC package, making it easy to achieve an EMC-robust design with no external components or PCB required.

Note that the bypass capacitor selection directly affects the slew rate. See the Electrical Characteristics table for the typical slew rate with 0.1 µF bypass capacitor. A 0.01 µF bypass capacitor slew rate is ten times faster. Typical application circuits are shown in “Figure 6: Typical Application Circuits” on page 14.

Extensive applications information for Hall-effect devices is available in:

- *Hall-Effect IC Applications Guide*, AN27701
- *Hall-Effect Devices: Guidelines For Designing Subassemblies Using Hall-Effect Devices*, AN27703.1
- *Soldering Methods for Allegro’s Products – SMT and Through-Hole*, AN26009
- www.allegromicro.com/ASIL

All are provided on the Allegro website:

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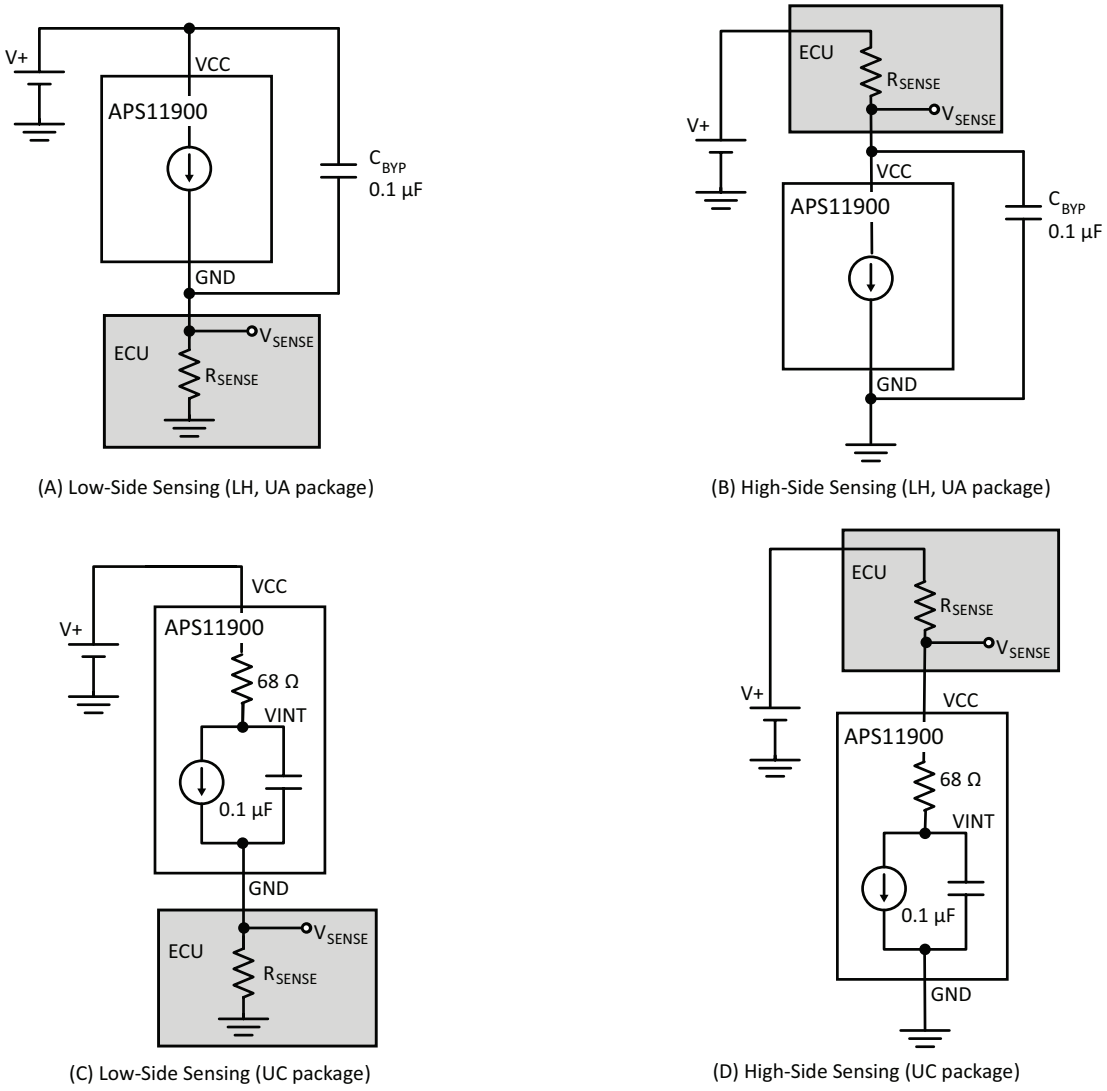

Figure 6: Typical Application Circuits

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Chopper Stabilization Technique

A limiting factor for switch point accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. “Figure 7: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)” illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro’s innovative chopper-stabilization technique uses a high-frequency clock.

The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS11900 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

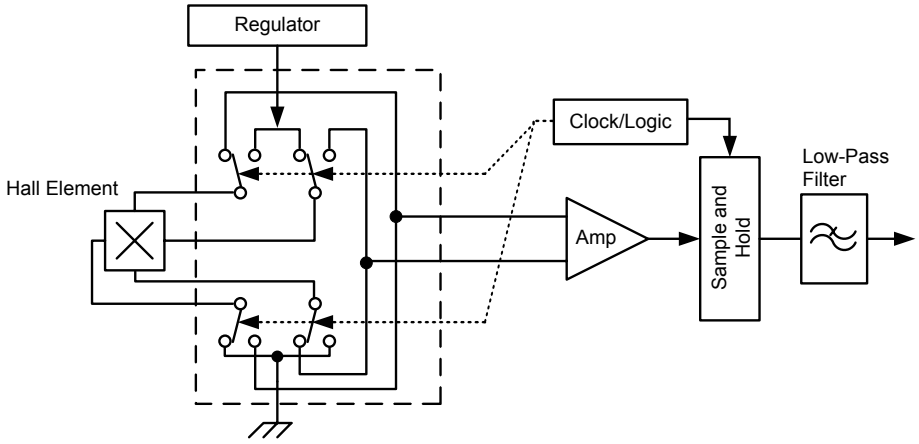

Figure 7: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

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POWER DERATING

The device must be operated below the maximum junction temperature, T_J (max). Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance (junction to ambient), $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. $R_{\theta JA}$ is dominated by the Effective Thermal Conductivity, K, of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions: T_A = 25°C, V_{CC} = 12 V, I_{CC} = 6 mA, and $R_{\theta JA}$ = 110°C/W for the LH package, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 6\ mA = 72\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 72\ mW \times 110°C/W = 7.92°C$$

$$T_J = T_A + \Delta T = 25°C + 7.92°C = 32.92°C$$

Determining Maximum V_{CC}

For a given ambient temperature, T_A, the maximum allowable power dissipation as a function of V_{CC} can be calculated. P_D (max) represents the maximum allowable power level without exceeding T_J (max) at a selected $R_{\theta JA}$ and T_A.

Example: V_{CC} at T_A = 150°C, package UA, using low-K PCB. Using the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 165°C/W, T_J (max) = 165°C, V_{CC} (max) = 24 V, and I_{CC} (max) = 17 mA, calculate the maximum allowable power level, P_D (max).

First, using equation 3:

$$\Delta T\ (max) = T_J\ (max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, from equation 2:

$$P_D\ (max) = \Delta T\ (max) \div R_{\theta JA} = 15°C \div 165°C/W = 91\ mW$$

Finally, using equation 1, solve for maximum allowable V_{CC} for the given conditions:

$$V_{CC}\ (est) = P_D\ (max) \div I_{CC}\ (max) = 91\ mW \div 17\ mA = 5.4\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ V_{CC} (est).

If the application requires $V_{CC} > V_{CC(est)}$ then $R_{\theta JA}$ must by improved. This can be accomplished by adjusting the layout, PCB materials, or by controlling the ambient temperature.

Determining Maximum T_A

In cases where the V_{CC} (max) level is known, and the system designer would like to determine the maximum allowable ambient temperature T_A (max), for example, in a worst-case scenario with conditions V_{CC} (max) = 24 V, I_{CC} (max) = 17 mA, and $R_{\theta JA}$ = 228°C/W for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 24\ V \times 17\ mA = 408\ mW$$

Then, by rearranging equation 3 and substituting with equation 2:

$$T_A\ (max) = T_J\ (max) - \Delta T$$

$$T_A\ (max) = 165°C - (408\ mW \times 228°C/W)$$

$$T_A\ (max) = 165°C - 93°C = 72°C$$

Finally, note that the T_A (max) rating of the device is 150°C and performance is not guaranteed above this temperature for any power level.

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PROGRAMMING GUIDELINES

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VCC (supply) pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as high (V_{PH}), mid (V_{PM}), and low (V_{PL}).

The APS11900 family allows the user to write to volatile configuration registers, called shadow registers, to “try” the configuration. Then the device configuration can be written to EEPROM, nonvolatile memory.

Shadow registers are reset after cycling the supply voltage.

EEPROM has a limited number of write cycles. For this reason, it is recommended to use the Shadow registers (“Try Mode”) to determine the correct device configuration.

After the desired device configuration has been determined, write the values into the device EEPROM and write the lock bit to prevent further access to the EEPROM.

After power-on, the EEPROM registers are read and the values are written into the shadow registers as described in the section “Power-On Behavior” on page 12 of this datasheet.

The following functionality is available through the APS11900 programming interface:

Function	Description
Shadow Register Write	Write volatile configuration registers in “Try Mode”.
Shadow Register Read	Read volatile configuration registers in “Try Mode”.
EEPROM Register Write	Write configuration to non-volatile memory (EEPROM). Note that EEPROM has limited write cycles as described in the Absolute Maximum Specifications table.
EEPROM Register Read	Read non-volatile configuration registers (EEPROM).
EEPROM Margining	Procedure to validate that the EEPROM bank was written successfully.
Increment BOP	This mode allows the user to increment BOPSEL each time a HV pulse is sent.
Decrement BOP	This mode allows the user to decrement BOPSEL each time a HV pulse is sent.
Increment BHYS	This mode allows the user to increment BHYS each time a HV pulse is sent.
Decrement BHYS	This mode allows the user to decrement BHYS each time a HV pulse is sent.

Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, ASEK-20, available through your local Allegro sales representative. The manual for the kit is available for download on the Allegro MicroSystems website.

For detailed programming instructions, refer to the APS11900 Customer EEPROM Programming manual.

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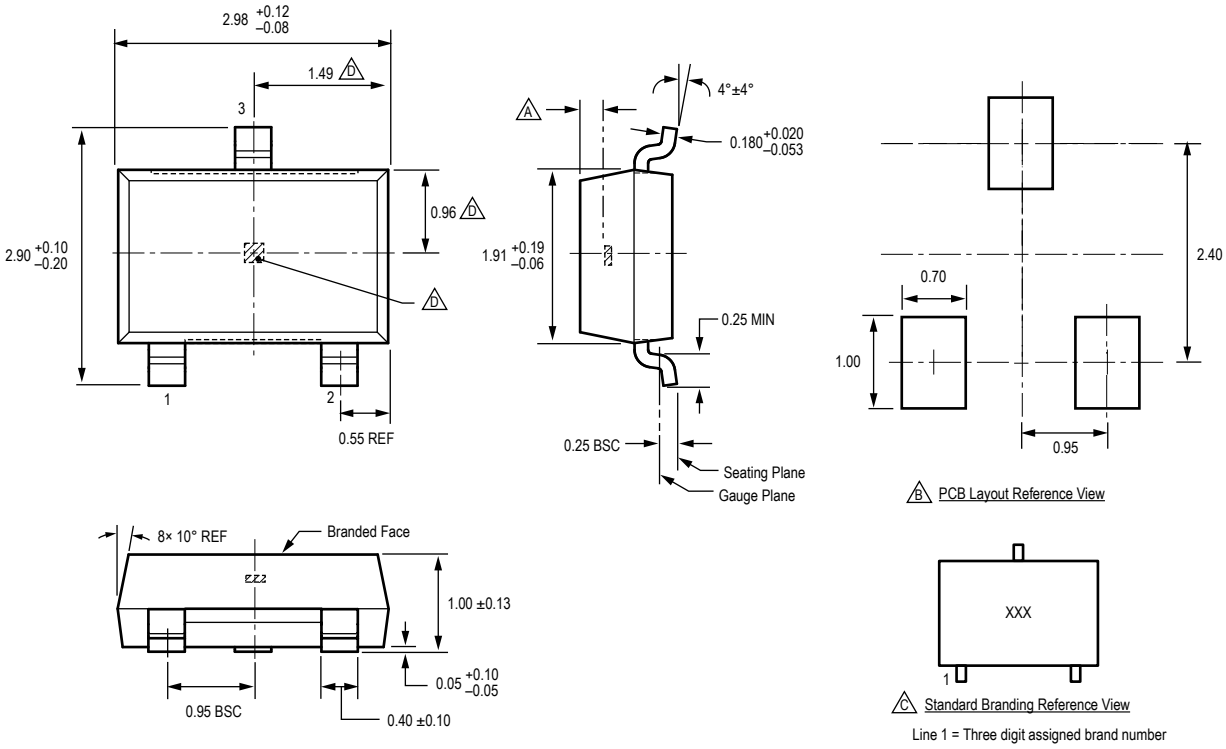
Package LH, 3-Pin SOT23W



For reference only; not for tooling use (reference DWG-0000055).
Dimensions in millimeters.
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions.
Exact case and lead configuration at supplier discretion within limits shown.

A Active Area Depth, 0.28 ±0.04 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

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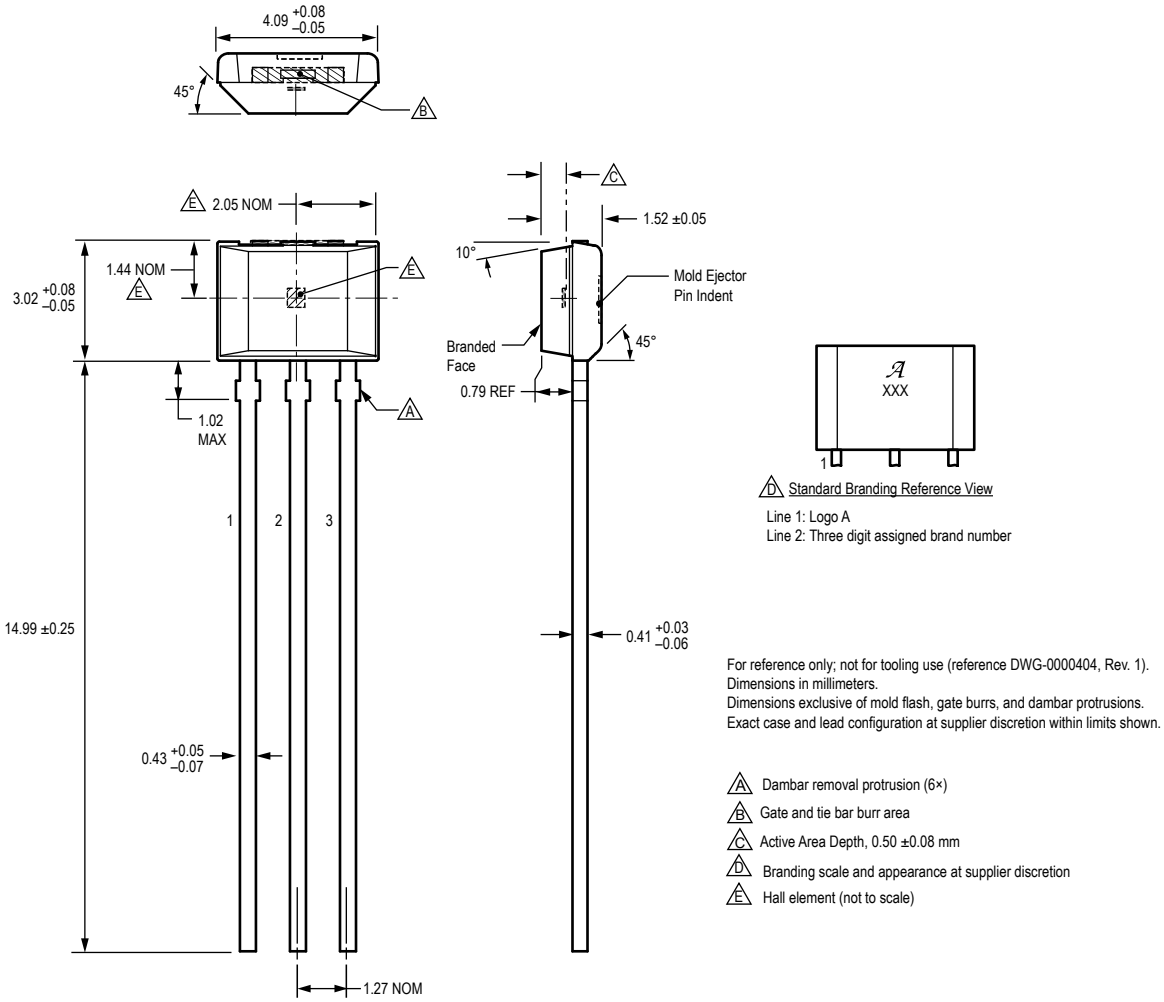
Package UA, 3-Pin SIP



For reference only; not for tooling use (reference DWG-0000404, Rev. 1).
Dimensions in millimeters.
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions.
Exact case and lead configuration at supplier discretion within limits shown.

A Dambar removal protrusion (6×)
B Gate and tie bar burr area
C Active Area Depth, 0.50 ±0.08 mm
D Branding scale and appearance at supplier discretion
E Hall element (not to scale)

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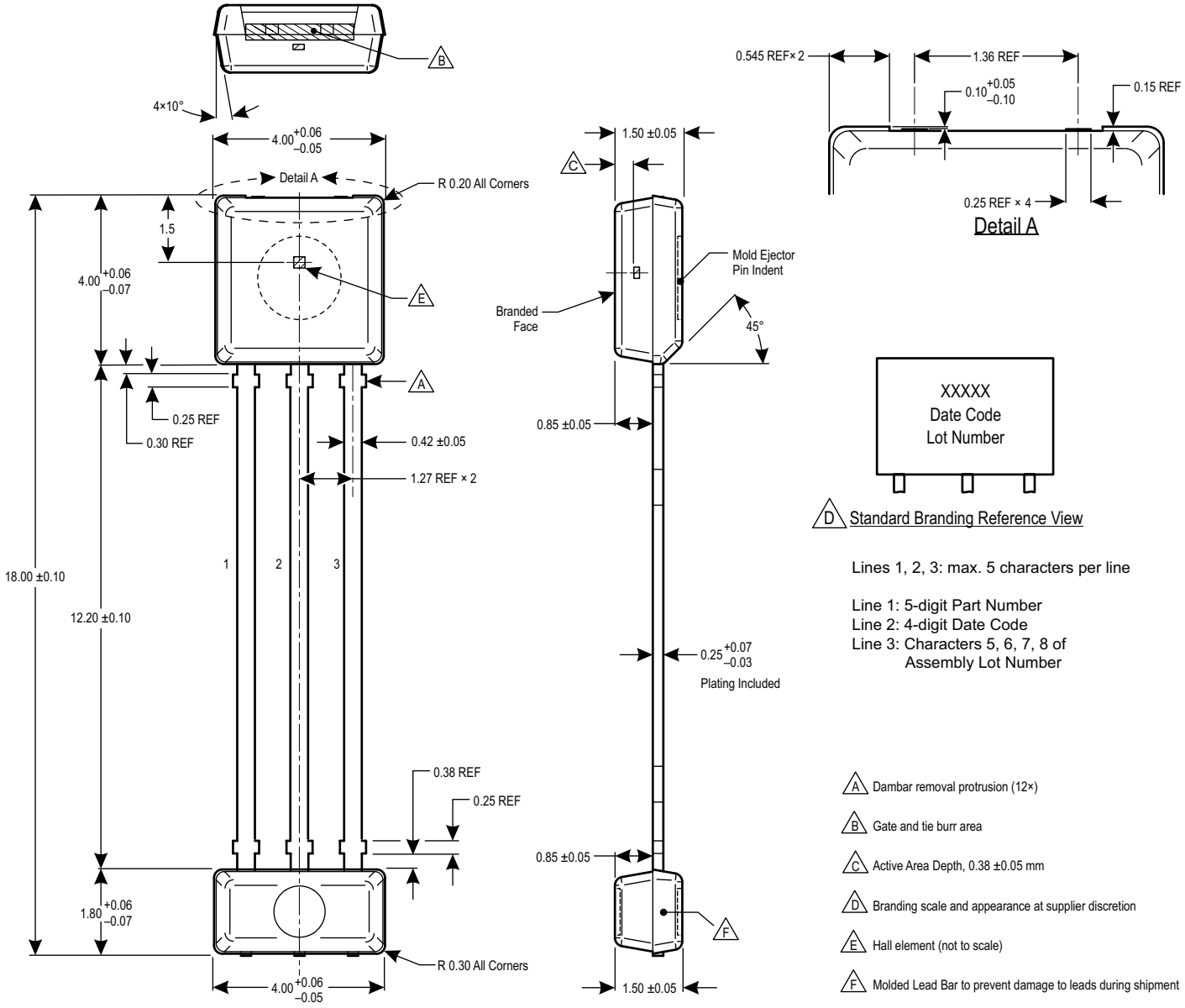
Package UC, 3-Pin SIP

For Reference Only – Not for Tooling Use

(Reference DWG-0000409, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Lines 1, 2, 3: max. 5 characters per line

Line 1: 5-digit Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

A Dambar removal protrusion (12×)

B Gate and tie burr area

C Active Area Depth, 0.38 ±0.05 mm

D Branding scale and appearance at supplier discretion

E Hall element (not to scale)

F Molded Lead Bar to prevent damage to leads during shipment

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REVISION HISTORY

Number	Date	Description
–	March 23, 2018	Initial release
1	April 18, 2018	Corrected supply current values and plots (pages 4 and 8)
2	February 4, 2019	Minor editorial updates
3	April 1, 2019	Updated ASIL status (page 1 and 10)
4	April 20, 2020	Updated selection guide (page 2) and minor editorial updates

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